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An Advanced Seven Level Multilevel Inverter Technique for Grid-Connected System Applications with Reduced Switching Devices

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ABSTRACT

Multilevel inverter execution is high thought about to the regular two level inverters due to their decreased harmonic distortion, lower electromagnetic interference. However the principle disadvantage of multilevel inverter is expanded number of switches, complex pulse width modulation control and adjusting of capacitor voltages. This paper proposes a 1-phase seven level inverter for grid connected systems. The proposed inverter topology comprises of less equipments with low complexity control drives and control signals. A LC channel is used to restrain the exchanging current ripple by giving high weakening of harmonic and high unique execution. This paper additionally displays the most important control and modulation strategies by another reference based PWM plot utilizing three comparable reference signals with a counterbalance of greatness equivalent to the adequacy of the carrier signal. The whole system is numerically reenacted utilizing MATLAB/SIMULINK and the simulation results are presented.

***Keywords* :*Inverter, LC Filter, Multilevel Inverter(MLI), Sinusoidal Pulse Width-Modulation Topology*.**

I. INTRODUCTION

Multilevel inverters concept was introduced more than twenty years ago for power conversion. The general concept includes utilization of higher number of semiconductor devices to power transformation with less voltage steps. We have several advantages with this topology as compared to that of the conventional power conversion topology. Different techniques are proposed in the literature as multilevel converters [1] gives some of the distinctiveness in common which direct to some of these obvious advantages.

- Reduction in the voltages connected to the main power devices, empowering operation at higher load voltages
- Transient voltages consequently restricted
- Production of higher power quality waveform, moved forward electromagnetic similarity
- They draw input current with low distortion.

The primary detriment related with the multilevel designs is their circuit intricacy, which requires high number of energy switches that must be controlled in a unequivocally decided grouping by a committed (and complex) Pulse width Modulation (PWM) circuit. They additionally require incredible number of dc levels for the generation of littler voltage steps, which are given by disconnected voltage sources or by a cluster of capacitive voltage dividers. Accessibility of disconnected voltage sources is bit a troublesome, and keeping the capacitive divider arrange under adjust additionally expands the many-sided quality of PWM hardware. To beat this voltage-adjusting issue, need of another multilevel converter may emerge [2]. In later a long time, new converter topologies and special modulation strategies are the consequence of expanded enthusiasm toward the research of multilevel power change. Multilevel converter frameworks are by and large delegated course inverters, diode clamping inverters, and flying-capacitor inverters. There are likewise some blend of the previously mentioned topologies which involves three-level diode-clipped converter fell with two level converter known as as cascade 3/2 converter and we will design a 5 level multi level inverter by combining the three level cascade converter and five level neutral point multilevel converter [3]. Multilevel converters have discovered across the board applications in industry. They can be utilized as a part of footing applications in the transportation business, matrix reconciliation of sustainable power sources [4], FACT's systems and vehicle impetus systems.

The technique proposed in this paper is similar since the estimations of all the DC connect voltage sources are equivalent. However there are couple of uneven topologies that require voltage sources of various values [5]. This asymmetry comes about in the need of dc voltage sources having a particular connection amongst them and furthermore the distinction in rating of the semiconductor devices is a main disadvantage. A portion of the topologies like the one proposed in [6] experiences complexities engaged with capacitor balancing.

This paper introduces an outline of another seven level inverter topology which has been created from the reversing voltage (RV) topology introduced in [7]. The advanced converter topology utilized as a part of the power arrange offers an essential change regarding lower devices count and decrease in circuit design than the previous techniques. This is more reliable and simpler control system for inverter and also the inverter efficiency is also more because of control switches operates at high frequency and no. of switches conducting current is less.

II PRESENTED INVERTER TECHNIQUE

2.1 Circuit Description

In Previous multilevel inverters, the power devices are worked to provide high- frequency responses in both negative and positive polarities. However, to produce bipolar levels, we need not to use all the switches. This is the simple idea that has been get into practice by the presented technique. In this technique, there are two stages i.e. namely level generator and polarity generator. Level generator stage takes responsibility to produce

levels in positive and negative polarity similarly polarity of the output voltage can complete by polarity generator stage. For generating the required levels, High switching frequency capability power semiconductor devices are used in the level generator stage. Coming to polarity generation stage line frequency power semiconductor devices are used. Then the positive polarity generated by the level generator is send to a Full bridge converter i.e polarity generator. Then required polarity of the output voltage is generated by polarity generator. This topology can be easily used to higher voltage level by decoupling the center stage as shown in below fig.

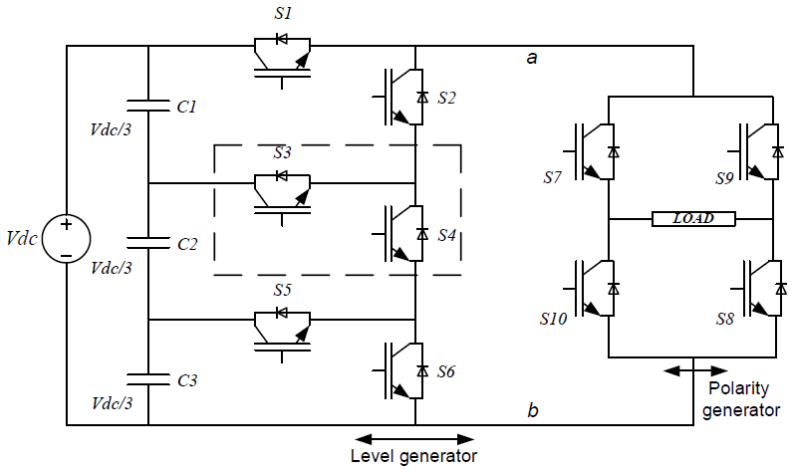

Fig. 2.1 configuration of presented single phase seven-level inverter.

2.2 Operation

Table I Shows The switching sequences named as level 0, level 1, level 2, level 3 for the generation of positive levels (0, Vdc/3, 2Vdc/3, Vdc). By observing the table, to control the inverter there are four possible switching states. The level generator will generate The required output positive voltage levels. Four stages are:

Level	0	1	2	3
Active Switches	2-4-6	2-4-5	2-3	1

2.2.1 Level I (Zero output voltaage level)

In this level conducting Switches are S_2 , S_4 , S_6. Then the conducting switches short circuits the input terminal ab of the polarity generator. Which is results in the generation of zero voltage (level 0). Current paths that are active at this stage are described by below Fig.

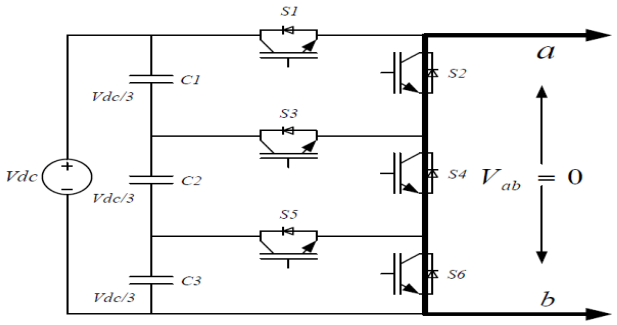

Fig. 2.2.1. Switching sequence required to produce output voltage level I.

2.2.2 Level II (V_{dc}/3 output level)

In this level conducting Switches are S_2 , S_4 , S_5. Then the conducting switches are connecting the terminal a to V_{dc}/3 and terminal b i.e remaining terminal to ground. As all other remaining high frequency controlled devices are OFF. Then the output voltage from the circuit V_{dc} / 3 as output generation. Current paths that are active at this stage are described by below Fig.

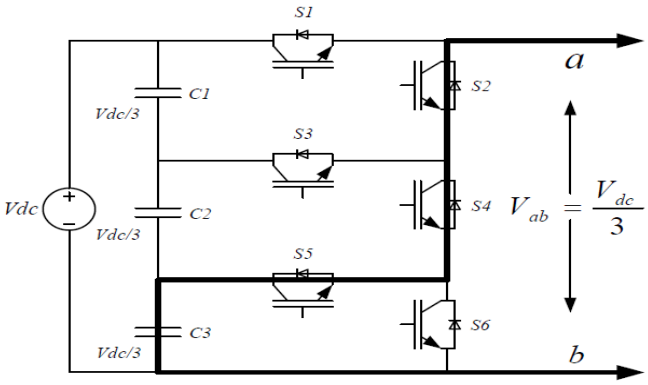

Fig. 2.2.2 Switching configuration required to produce output voltage level 1I.

2.2.3 Level III ($2V_{dc}$/3 output level

In this level conducting Switches are S_2 , S_3. Then the conducting switches are connecting the terminal a to $2V_{dc}$/3 which will derived from the combination of two equal capacitor voltages and terminal b i.e remaining terminal to ground. As all other remaining high frequency controlled devices are OFF. Then the output voltage from the circuit $2V_{dc}$ / 3 i.e Level II as output generation. Current paths that are active at this stage are described by below Fig.

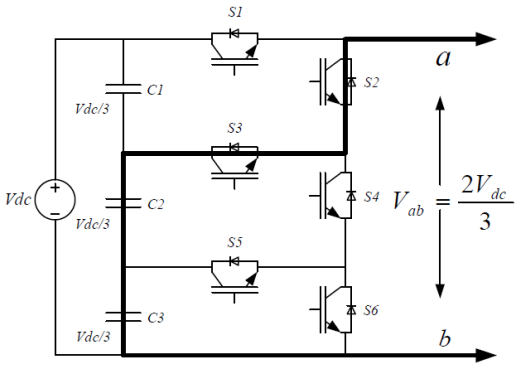

Fig. 2.2.3 Switching configuration required to produce output voltage level III.

2.2.4 Level IV (Max. positive output level)

In this level conducting Switch is S_1 only. Then the conducting switch is going to connect the terminal a to V_{dc} which will derived from the combination of three equal capacitor voltages and terminal b i.e remaining terminal to ground. As all other remaining high frequency controlled devices are OFF. Then the output voltage from the circuit is $2V_{dc}$ / 3 i.e Level II as output generation. Current paths that are active at this stage are described by below Fig.

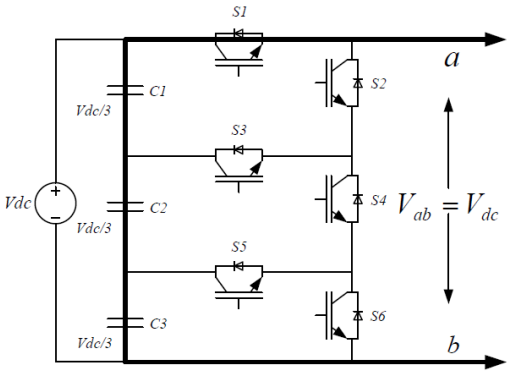

Fig. 2.2.4 Switching configuration required to generate output voltage level IV.

III NUMBER OF COMPONENTS USED

Number of high-switching frequency power semiconductor devices required in This Advanced technique is very less which is very important advantage of the presented technique which results in increase in reliability of the converter. We will easily know that the switching devices number of power stage is very less than that of remaining techniques some of them are a new and highly improved multilevel stage, the neutral point clamped and diode clamped designs. In future, by increasing number of voltage levels, the number devices which are used for switching purposewill decrease tremendously.

Table I

Representation of conducting Switches to generate Level I, II. III & IV

S.No.	Level	Conducting Switches
1	Level I	Devices S_2, S_4, S_6
2	Level II	Devices S_2, S_4, S_5
3	Level III	Devices S_2, S_3
4	Level IV	Device S_1

The difference between the numbers of devices required for different types of seven level inverters configurations are shown in Below Table,

Table II

S.No	Multilevel Inverter Type	Main Switches	DC bus capacitors	Main Diodes	Total Devices
1	Presented Technique	10	3	10	23
2	Cascaded	12	3	12	27
3	Flying Capacitor	12	6	12	30
4	NPC	12	6	12	30

IV PULSE WIDTH MODULATION

The Inverter operates in three(3) states in one half cycle of the output frequency of 50Hz. Normally we all know that PWM gating singles for switches are generated by comparing by three(3) reference signals (V_{r1}, V_{r2}, V_{r3}) with a carrier signal (V_{car}) [8]. The reference signals (V_{r1}, V_{r2}, V_{r3}) which are compared with carrier signals have the same frequency equal to line frequency and equal amplitude. The reference signals (V_{r1}, V_{r2}, V_{r3}) which are compared with carrier signals are in phase with each signal in comparison with an offset amplitude same to the value of the carrier signal. Three reference signals (V_{r1}, V_{r2}, and V_{r3}) are compared with the carrier signal (V_{car}) at a time cycle by cycle. If First reference signal i.e V_{r1} exceeds the peak of the carrier signal V_{car}, Second reference signal i.e V_{r2} will come into action and that will be compared with the carrier signal V_{car} until it exceeds the peak of carrier signal i.e V_{car}. Then onwards Third reference signal i.e V_{r3} will come into action and that will be compared with the carrier signal V_{car} until it crosses Zero. When Third reference signal i.e V_{r3} crosses zero, Second reference signal ,V_{r2} will be compared again until it crosses zero. Then onwards First reference, V_{r1} will be compared with carrier Signal, V_{car}.

The three states which are explained above are described below:

$$\text{State1: } 0 < \omega t < \omega t1 \quad \text{and} \quad \omega t_4 < \omega t < \pi$$
$$\text{State1: } \omega t_1 < \omega t < \omega t_2 \quad \text{and} \quad \omega t_3 < \omega t < \omega t_4$$
$$\text{State1: } \omega t_2 < \omega t < \omega t_3$$

The Ratio of the Amplitude of the Reference signal (V_{r1} or V_{r2} or V_{r3}) to the Amplitude of Carrier signal, V_{car} is The Modulation Index(m) of an inverter.

$$\text{Modulation Index, } m_a = \frac{\text{Amplitude of the Reference signal}}{\text{Amplitude of the Carrier signal}}$$

$$\Rightarrow M_a = {}^{A_m}\!/_{A_c}$$

In above expression, A_m is the peak value of voltage reference signal and A_c means the peak-to-peak value of carrier signal.

Modulation Index (m) of an Inverter should be less than one (1) and greater than Zero (0) i.e $0 < m < 1$.

To get M_a modulation index greater than 0.66, the phase angle displacement is calculated as,

$$\omega t_1 = \sin^{-1}({}^{A_c}\!/_{A_m})$$
$$\omega t_2 = \sin^{-1}({}^{A_c}\!/_{2A_m})$$
$$\omega t_3 = \pi - \omega t_2$$
$$\omega t_4 = \pi - \omega t_1$$

Below fig. describes the switching technique used in this presented Inverter and output voltage amplitude according to device ON & OFF conditions. It also explains the five areas that makes up one partial cycle of the inverter result.

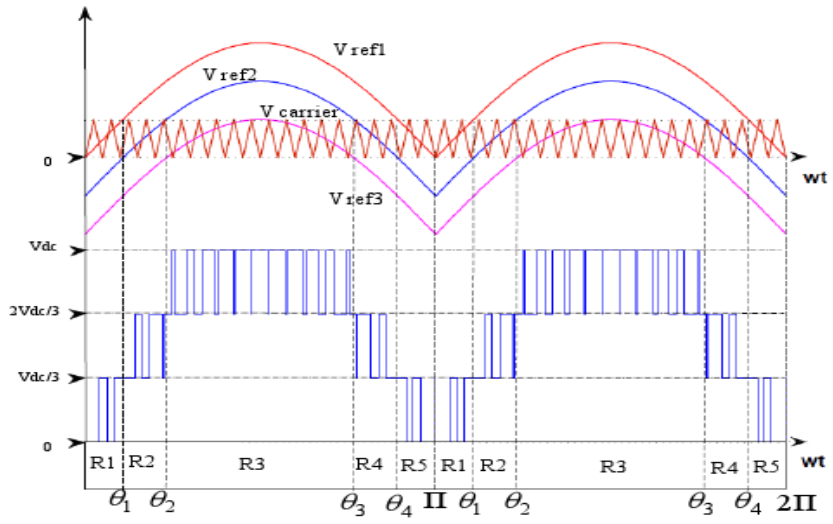

Fig. 3 .From top: PWM switching signal generation, Output of level generator, Output regions for gating signals.

Below fig. describes the output signals given by the pulse width modulation (PWM) technique. In above fig.,

- W_1 represents the resultant signal generated by comparing first reference signal, V_{r1} and carrier Signal, V_{car}.
- W_2 represents the resultant signal generated by comparing second reference signal, V_{r2} and carrier Signal, V_{car}.
- W_3 represents the result ant signal generated by comparing third reference signal, V_{r3} and carrier Signal, V_{car}.

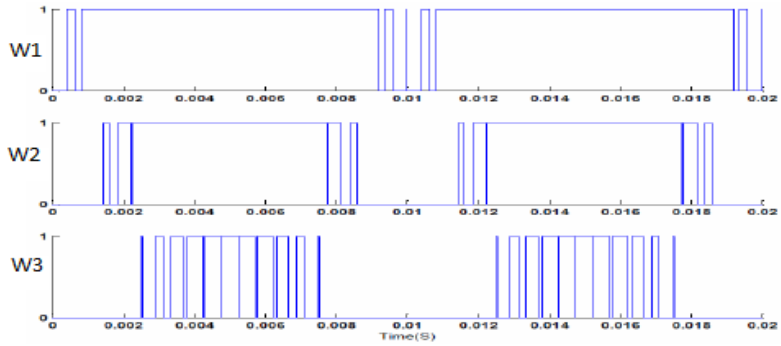

Fig. 4. Decision signals produced by the comparators.

Changing the polarity of inverter output voltage is simple by using gating signal to output polarity generator stage. Normally Low-frequency output polarity generator stage works in two modes:

1. Forward mode and
2. Reverse mode.

Forward mode: In this switching Devices S_7 and S_8 are ON to generate positive polarization output.

Reverse mode: In this switching Devices S_9 and S_{10} are ON to generate negative polarization output.

V SIMULATION RESULTS

MATLAB/SIMULINK software was used to perform/simulate Presented Inverter technique simulations and Pulse Width Modulation (PWM) pattern. To remove the high frequency switching ripples, an LC filter is used and also LC filter is designed in the proper way to remove the high frequency ripples in the same way of tuning filter values as given in [9]. The resonance frequency of an inverter by using this technique is considered to be 30 times the line frequency (50 Hz). As we all know that by comparing three reference signals (V_{r1}, V_{r2} and V_{r3}) with carrier signal i.e triangular signal, gating signals to be generated to the switching Devices. Table III describes the Specifications of the multilevel inverter which is designed and its related parameter,

TABLE III

Specifications of MLI

Parameter	Capacity
DC link voltage V_{dc}	300 Volts
C1-C2-C3	3300µF
Switching frequency	10 kHz
Filter inductor	5mH
Filter capacitor	2µF
Filter damping resistor	2 Ω

Below Fig. describes the response of MLI using present technique with an output filter and with RL series load of 150Ω and 30mH resp.

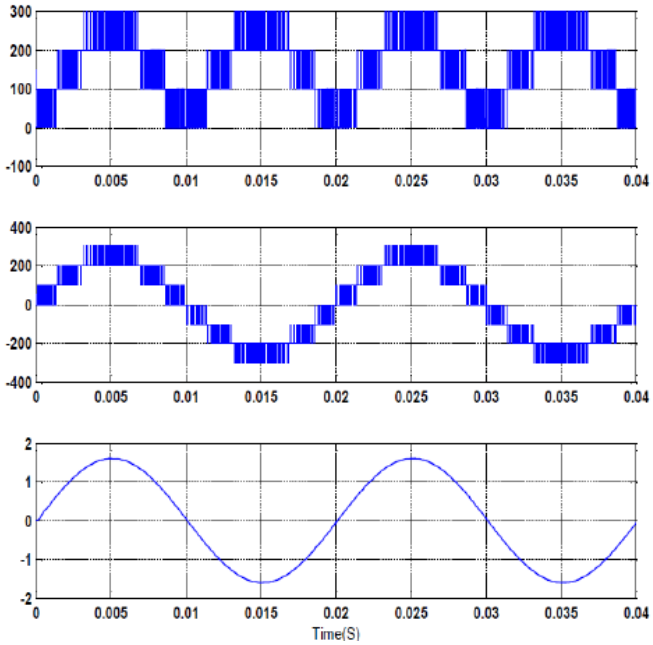

Fig.5. Output voltage of level generator (100 V/div), output voltage (200 V/div) and output current (1 A/div) at M_a=0.8.(From top)

Below fig. represents the generation of output voltage having only five levels for modulation index, M_a in between 0.33 and 0.66 and Current THD waveform for five levels of output voltage at modulation index, M_a in between 0.33 and 0.66. Only Reference signals V_{r1} and V_{r2} are going to compared with the triangular carrier wave which results in the generation of output voltage having only five levels.

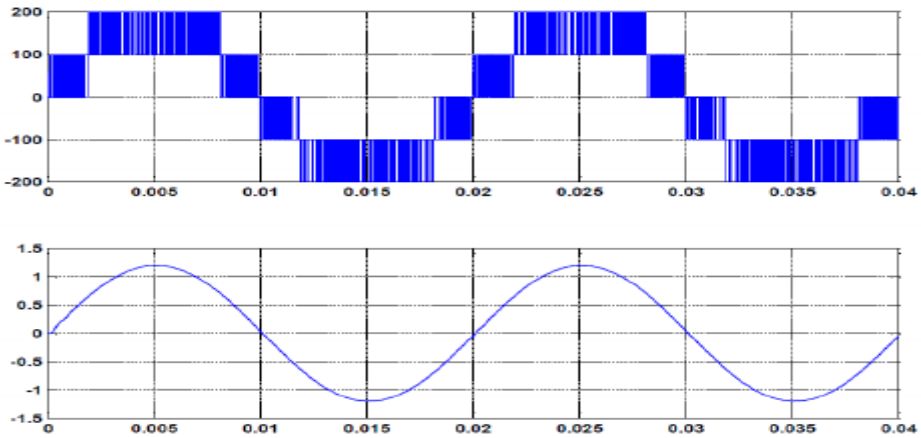

Fig. 6. Output voltage of polarity generator (100 V/div), and output current (0.5 A/div) for Ma=0.6 (From top)

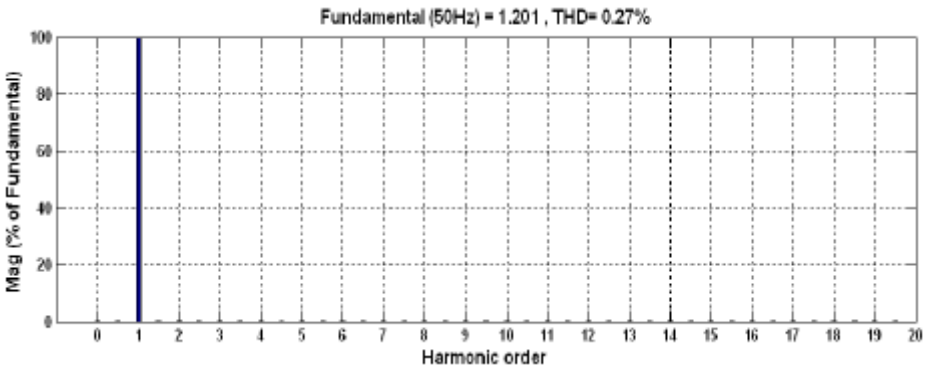

Fig. 7. Current waveform THD for five levels of output voltage of Fig.6.

Below fig. represents the generation of output voltage having only three levels for modulation index, M_a in less than 0.33 and Current THD waveform for three levels of output voltage at modulation index, M_a in less 0.33. Only Reference signals V_{r1} is going to compared with the triangular carrier wave which results in the generation of output voltage having only five levels.

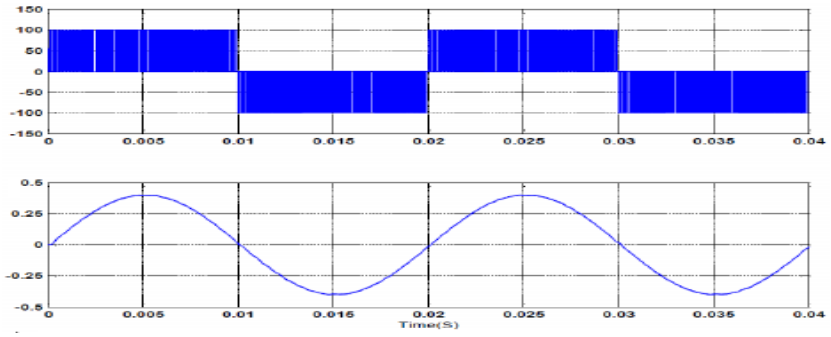

Fig.8. Output voltage of polarity generator (50 V/div), and output current (0.25 A/div) for Ma=0.2.(From top)

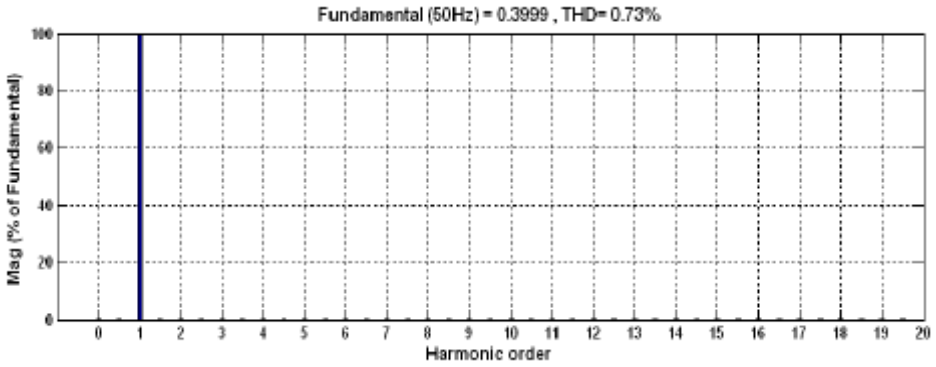

Fig. 9. Current waveform THD for three levels of output voltage of Fig.8

Finally, by observing above results we will decide that the Current THD values for three different modulation index explains that the THD values of the Current reduces with the Increase the number of output voltage levels. Therefore by increasing the number of output voltage levels we will reduce the THD values of the Current.

VI CONCLUSION

By using this inverter technique presented in this paper will enhance the response of the inverter which offers enhanced output responses and lower THD over previous techniques. This technique will reduces the number of switching devices used, manufacturing and maintenance cost, improved reliability and improved control system. The number of power semiconductor switching devices required in this inverter technique is very less. Whereas the number of switching devices to provide path to current for generation of level 2 and level 3 is less results in improved Performance of the inverter, in terms of its efficiency. The complexity of PWM for this inverter technique is very low because it only needs to generate gating pulses for generation of positive level only. In this paper, The inverter generates a 3- level output waveform for modulation index less than 0.33. a 5-level output waveform for modulation index between 0.33-0.66, a 7-level output waveform for modulation index above 0.66, and the results obtained clearly shows the effectiveness of the proposed technique as a multilevel inverter with carriers for PWM and reduced number of switches.

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