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High Speed Implementation of Pulse Shaping FIR Filter Using DA Algorithm

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ABSTRACT

Signal processing ranks among the most demanding applications of digital design concepts. It is a mature technology domain wherein the demands for enhanced performance and reduced resource utilization have risen exponentially over the years. This paper describes an approach to the implementation of digital filter based on field programmable gate arrays (FPGAs) which is flexible and provides performance comparable or superior to traditional approaches, lowpower, area-efficient re-configurable digital signal processing architecture that is tailored for the realization of arbitrary response of Pulse Shaping Finite impulse response (FIR) filters. Pulse shaping is utilized to increase transmission data rate without increasing the bandwidth or bit error rate. In this paper an efficient approach is presented to design and implement a high speed shaping filter using Distributed Arithmetic Algorithm.

Keywords: Digital Filters, FIR, IIR, Pulse Shaping FIR, DA

I. INTRODUCTION

A Filter is frequency selective network, which is used to modify an input signal in order to facilitate further processing. Basically there are two types of filters-analog and digital. Digital Filters are widely used in different areas, because Digital filters have the potential to attain much better signal to noise ratio than analog filters. The digital filter performs noiseless mathematical operations at each intermediate step in the transform and their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters Digital filters operate on numbers opposite to analog filters, which operates on voltages.

The basic operation of digital filter is to take a sequence of input numbers and compute a different sequence of output numbers. There exists a range of different digital filters. FIR and IIR filters are the two common filter forms. A drawback of IIR filters is that the closed-form IIR designs are preliminary limited to low pass, band pass, and high pass filters, etc. secondly FIR filters can have precise linear phase. Also, in the case of FIR filters, closed-form design equations do not exist and the design problem for FIR filters is much more under control than the IIR design problem. A FIR filter is a filter structure that can be used to implement almost any sort of frequency response digitally. It is usually implemented by using a series of delays, multipliers, and adders to create the filter's output. The architecture of FIR filter is shown in

Fig 1

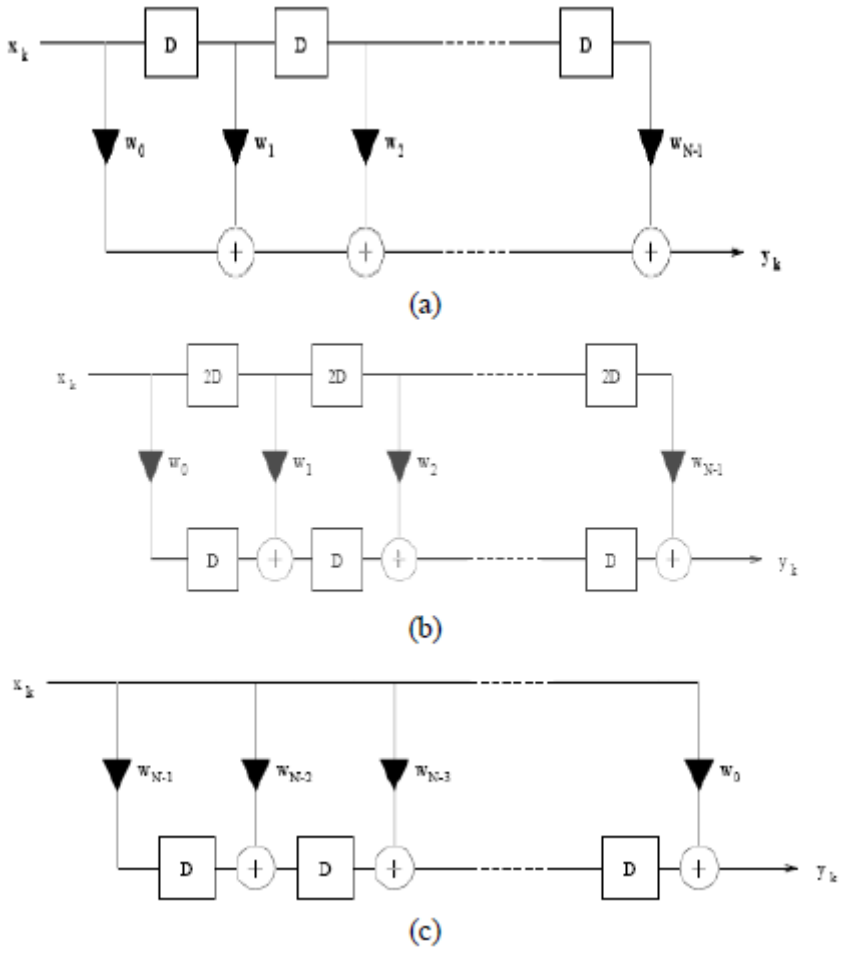

Fig. 1. FIR Filter Architecture (a) canonical form (b) pipelined (c) inverted form.

From this structure the transfer function of canonic form of the filter can be easily described in Z-domain as:

$$H(Z)=w_0+w_1z^{-1}+w_2z^{-2}+\text{------}+w_{M-1}Z^{L-1}$$

In addition the advantages of FIR filter generally we use raised cosine pulse. The rectangular pulse occupies a large bandwidth so an alternative to rectangular pulse is a sinc pulse, which reduces the bandwidth and Inter Symbol Interference. The rectangular pulse is passed through the Root Cosine Filter a set of FIR filters to pulse shape the pulses to sinc [5]. If very high sampling rates are required, full parallel hardware must be used. Such filters can be implemented on FPGAS using combinations of the general purpose logic fabric, on-board RAM and embedded arithmetic hardware. Full-parallel filters cannot share hardware over multiple clock cycles and so tend to occupy large amounts of resource. Hence, efficient implementation of such filters is important to minimize hardware requirement [3].

II FIR FILTER DESIGN TECHNIQUES

FIR filters are particularly useful for applications where exact linear phase response is required. The FIR filter is generally implemented in a non-recursive way, which guarantees a stable filter [2]. FIR filter design essentially consists of two parts:-

A. Approximation Problem

The approximation stage takes the specification and gives a transfer function through four steps. They are as follows:

1) A desired or ideal response is chosen, usually in the frequency domain.

2) An allowed class of filters is chosen (e.g. the length *N* for a FIR filters).

3) A measure of the quality of approximation is chosen.

4) A method or algorithm is selected to find the best filter transfer function.

B. Realization problem

The realization part deals with choosing the structure to implement the transfer function which may be in the form of circuit diagram or in the form of a program. There are essentially three well-known methods for FIR filter design namely:

1) The window method

2) The frequency sampling technique

3) Optimal filter design methods

III. PULSE SHAPING FILTERS

In communications systems, two important requirements of a wireless communications channel demand the use of a pulse shaping filter. The first requirement is generating band limited channels, and the second requirement is reducing Inter Symbol Interference (ISI) arising from multi-path signal reflections.

Both requirements can be accomplished by a pulse shaping filter which is applied to each symbol. Pulse shaping filter are often used in communication transmitters for baseband processing in order to improve the transmission efficiency of a signal spectrum. The pulse shaping filters are widely used in Mobile Phones, HDTV, Space communication, Radar, Audio/data/CD/video system, Speech synthesis recognition, A/D and D/A conversion. The pulses are sent by the transmitter and these are detected by the receiver in any data transmission system. At the receiver, the goal is to sample the received signal at an optimal point in the pulse interval to maximize the probability of an accurate binary decision. This implies that the fundamental shapes of the pulses be such that they do not interfere with one another at the optimal sampling point.

Before digital filters were available, pulse shaping was accomplished with analog filters. There are two criteria that ensures non interference. The first criteria is that the pulse shape exhibits a zero crossing at the sampling

point of all pulse intervals except its own. Otherwise, the residual effect of other pulses will introduce errors into the decision making process and the second criteria is that the shape of the pulses be such that the amplitude decays rapidly outside of the pulse interval [8].The pulse shape used for transmission should have low bandwidth and also have no intersymbol interference (ISI). A sinc function has both these properties and hence can significantly increase spectral efficiency. However a system using a sinc function for pulse shaping is highly susceptible to timing jitter and phase error. This is one of the main drawbacks to be considered while designing practical pulse shaping filters. A rectangular wave filter is not as sensitive to timing jitter but needs a very high bandwidth. The raised cosine filter is commonly used in practical applications as it provides an optimal trade off between spectral efficiency and design complexity.

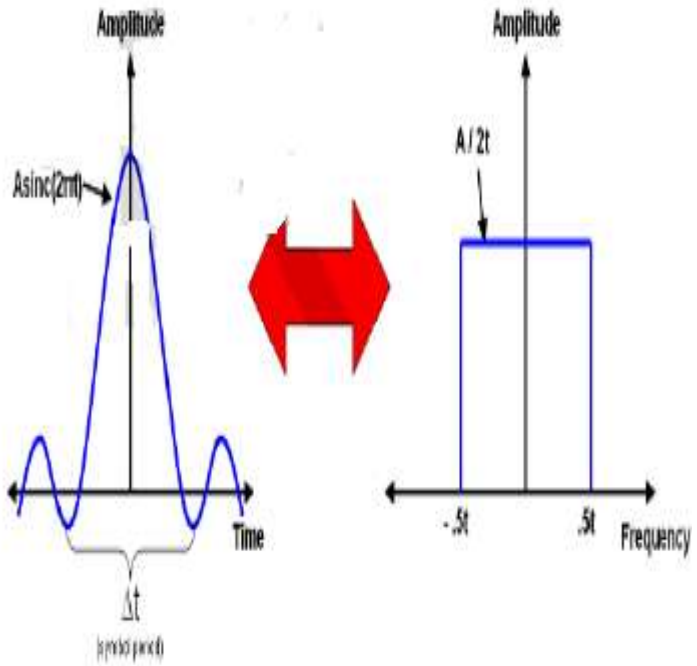

Fig. 2. Sinc Pulse Time & Frequency Response [9]

The sinc pulse is periodic in nature and is has maximum amplitude in the middle of the symbol time. In addition, it appears as a square wave in the frequency domain and thus can effectively limit a communications channel to a specific frequency range. The unbounded frequency response of the rectangular pulse renders it unsuitable for modern transmission systems. This is where pulse shaping filters come into play.

IV. DISTRIBUTED ARITHMETIC (DA)

The convolution sum is given by y=f (h,y)=(from n=0 to N-1)Σh(n)*x(n). In DSP applications, if filter coefficients are known beforehand then partial products of the h (n).x (n) can be calculated. These partial products are stored in ROM as a look up table (LUT) and then accessed by the input samples each bits of which are used as the address for ROM. Coefficients h (n) are constants and inputs x (n) is a variable. Therefore x(n)

can be represented as, x(n)=(from b=0 to B-1)Σxb(n).2b with xb(n)Є(0,1) where xb(n) denotes the bthof x(n) or nth sample of x.. The inner product y can be written as, y= (from n=0 to N-1) Σh (n). (From b=0 to B-1) Σ xb (k) .2b. redistributing the order of summation we get, y=(from b=0 to B-1) Σ 2b*(from n=0 to N-1) Σh(n).xb(n)=(from b=0 to B-1) Σ2b*(from n=0 to N-1) Σf(h(n),xb(n)).

The distributed arithmetic requires 2N word LUT which is pre-programmed to the target device. These partial products are accessed using input vector xb= (xb(0), xb(1),…..xb(N-1)) are weighed by the power of 2 and accumulated. The inner product of y is computed after N look up cycles.

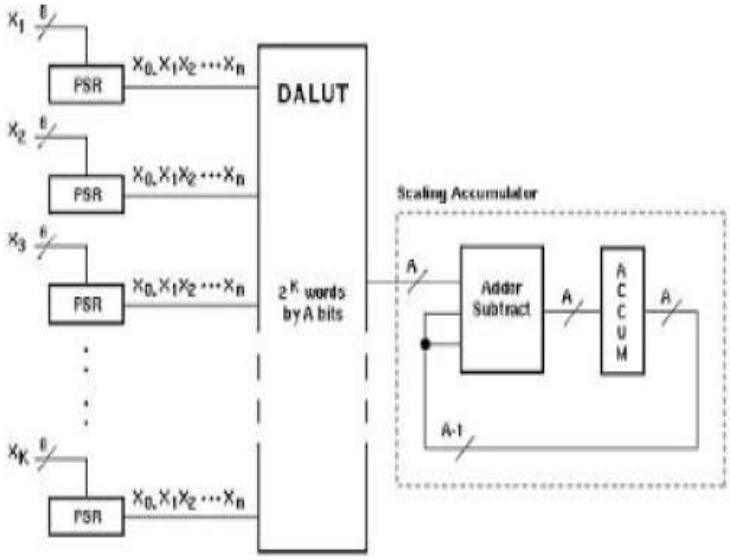

Figure. 3 Bit serial DA architecture

V. RESULTS

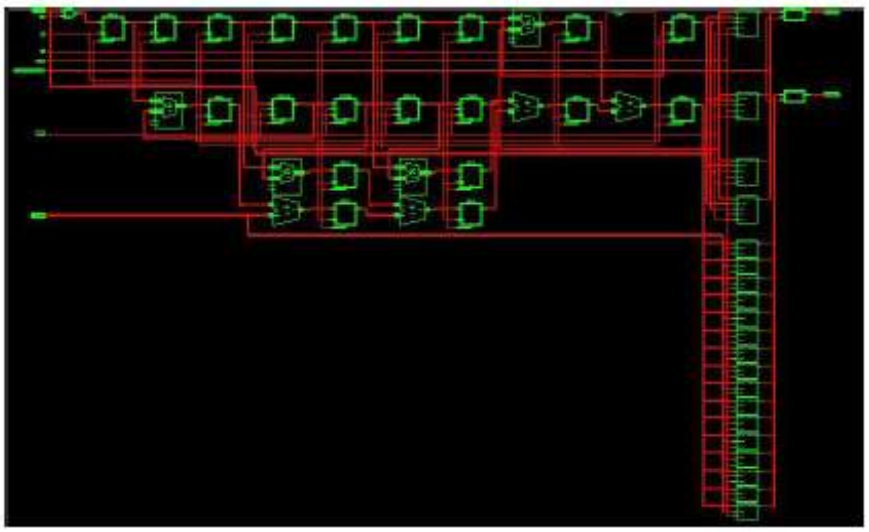

Fig 4. RTL View of FIR Filter

Fig 5. Simulation Result of FIR

VI CONCLUSION

The multiplier less distributed arithmetic (DA)-based technique has gained substantial popularity, Due to its high-throughput processing capability and increased regularity, results in cost-effective and area-time efficient computing structures. By reducing chip count, it improves the overall reliability of the system, provides low area, low power and high-speed implementation of FIR filters. It also reduces filter latency.

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