Performance Evaluation of Modified Booth Encoder using Redundant Binary Representation

B. Priyathamkumar[1], M M Gayatri[2]

[1,2]*Dept. of Electronics and Communication Engineering, Sri Venkateswara College of Engineering and Technology, Srikakulam, AP, (India)*

ABSTRACT

The requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. The work mainly deals with in improving multiplication process by using Redundant Binary Technique. The redundant binary in design of high speed digital multiplier is beneficial due to high modularity and carry free addition. Generally, in high radix modified booth encoding algorithm the partial products are reduced in multiplication process. But it yields complexity in producing in generation of hard multiples. Therefore booth encoding scheme along with redundant binary scheme solves this problem by using booth encoding, RB partial product generator, RB partial product accumulator, RB to NB converter stage. Adders are the key element of the arithmetic unit, especially fast parallel adder. Redundant Binary Signed Digit (RBSD) adders are designed to perform high-speed arithmetic operations. Generally, in a high radix modified Booth encoding algorithm the partial products are reduced in multiplication process. Due to its high modularity and carry-free addition, a redundant binary (RB) representation can be used when designing high performance multipliers. The conventional RB multiplier requires an additional RB partial product (RBPP) row, because an error-correcting word (ECW) is generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding.

Keywords: Redundant Binary, Modified Booth Encoding, RB Partial Product Generator, RB Multiplier.

I. INTRODUCTION

The nature of the work is introduced to improve the speed of the multiplier and to remove the hard multiples and to reduce the partial products than previous work. By improving the multipliers in the ALU processors from past to present they are giving better results comparing to previous improvements. So, now introducing the Redundant Binary Representation technique in digital multipliers to overcome drawbacks in previous techniques. Redundant Binary (RB) representations first introduced by Avizienis in 1961 for fast parallel arithmetic. This new Arithmetic was applied for fast Multiplication by takagi and implemented by Edamatsu. Multiplication is a most commonly used operation in many computing systems. Infact multiplication is nothing but addition since, multiplicand adds to itself multiplier number of times gives the multiplication value between multiplier and multiplicand. But considering the fact that this kind of implementation really takes huge hardware resources and the circuit operates at utterly low speed. In order to address this so many ideas have been presented so far for the last three decades. Each one is aimed at particular improvement according to the requirement.

One may be aimed at high clock speeds and another maybe aimed for low power or less area occupation. Either way ultimate job is to come up with an efficient architecture which can address three constraints of VLSI speed, area, and power. Among these three speeds is the one which requires special attention. If we observe closely multiplication operation involves two steps one is producing partial products and adding these partial products. Thus, the speed of a multiplier hardly depends on how fast generate the partial products and how fast we can add them together. If the numbers of partial products to be generated are of less than it is indirectly means that we have achieved the speed in generating partial products. Booth's algorithms are meant for this only. To speed up the addition among the partial products we need fast adder architectures. Since the multipliers have a significant impact on the performance of the entire system, many high performance algorithms and architectures have been proposed.

II.NUMBER SYSTEM REPRESENTATIONS

In computing signed digit number representation is required to encode negative numbers in binary number systems. In mathematics, negative numbers in any base are represented by prefixing them with a–sign. However, in computer hardware, numbers are represented in binary only without extra symbols, requiring a method of encoding the minus sign. The signed digit number representation makes it possible to perform addition without carry propagation chains that are used to speed up arithmetic operations

A. Redundant Signed Digit-Carry-Free Addition Algorithm

A symmetrical signed digit (SD) number can assume the following values i.e. [−α,..-1,0,1….α]. Where the maximum value of α must be within the following range:

$$[(r-1)/2] \leq \alpha \leq r - 1$$

In order to yield minimum redundancy, one can choose the maximum magnitude α = [r/2]. If r = 2, then number representation is known as Redundant Binary Signed Digit (RBSD) number system. A digit set need not be the standard. Radix-r, a digit set [–k, μ], having the condition k + μ + 1≥r may be Converted to a radix-r digit set[α, β], for α + β + 1 ≥γ. The redundancy δof the number system is defined asδ = α + β + 1 −γ. In the binary signed digit number system, each digit can assume any one of three values {-1, 0, 1}. As a result redundancy is introduced in a system i.e. a number can be represented in more than one way. Due to the presence of redundancy one can perform carry-propagation free addition and hence parallel addition of two redundant numbers can be performed in a constant time independent of the word length of operands.

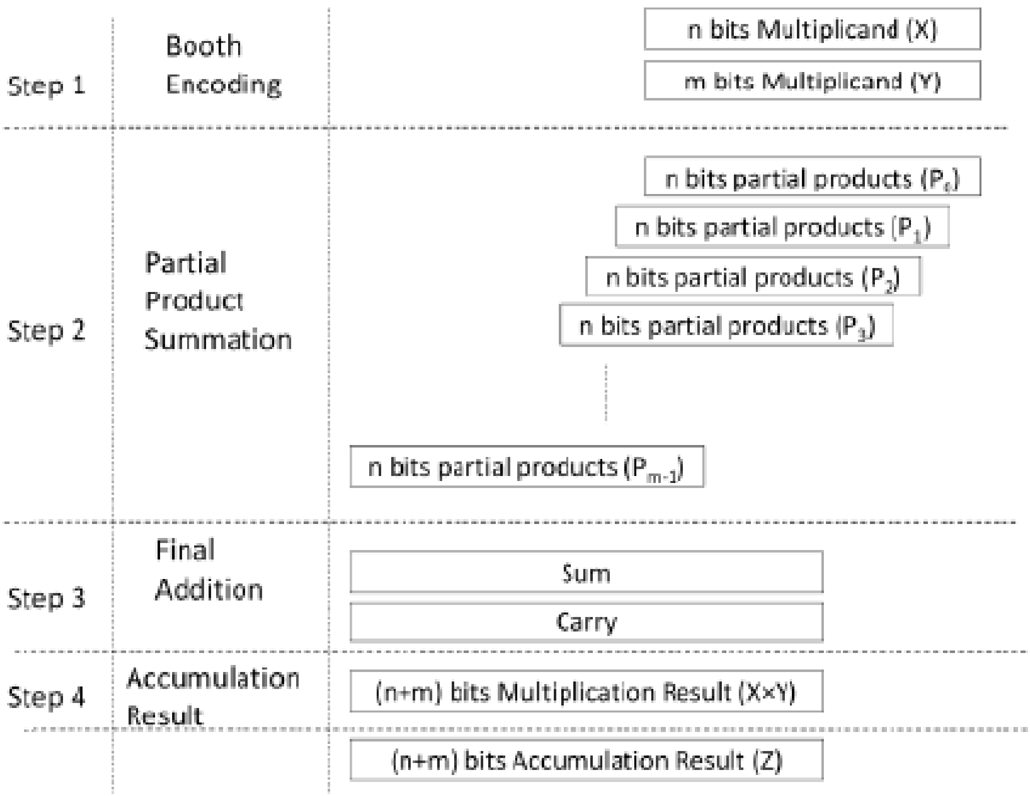

Fig 1. Basic Arithmetic steps of Multiplication and Accumulation.

III. ALGORITHM OF THE MULTIPLIER

A. Radix - 4

Modified Booth Encoding (Radix-4) can effectively be applied to reduce the number of partial product rows to half in parallel multipliers. This is performed by grouping three adjacent multiplier bits (B = bn-1 bn-2…b0) to select one of the signed multiples as shown in Table I. The side bits of each group are overlapped with the two adjacent groups. The lastbit in each group is referred as reference bit. The first group is coded by adding "0" as reference bit prior to least significant bit position i.e., (b1, b0, 0).Depending on these select signals, the partial product rows are generated by selecting one of the combination {-2A,-A, 0, A, 2A} of the multiplicand (A = an-1an-2…a0). The twice of multiplicand (2A) in Table I is obtained by left shifting the multiplicand by one bit position and negation operation is achieved by inverting each bit of multiplicand (i.e. one's complement) and adding "1" to its least significant bit position.

TABLE I: Modified Booth's Encoding Unit For Radix 4

x_{i+1}	x_i	x_{i-1}	Y	Comments
0	0	0	0	String of Zeros
0	0	1	1.A	End of 1's
0	1	0	1.A	A single 1
0	1	1	2.A	End of 1's
1	0	0	-2.A	Beginning of 1's
1	0	1	-1.A	A single 0
1	1	0	-1.A	Beginning of 1's
1	1	1	0	String of ones

B. Radix 8

Radix-8 Booth recoding applies the same algorithm as that of Radix-4, but now we take quartets of bits instead of triplets. Each quartet is codified as a signed digit using Table III. Radix-8 algorithm reduces the number of partial products to n/3, where n is the number of multiplier bits. Thus it allows a time gain in the partial products summation.

Multiplier Bits				Recoded Operation on multiplicand, X
Y_{i+2}	Y_{i+1}	Y_i	Y_{i-1}	
0	0	0	0	0X
0	0	0	1	+X
0	0	1	0	+X
0	0	1	1	+2X
0	1	0	0	+2X
0	1	0	1	+3X
0	1	1	0	+3X
0	1	1	1	+4X
1	0	0	0	-4X
1	0	0	1	-3X
1	0	1	0	-3X
1	0	1	1	-2X
1	1	0	0	-2X
1	1	0	1	-1X
1	1	1	0	-1X
1	1	1	1	0X

Sign Extension Corrector: Sign Extension Corrector is designed to enhance the ability of the booth multiplier to multiply not only the unsigned number but as well as the signed number. The working principle of sign extension that converts signed multiplier signed unsigned multiplier as follows. One bit control signal called signed-unsigned(s_u) bit is used to indicate whether the multiplication operation is signed number or unsigned number .when sign-unsign s_u=0, it indicates unsigned number multiplication and when s_u=1, it indicates signed number multiplication.

Partial Product Generator: A product formed by multiplying the multiplicand by one digit of the multiplier when the multiplier has more than one digit. Partial products are used as intermediate steps in calculating larger products. Partial product generator is designed to produce the product by multiplying the multiplicand A by 0, 1, -1, 2, -2,-3,-4, 3, 4. For product generator, multiply by zero means the multiplicand is multiplied by "0".Multiply by "1" means the product still remains the same as the multiplicand value. Multiply by "-1" means that the product is the two's complement form of the number. Multiply by "-2" is to shift left one bit the two's complement of the multiplicand value and multiply by "2" means just shift left the multiplicand by one place. . Multiply by "-4" is to shift left two bit the two's complement of the multiplicand value and multiply by "2" means just shift left the multiplicand by two place. Here we have an odd multiple of the multiplicand, 3Y, which is not immediately available. To generate it we need to perform this previous add: 2Y+Y=3Y. But we are designing a multiplier for specific purpose and thereby the multiplicand belongs to a previously known set of numbers which are stored in a memory chip. We have tried to take advantage of this fact, to ease the bottleneck of the radix-8 architecture, that is, the generation of 3Y. In this manner we try to attain a better overall multiplication time, or at least comparable to the time we could obtain using radix-4 architecture (with the additional advantage of using a less number of transistors). To generate 3Y with 8-bit words we only have to add 2Y+Y, that is, to add the number with the same number shifted one position to the left.

IV.DESIGN OF 32 BIT REDUNDANT BINARY MULTIPLIER

The Redundant Binary Representation Technique will eliminate the hard multiples generation problem by increasing the radix values.

A. Design of 32x32 based RB multiplier

The block diagram of 32*32 consists of 3 stages:

- Booth encoder and partial product generator stage (BEPPG stage)
- Redundant binary adder summing tree stage (RBA summing stage)
- Redundant binary to NB conversion stage (RB-to-NB stage)

Step 1: Booth Encoder and Partial Product Generator stage (BEPPG stage): Booth encoder and partial product generator affect the efficiency of the partial product generation. The number of partial products that can be saved by this stage impacts the cost, performance, and power consumption of the RB summing tree and the multiplier as a whole. In the first stage, 16 CRBBE-4 slices are used to generate the control signals from the multiplier. The hard multiple 5X is generated. The multiplicand bits are shifted and selected into 16 rows of RB partial products in 16 slices of RBPPG.

Step 2: Redundant Binary Adder summing tree stage (RBA summing stage): Here all the partial products generate 128 bits. These bits are added by the Redundant Binary Adders (RBA)denoted as1, 2, 3, 4. RBA had divided into sub blocks with 128 bits.

Step 3: Redundant binary to NB conversion stage (RB-to- NB stage): An RB-to-NB converter converts the final accumulation result to NB representation. Due to the unequal delay profile of the final RB result bits, the conversion can be carried out in uneven groups of consecutive digits according to their arrival time. The carry generation of the next group of digits can be evaluated with a carry-look ahead adder as they do not depend on the final summation results in the RBA tree stage as shown in Figs.2 and 3.

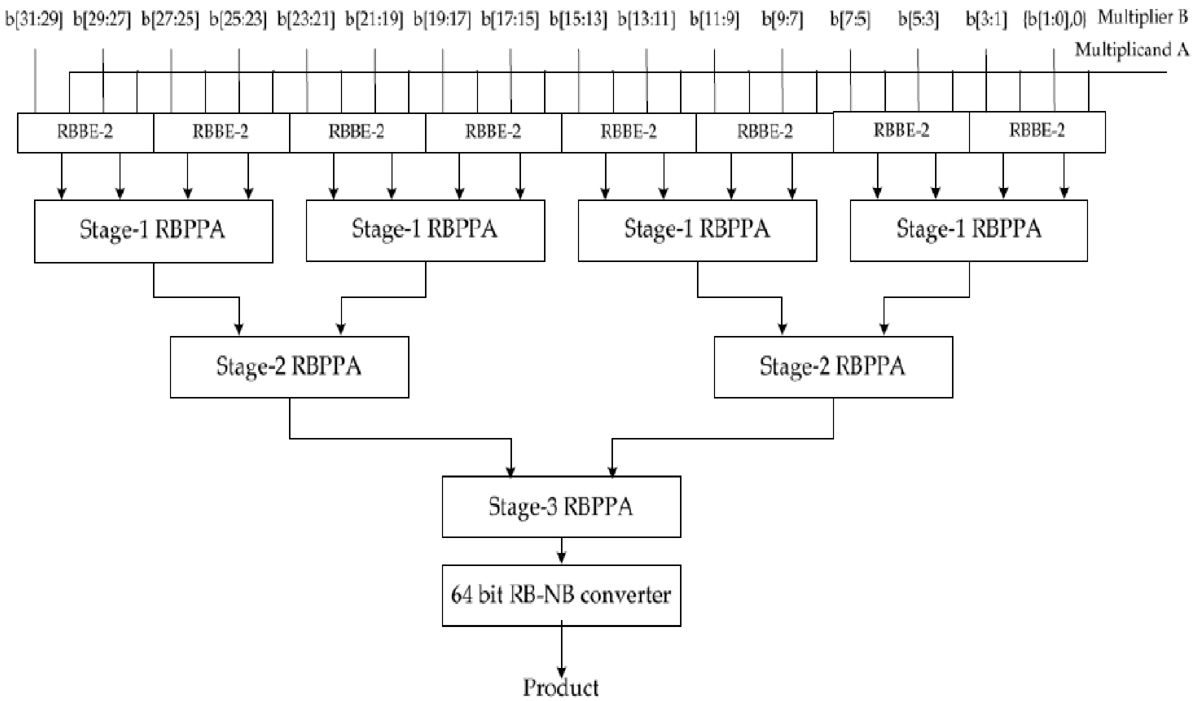

Fig 2. The block diagram of a 32-bit RB multiplier using the proposed RBMPPG-2.

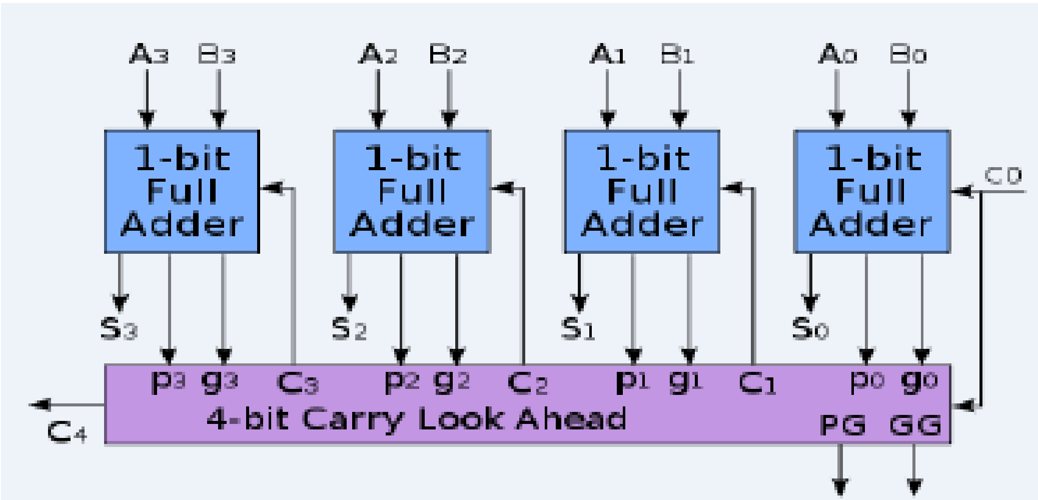

Fig 3. 4-Bit carrylook-ahead adder.

V.SIMULATION RESULTS

This paper presents a high performance 32x32 bit. Redundant binary multiplier with modified redundant binary partial product generator, RB summing tree, and 32 RB to NB Converter. Multiplier designs are synthesized using Xilinx ISE 14.3 targeting a Xilinx Spartan 3 device using randomly generated input patterns. Top View module, RTL Schematic View are mentioned Fig. 4 and Design Summary report of designed multiplier are given in Fig.5 and Fig 6.

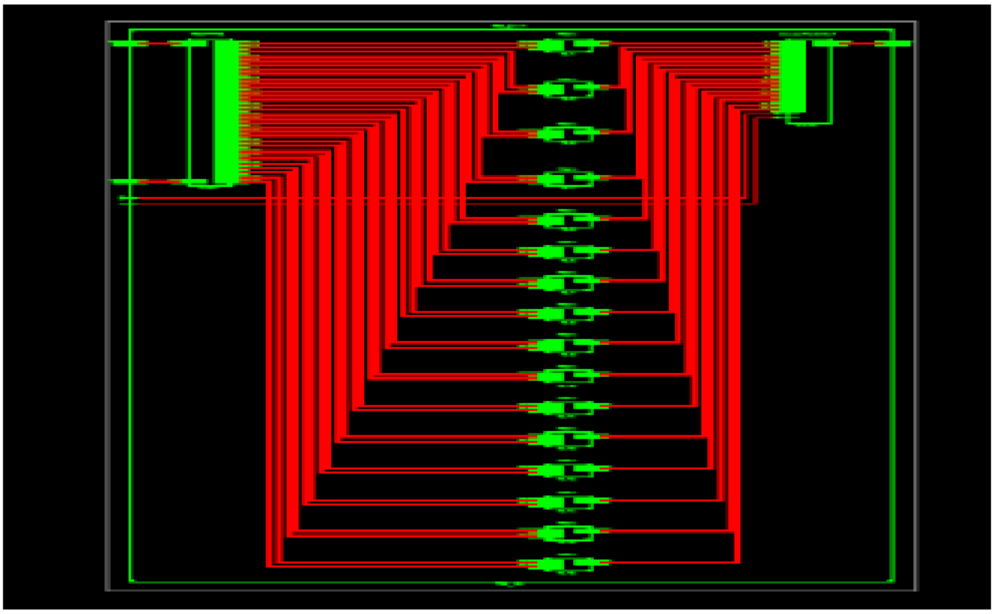

Fig 4. RTL schematic

radix_8 Project Status (04/10/2017 - 15:51:45)			
Project File:	RB_64x64.xise	Parser Errors:	No Errors
Module Name:	RB_64	Implementation State:	Synthesized
Target Device:	xc7vx330t-3ffg1157	• Errors:	No Errors
Product Version:	ISE 14.3	• Warnings:	1 Warning (1 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	7583	204000	3%
Number of fully used LUT-FF pairs	0	7583	0%
Number of bonded IOBs	258	600	43%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig 5. Design Summary Report.

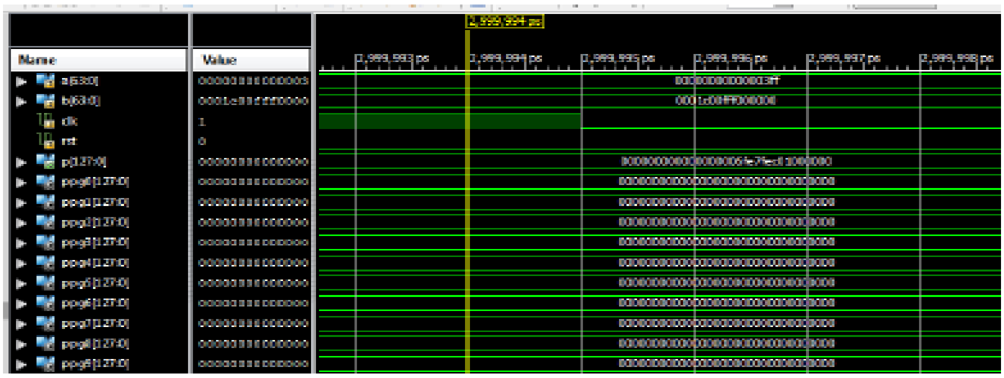

Fig 6. simulation results.

Fig 7. Array Multiplier output

Fig 8. 32 Bit Booth Radix output

We have used Spartan-3 FPGA kit to show the output of the proposed work. The above shown are the results obtained for 32-bit multiplication on Spartan-3.

VI. CONCLUSION

The high performance 32x32 bit RB multiplier architecture has been designed in this paper, by considering a tradeoff between area, power and delay. The RBR technique removes hard multiples and reduces the partial products. By removing hard multiples in the Digital multiplier of the processor, Digital multiplier will perform much faster than existing method. Hence speed of the processor has been increased and it is used for higher multiplications by proposed method. The power delay factor has been reduced to 32 % from 59% when compared with existing approach. In future RBR technique is used for Digital Signal Processing, Fast Fourier Transformations and multimedia applications.

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B Priyathamkumar pursuing his M.Tech in the department of Electronics and Communication Engineering (VLSI), Sri Venkateswara College of Engineering & Technology, Etcherla, Srikakulam, A.P., India. Affiliated to Jawaharlal Nehru Technological University, Kakinada. Approved by AICTE, NEW DELHI. He obtained his B.Tech(ECE) from AITAM College, Tekkali.

M M Gayatri working as Assistant Professor, in the Department of Electronics and Communication Engineering(VLSI), Sri Venkateswara College of Engineering & Technology, Etcherla, Srikakulam. She obtained her M.Tech from AITAM College, Tekkali. Her area of interest is VLSI design and embedded systems.