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DESIGN OF HIGH SPEED 32 BIT UNSIGNED MULTIPLIER USING CLAA AND CSLA

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ABSTRACT

In computational circuits the adders plays a key role in arithmetic operations. Adders like Ripple carry adder, Carry look ahead adder, Carry select adder, Carry skip adder and carry save adder etc. The aim is to develop area efficient, high speed and low power devices. Accurate operation of a digital system is mainly influenced by the performance of the adders. Multipliers are also very important component in digital systems. In this paper, a high performance and low power 32bit unsigned multiplier is proposed using adders. The design of 32bit unsigned multiplier using CLAA and 32bit unsigned multiplier using CSLA multiplies and gives the product term of 64bit. The CLAA based multiplier and CSLA based multiplier uses the same delay for multiplication operation. These two 32-bit unsigned multipliers are simulated using using Xilinx tool.

Keywords:Ripple carry adder, Carry look ahead adder (CLAA), Carry select adder (CSLA), Unsigned Multiplier

I.INTRODUCTION

The design of low power, low area and high performance logic systems are most essential in VLSI system design. The digital systems such as embedded systems, Digital signal processing (DSP), Data process unit and Communication network the arithmetic operations like addition, subtraction; multiplication and division are mostly used and plays a key role in various applications. In electronics, the adder is a digital circuit. The adder can be used to perform the addition of binary numbers. In many computers and different type of processors and controllers, adders are not only used in the arithmetic logic unit and not only perform the addition operation. They are used to calculate addresses, registers and different type of operations. Multiplication is one of the basic arithmetic operations. Multiplication operation is also called as a adding and shifting method. Multiplication operation involves two methods one is Generation of partial products and another one is summation. The speed of multiplication is mainly depends on the Partial product generation and/or summation. The multiplication speed will be high when the generation of partial products are less. In this, we are going to implement the Two 32-bit unsigned multipliers using adders. . In many processors Carry select adder is used to perform the fast arithmetic operations. The carry propagation delay time is very high in Ripple carry adder. To overcome this problem Carry look ahead adder is proposed. This type of adder does not require the carry propagation step by step. The CLAA and CSLA adders have the similarity properties. For the multiplication process the both

adders (CLAA & CSLA) will have the nearly same delay speed. Here The Two 32-bit unsigned multipliers multiplies (N*N) and gives the 64 bit (2N) output.

II.ADDERS

In electronics, an adder is digital circuit which is used to perform the addition of binary digits. In vlsi system design using adders we are increasing the performance of the module. In this section we will review the different types of adders and their characteristics and performance.

A. Half adder

The half adder adds two binary inputs a,b and its have the two binary outputs Sum and carry. The logic diagram of half adder is shown in below figure1.

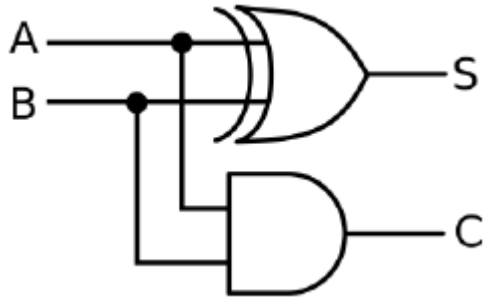

Figure 1 Half adder logic diagram

B. Full adder

The full adder adds three binary inputs a,b,cin and its have the two binary outputs Sum and Carry. The logic diagram of full adder as shown in figure 2.

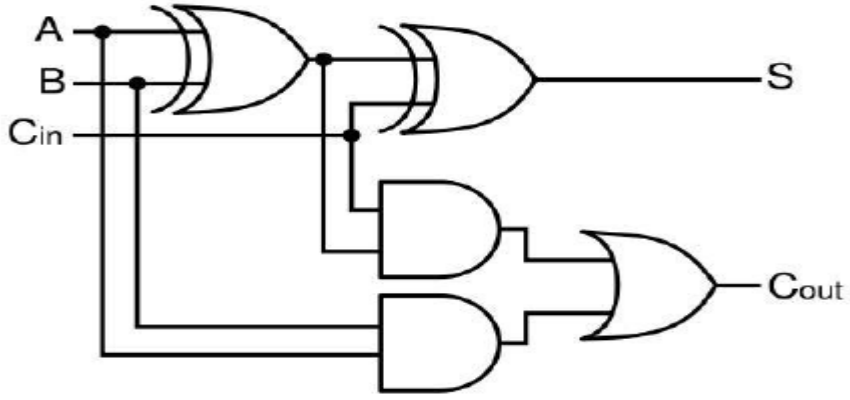

Figure 2 Full adder logic design

C. Ripple Carry Adders:

The well known adder architecture, ripple carry adder is composed of cascaded full adders for n-bit adder, as shown in figure.3 .It is constructed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder it requires n full adders.

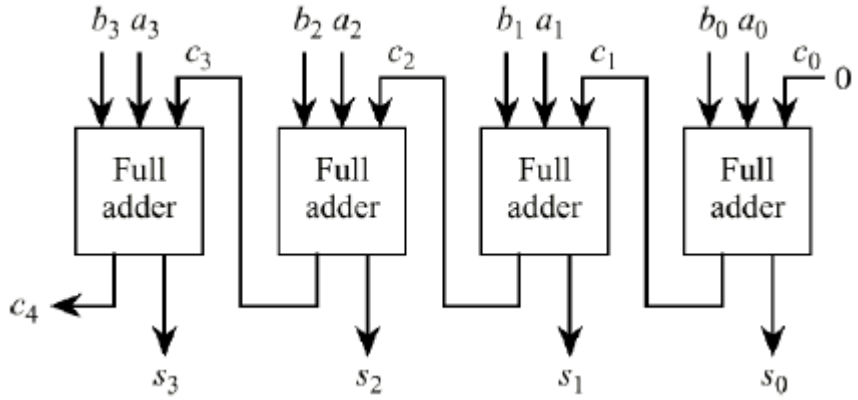

Figure 3 Ripple Carry Adder

Disadvantages:

- Not very efficient when large number bit numbers are used.
- Delay increases linearly with bit length.

III.CARRY SELECT ADDERS

In Carry select adder scheme, blocks of bits are added in two ways: one assuming a carry-in of 0 and the other with a carry-in of 1.This results in two recomputed sum and carry-out signal pairs (s0i-1:k , c0i ; s1i-1:k , c1i) , later as the block's true carry-in (ck) becomes known , the correct signal pairs are selected. Generally multiplexers are used to propagate carries.

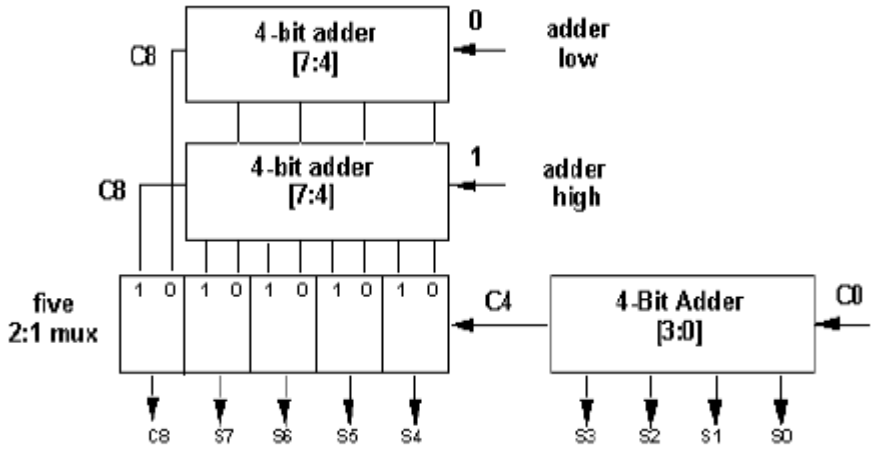

Figure 4 Carry Select Adders

Because of multiplexers larger area is required.

- Have a lesser delay than Ripple Carry Adders (half delay of RCA).
- Hence we always go for Carry Select Adder while working with smaller no of bits.

IV. CARRY LOOK AHEAD ADDERS

Carry Look Ahead Adder can produce carries faster due to carry bits generated in parallel by an additional circuitry whenever inputs change. This technique uses carry bypass logic to speed up the carry propagation.

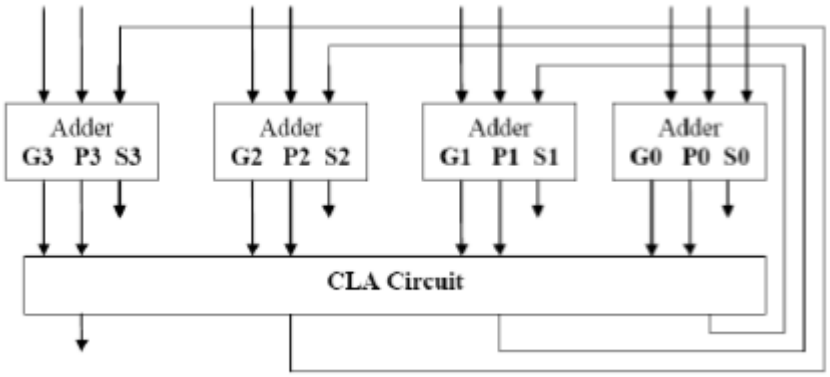

Figure 5 4-Bit CLA Logic equations

Let **ai** and **bi** be the augends and addend inputs, **ci** the carry input, **si** and **ci+1** , the sum and carry-out to the **ith** bit position. If the auxiliary functions, **pi** and **gi** called the propagate and generate signals, the sum output respectively are defined as follows. pi = ai + bi gi = ai bi si = ai **xor** bi **xor** ci c**i+1** = gi + pici .

- As we increase the no of bits in the Carry Look Ahead adders, the complexity increases because the no. of gates in the expression **Ci+1** increases. So practically its not desirable to use the traditional CLA shown above because it increase the Space required and the power too.

Instead we will use here Carry Look Ahead adder (less bits) in levels to create a larger CLA. Commonly smaller CLA may be taken as a 4-bit CLA. So we can define **carry look ahead** over a group of 4 bits. Hence

now we redefine terms **carry generate** as [**Group Generated Carry**] **g[i,i+3]** and **carry propagate** as [**Group Propagated Carry**] p**[i,i+3]** which are defined below.

V.MULTIPLIER FOR UNSIGNED DATA

Multiplication involves the generation of partial products, one for each digit in the multiplier, as in Figure3.These partial products are then summed to produce the final product. The multiplication of two n-bit binary integers results in a product of up to 2n bits in length [2].

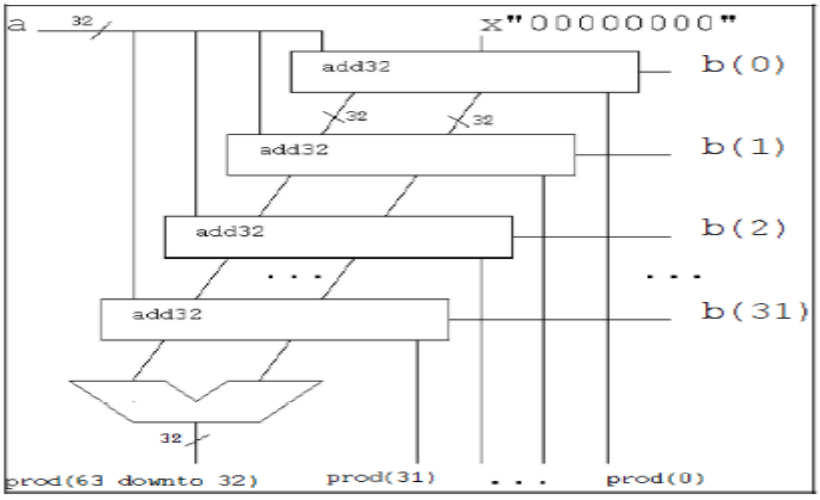

Figure 6. A partial schematic of the multiplier

We used the following algorithm to implement the multiplication operation for unsigned data.

VI.MULTIPLICATION ALGORITHM

Let the product register size be 64 bits. Let the multiplicand registers size be 32 bits. Store the multiplier in the least significant half of the product register. Clear the most significant half of the product register. Repeat the following steps for 32 times: 1. If the least significant bit of the product register is "1" then add the multiplicand to the most significant half of the product register. 2. Shift the content of the product register one bit to the right (ignore the shifted-out bit.). 3. Shift-in the carry bit into the most significant bit of the product register. Figure 7.Shows a block diagram for such a multiplier [2].

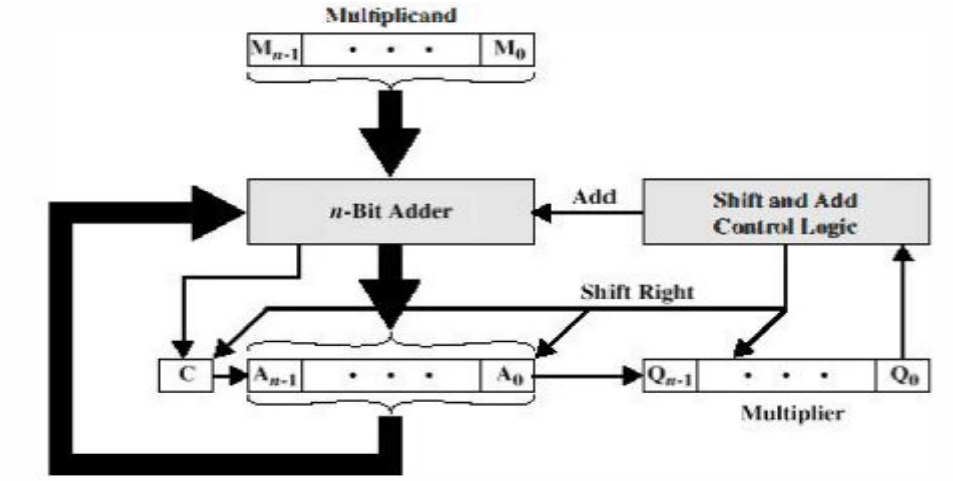

Figure7. Multiplier of two n-bit values.

VII.SIMULATION RESULTS

Codes for Multiplier and MCSLA are successfully verified by the simulation. Error conditions are intentionally made in the coding to check the complete functionality. Obtained

utilization summery and simulated output is shown below Figure 8. This adder can be used for the construction of add and shift multiplier which have lowest area, high speed and minimum power consumption.

Figure 8: RTL Diagram Multiplier

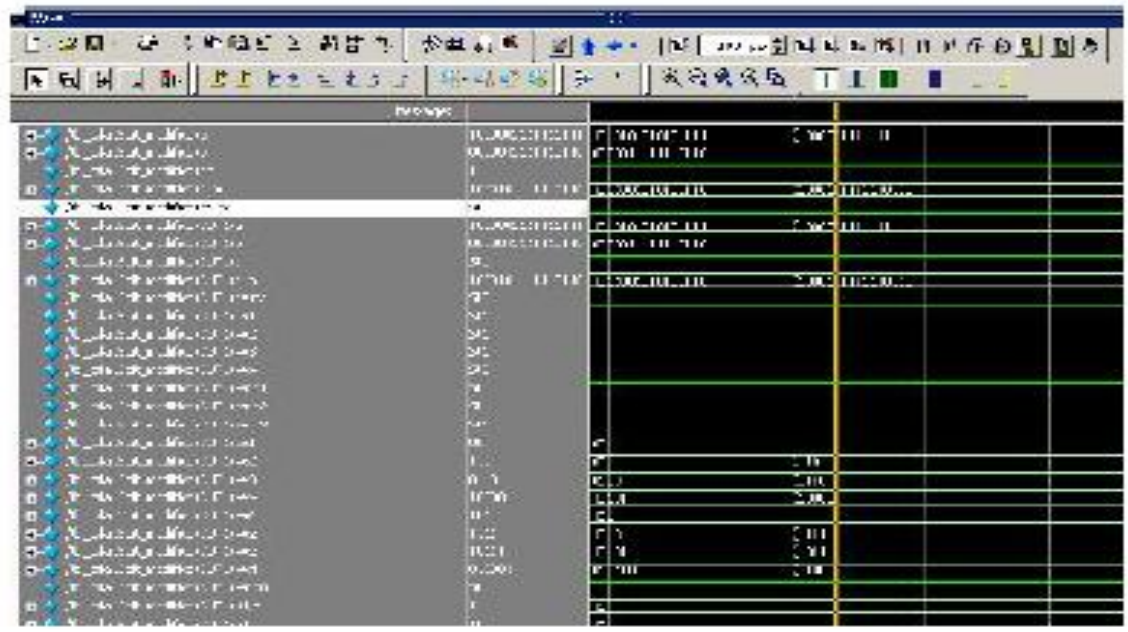

Figure 9. Simulated output of CSLA

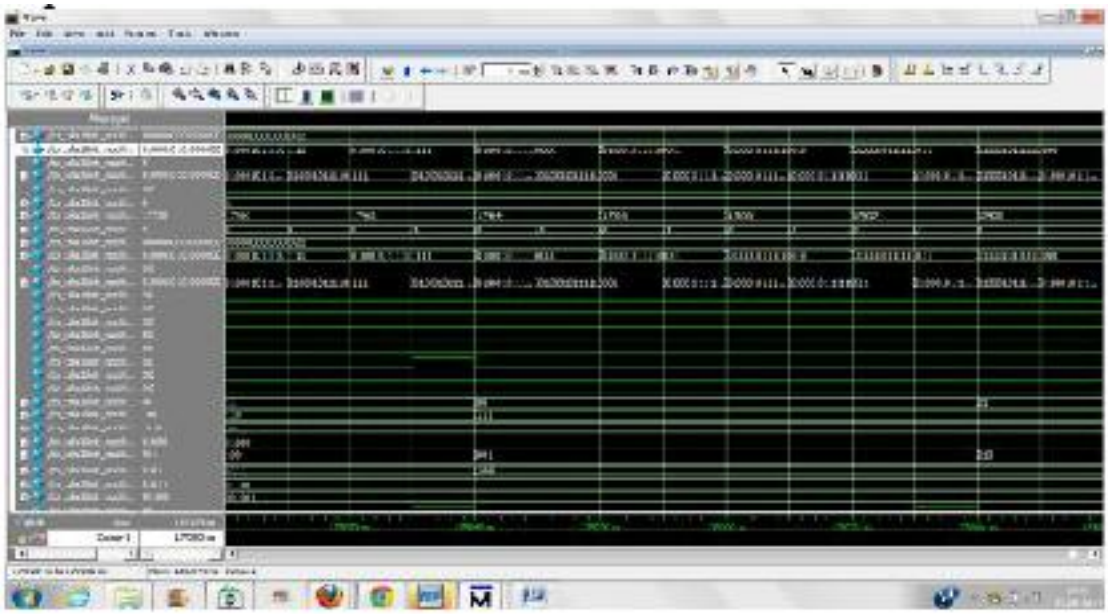

Figure 10. Simulation Output of Multiplier

VIIICONCLUSION

A design and implementation of a VHDL-based 32- bit unsigned multiplier with CLAA and CSLA was presented. VHDL, a Very High Speed Integrated Circuit Hardware Description Language, was used to model and simulate our multiplier. Using CSLA improves the overall
performance of the multiplier.

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