6th International Conference on Recent Development in Engineering Science, Humanities and Management
National Institute of Technical Teachers Training & Research, Chandigarh, India (ESHM-17)
14th May 2017, www.conferenceworld.in ISBN: 978-93-86171-36-8

NOISE PARAMETER EXTRACTION FOR SYMMETRIC DUAL MATERIAL GATE ALGAN/GAN MODFET FOR LNA DESIGN

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ABSTRACT

This article proposes noise parameter extraction and simulation for enhanced field plated Dual Material Gate AlGaN/GaN MODFET first time in order to characterize the device for its noise performance in the microwave range of frequencies. Noise equivalent circuit model based on small signal model of the proposed device structure is developed for parameter extraction and simulation. On the basis van der Ziel and Pucel model the proposed device structure is investigated for noise figure, noise resistance, magnitude of source reflection coefficient and angle of source reflection coefficient. Gate and drain noise current sources and their correlation coefficient is studied as part of small signal intrinsic elements of equivalent noise circuit model. Device ambient temperature is taken into account for extraction of parasitic elements. After de-embedding parasitic elements intrinsic elements of noise equivalent circuit model are extracted. TCAD simulation of device noise figure, noise resistance, magnitude and angle of source reflection coefficient is also performed using Silvaco TCAD device simulator. Extracted noise equivalent circuit model result and noise performance metrics are validated with simulated and experimental results and found in good agreement thus assuring extraction accuracy for noise parameters for the device.

Key words: Analysis of noise figure, small signal parameter, GaN HEMT, low noise amplifier design

I. INTRODUCTION

GaN based modulation doped field effect transistors are well known devices for excellent high power, high temperature microwave performance in LNA. Compound semiconductor based devices are generally preferred over conventional semiconductor devices due to their high speed of operation, high current densities and high efficiencies at microwave range of operation [1] [2] [3] [4]. It is important to note that GaN device based low-noise amplifier may also eliminate the requirement of dedicated protection circuitry used in the receiver systems [5]. Long back intrinsic and extrinsic noise performance of the GaN MODFETs was studied by [6], whereby it was concluded that the device resistances are main cause limiting the noise performance of device operating in microwave range. A surface potential based modeling done by [7] to develop compact noise model. The previous works by Van der Ziel [8], Pucel [9], Fukui, and Pospieszalski [10] and other scientists [11] [12] [13]

ISBN: 978-93-86171-36-8

have been studied in order to consider suitability of model for noise analysis for DMG AlGaN/GaN MODFET structure We found Van der Ziel and Pucel Model (also called PRC model) most appropriate for analysis of our proposed DMG MODFET noise performance. These models consider correlation between gate noise and drain noise which is important for MODFETs analysis. Contribution in noise figure by various intrinsic and extrinsic device elements is also analyzed accurately in this article.

II.MODEL FORMULATION

1.1 Device structure: Enhanced device structure based on [14] of DMG AlGaN/GaN MODFET incorporating field plate to obtain better field distribution and performance of device is shown in Fig.1 (a). This unique device structure has dual material gate engineering having two metal based gate regions of different work functions that results in suppressing of short channel effects (SCE). Gate forms Skottky contact with unintentionally doped $Al_{0.3}Ga_{0.7}N$ cap layer followed by n-$Al_{0.3}Ga_{0.7}N$ barrier-layer, a UID $Al_{0.3}Ga_{0.7}N$ spacer layer and GaN channel layer. These all layers are placed over sapphire substrate that is capable to with stand higher operating temperature of device. Two dimensional electron gas (2-DEG) based channel is formed at the interface of spacer and GaN layer that provides higher operation speed to device comparatively to conventional inversion layer based devices. Device dimensions and parameters values are depicted in the figure for various parts of device structure. ϕ_{M1} and ϕ_{M2} represent work function of each gate metal region as shown in device schematic diagram.

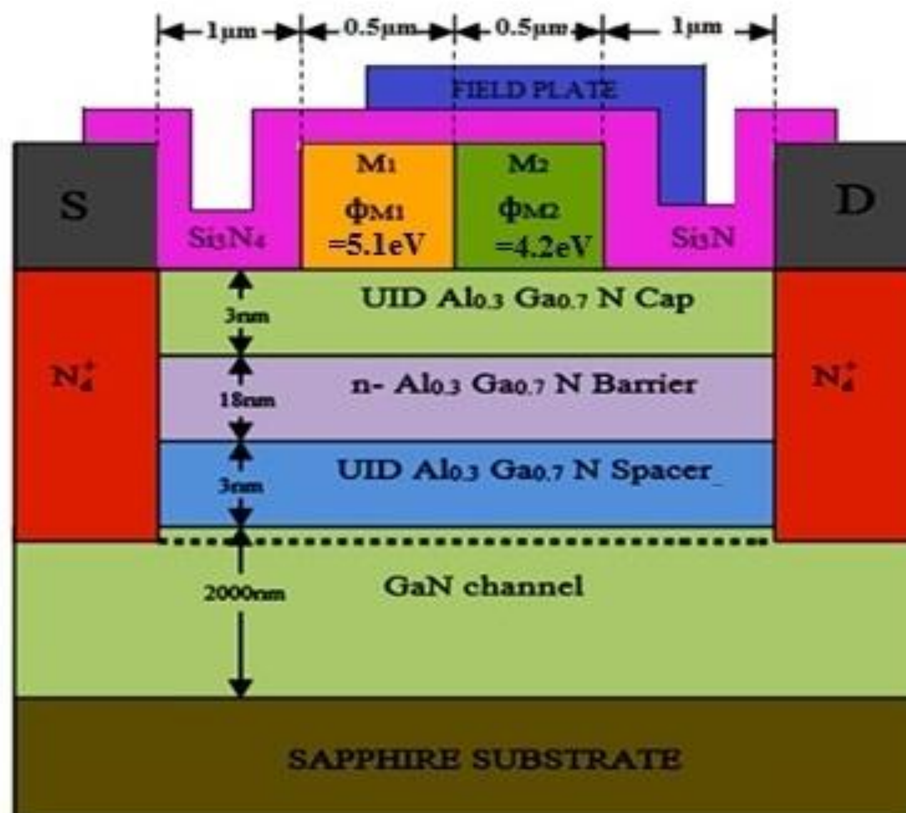

Figure 1 Cross sectional epitaxial view of field plated DMG AlGaN/GaN MODFET

ISBN: 978-93-86171-36-8

1.2 Small signal noise equivalent circuit model: A small-signal circuit model [15] is basis in determining the device noise figure. Model used in this article is superimposed on cross section of MODFET. It is well known fact that the model parameters are dependent on bias but independent from frequency. The important parameter of model is gate source capacitance, C_{gs}, and transconductance, g_m. R_g, R_s and R_d represent parasitic resistances of gate, source and drain respectively. L_s, L_d , L_g represent source, drain, gate electrodes inductances respectively.

Device contact pad capacitances between drain to source and gate to source are represented by C_{pg} and C_{pd} respectively. R_{gs} and R_{gd} represent input and output channel region resistances. C_{ds} C_{gs} and C_{gd} represent intrinsic capacitances between drain-source, gate-source and gate-drain respectively. g_{ds} represents drain conductance of device. Current generator ($g_m V_{gs}$) in the output circuit of the model is controlled by gate to source voltage (V_{gs}). Gate terminal capacitance having phase shift of $e^{-j\omega\tau}$ uses transit time (τ) through the velocity saturated region of the 2DEG-channel. Applied small amplitude RF signal at gate terminal has angular frequency (ω=2πf) in radian /sec. In noise equivalent circuit model, $\overline{i_{dn}^2}$ and $\overline{i_{gn}^2}$ represent output and input sources of noise current. All of parasitic resistances (R_s, R_g and R_d) generate thermal noise voltage can be modeled as [16]

$$\overline{e_g^2} = 4kT_a R_g \Delta f \tag{1}$$

$$\overline{e_s^2} = 4kT_a R_s \Delta f \tag{2}$$

$$\overline{e_d^2} = 4kT_a R_d \Delta f \tag{3}$$

Where T_a is ambient temperature, Δf is band width centered on frequency (f). R_s and R_g are more important for modeling of noise figure. R_d being at the output its magnitude of noise is far smaller than the channel noise therefore it can be ignored keeping accuracy intact in analysis. S-parameter measurements of devices along with open and shorted test were used to find the small-signal parameters of small signal noise equivalent circuit model.

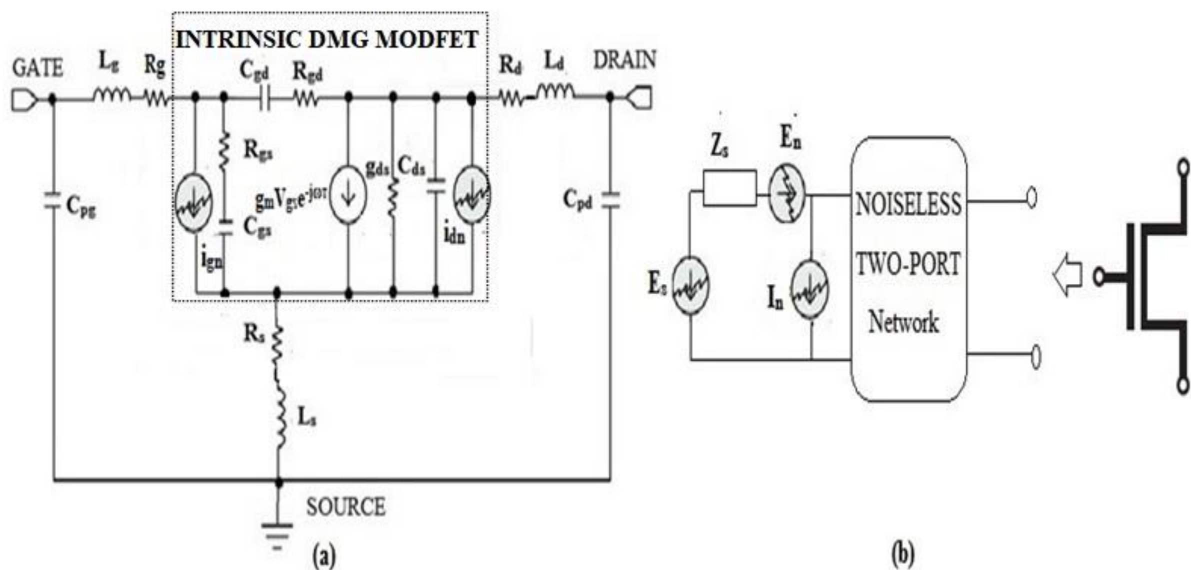

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Figure 2 (a) Small signal noise equivalent circuit model for DMG AlGaN/GaN HEMT (b Circuit model driven by noisy source of impedance Z_s

1.3 Analytical noise expressions: Following two models are applied for noise analysis of proposed device structure in the article. These are discussed below one by one:

1.3.1 Application of van der Ziel noise model: If we consider proposed device noise circuit model, the gate noise source, $\overline{i_{gn}^2}$ acts as fluctuating input noise source for the channel. Similarly noise current $\overline{i_{dn}^2}$ acts as output noise source in the device. Now, noise factor (F) for the device can be modelled using [8] as follows,

$$F = 1 + \frac{\left\langle \left| E_n + I_s Z_s \right|^2 \right\rangle}{\left\langle E_s \right\rangle^2} \tag{4}$$

$$F = F_{\min} + \frac{4R_n \left| \Gamma_s + \Gamma_{opt} \right|^2}{Z_o \left(1 - \left|\Gamma_s\right|^2\right) \left|1 + \Gamma_{opt}\right|^2} \tag{5}$$

Where, F, E_n, I_s, Z_s and E_s represent noise factor, equivalent open circuited noise voltage source, equivalent noise current source and source voltage respectively. F_{min}, Γ_s, $|\Gamma_{opt}|$ and $\angle\Gamma_{opt}$ are minimum noise figure, source reflection coefficient, magnitude and angle of reflection coefficient respectively. R_n is effective noise resistance that can be normalized to using reference impedance (Z_o) and then it can be represented as r_n (=R_n/Z_o). Noise factor can be represented in dB (=$10\log_{10}(F)$).

1.3.2 Application of PRC noise model: If we consider capacitive coupling to the gate through C_{gs} and C_{gd}, and correlated noise source at the drain terminal, the analytical expressions for device can be obtained. Considering gate noise source, drain noise source, correlation coefficient (C) and cross-term $\overline{i_{gn}^2 i_{dn}^{2\,*}}$, noise parameters can be modeled using [9] as

$$\overline{i_{gn}^2} = 4kT_a \gamma \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \Delta f \tag{6}$$

$$\overline{i_{dn}^2} = 4kT_a \Gamma g_{d0} \Delta f \tag{7}$$

$$C = \frac{\overline{i_{gn}^2 i_{dn}^{2\,*}}}{\sqrt{\overline{i_{gn}^2}\,\overline{i_{dn}^2}}} \tag{8}$$

$$C = \frac{\frac{2}{3} j\omega C_{gs} k T_a \Delta f}{\sqrt{\overline{i_{gn}^2}\,\overline{i_{dn}^2}}} \tag{9}$$

$$P = \frac{\overline{i_{dn}^2}}{4KT_a g_m \Delta f} \tag{10}$$

$$R = \frac{g_m}{4KT_a \omega^2 C_{gs}^2 \Delta f} \overline{i_{gn}^2} \tag{11}$$

Where, T_a, ω, g_{d0} are ambient temperature, angular frequency and drain conductance at zero drain bias respectively. Also Γ, γ are fitting parameters with values as 2/3 and 4/3 respectively [8]. We have considered

velocity saturation and noise changes with bias based small-signal parameters and their noise variables C , P and R as given by equation (9),(10) and (11) respectively.

III. RESULTS AND DISCUSSIONS

Analytical expressions of proposed noise circuit model are numerically evaluated using MATLAB software. Proposed device structure is simulated for noise properties using industry standard Silvaco TCAD device simulator [17]. Table.1 shows, the list of extracted small signal noise circuit model parameters of proposed device. Extracted results are in good match with experimental results of GaN MODFET devices [15] [18]. Fig.3 (a) shows simulated epitaxial contour of device giving structural profile under simulation. Fig.3(b) depicts simulated logarithmic potential profile inside device structure. Fig.4 (a) represents simulated log electric field-x in side device structure Fig.4 (b) shows relative percentage contributions of different noise sources to the overall noise figure of device. This is obtained using the model at an optimal bias for noise performance study. The channel thermal noise accounts for almost half the contribution to noise figure in device.

Fig.4 (a) and (b) show comparison of experimental [18] [19] and simulated smith plot of S_{11} and S_{22}. It is clear from charts that both S-parameters start from maximum impedance or open circuit and follow circles of capacitance while approaching towards matching point. Similarly Fig.5 (a) and (b) show comparison of experimental [19] [18] and simulated S12 and S21 parameters on smith charts. It is clear from the plot that with rise in frequency from 1GHz to 200GHz, the S_{12} and S_{21} follow circles of inductances. From analysis of S-parameters it can be said that device is stable up to 200 GHz of frequency. These plot also validate simulated results with corresponding experimental results.

Fig.6 (a) shows minimum noise figure, NF_{min} vs. frequency plot and compares model, simulation and experimental results [16] [20] for the purpose of validation. Fig. 6 (**b) shows n**ormalized noise resistance**,** $\mathbf{r_n}$ vs. frequency plot and compares model, simulated and experimental results to predict close conformity, Fig.6 (c) shows source reflection coefficient magnitude vs. frequency and source reflection coefficient angle vs frequency plot. Model simulated and experimental results are also validated for accuracy on comparison.

On comparison of all the extracted model, simulated and experimental results we find a close match in results. Now, it can be said that proposed noise circuit model provide accurate noise performance of enhanced DMG MODFET and can be used for LNA design.

Table 1 Extracted Small Signal Noise Circuit Model Parameters for 1X100μm^2 Gate Area MODFET at V_{ds}=24V and V_{gs}=-1V, T_a=296K

Intrinsic Parameters	Value	Extrinsic Parameters	Value	Noise Parameter	Value
g_m	38mS	R_g	6.5Ω	NF_{min}	1.12
C_{gs}	0.258pF	R_d	9Ω	r_n	1.05
C_{gd}	2.25fF	R_s	3.1Ω	Γ_{opt}	0.800
C_{ds}	20fF	L_s	12.6pH	$\angle\Gamma_{opt}$	19.7
g_{ds}	500mS/mm	L_g	45.4pH	$\langle i_g^2 \rangle \left(10^{-24} \frac{A^2}{Hz}\right)$	7.08

ISBN: 978-93-86171-36-8

R_{gs}	8.1Ω	L_d	22.5pH	$\langle i_d^2 \rangle \left(10^{-24} \frac{A^2}{Hz}\right)$	5.90
R_{gd}	1.8KΩ	C_{pg}	1.4fF	$\lvert C \rvert$	0.801
τ	*2.3pS*	C_{pd}	29fF	∠C (degrees)	115

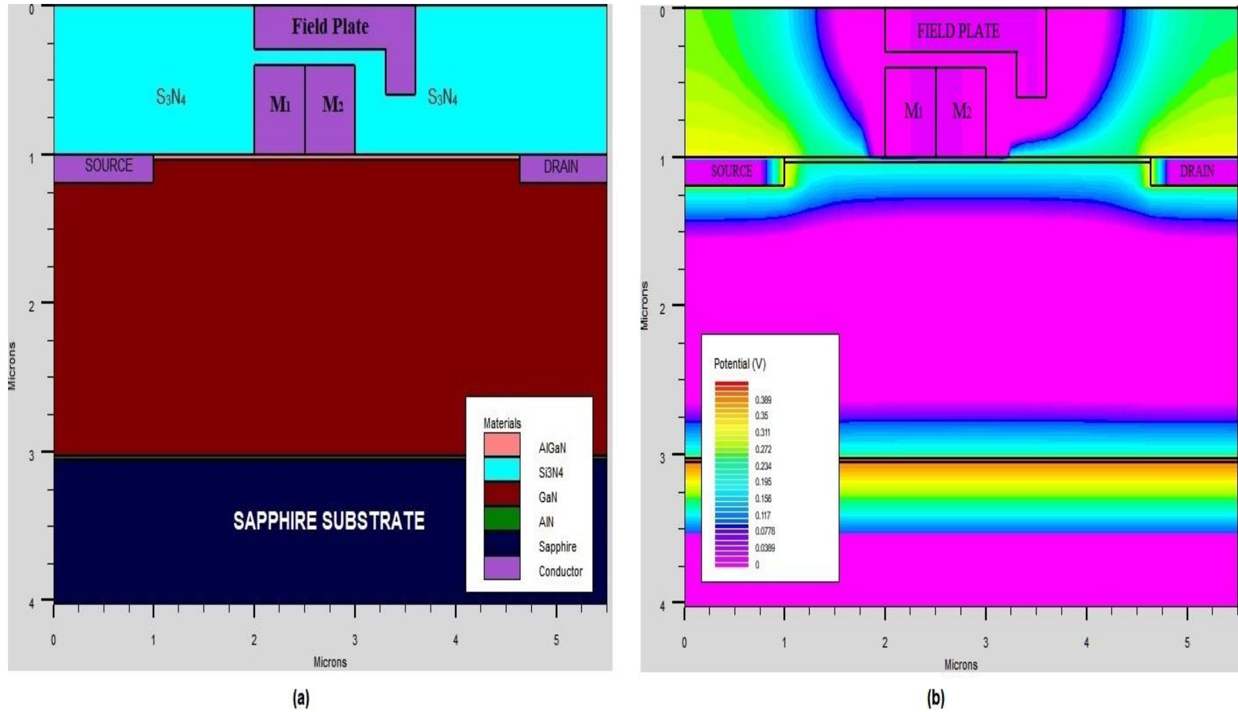

Figure 3 (a) Simulated epitaxial contour of device N (b) Simulated logarithmic potential contour of proposed device

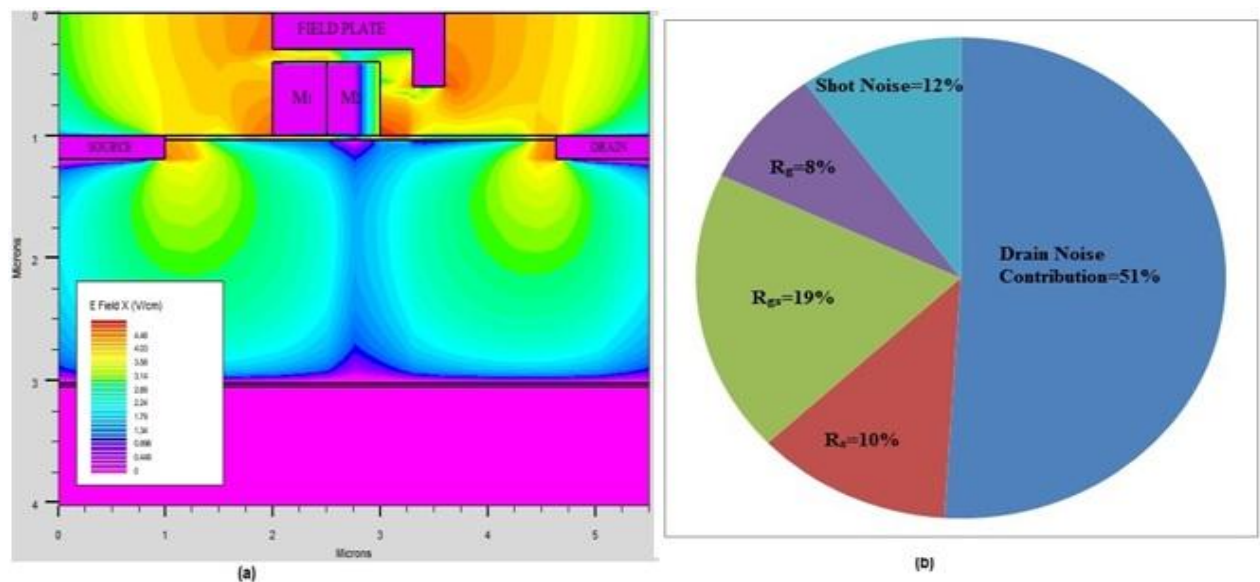

Figure 4 (a) Simulated log electric field contour of device (b) Pie chart showing relative contributions of different noise sources to the overall noise figure of device.

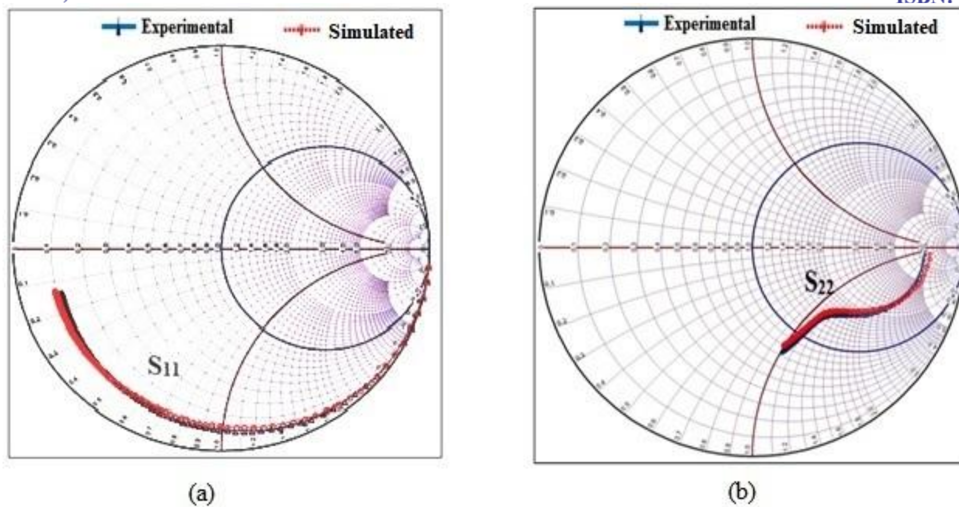

Figure 5 (a) Smith plot for measured (blue triangles) and simulated (red circles) S_{11} parameters and (b) Smith plot for measured (blue triangles) and simulated (red circles) S_{22} parameters at Vgs=-1V, Vds=24V, fstart=1GHz fstop=200GHz

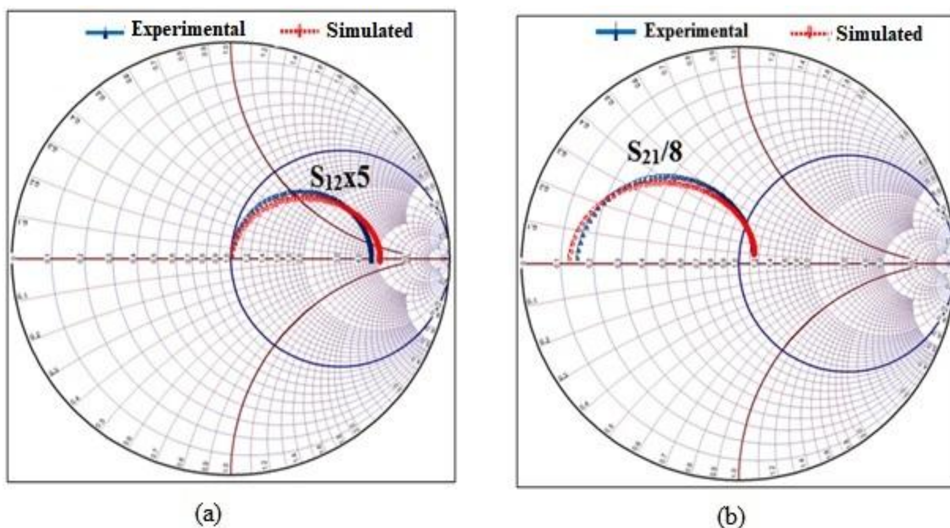

Figure 6 (a) Smith plot for measured (blue triangles) and simulated (red circles) S_{12} parameters and (b) Smith plot for measured (blue triangles) and simulated (red circles) S_{21} parameters at Vgs=-1V, Vds=24V, fstart=1GHz fstop=200GHz

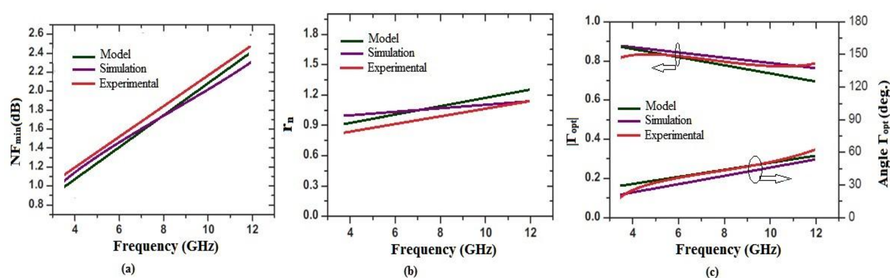

Figure 7 (a) NF_{min} vs. Frequency plot (b) Normalized noise resistance, r_n vs. frequency plot (c) Source reflection coefficient magnitude vs. frequency and Source reflection coefficient angle vs frequency plot

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IV. CONCLUSION

A minimum value of noise figure (NF_{min}) of 1.21 at 3 GHz and maximum value of noise figure (NF_{min}) of 2.40 at 12 GHz is obtained for the proposed device. Normalized noise resistance for device varies from 0.9 at 3GHz to 1.35 at 12 GHz of operating frequency. Magnitude of source reflection coefficient varies from 0.9 at 3GHz to 0.84 at 12 GHz. Angle of source reflection coefficient varies from 30 degrees at 3GHz to 50 degrees at 12 GHz of operating frequency. The model results are validated with simulation and experimental results and found to be in good agreement. It can now be concluded that the proposed device small signal noise circuit model is consistent and accurate. On the basis of extracted results it can be stated that our proposed device has superior noise performances in comparison of conventional MODFETs and can be used for design of low noise amplifies (LNA). Proposed device model can also be used for the purpose of circuit simulation in TCAD softwares.

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ISBN: 978-93-86171-36-8

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