

REVIEW ON DIFFERENT FPGA BASED DATA COMMUNICATION SYSTEM DESIGN

Ms. Amruta Joshi¹, Prof. A.S.Patel²

^{1,2}E&TC Department, MSSs CET, NagewadiJalna(MS), (India)

ABSTRACT

In the current years, evolution of sensor systems not only provide more accuracy and resolution but also decreasing the size and power consumption. FPGAs are reprogrammable silicon chips and can configure these chips to implement custom hardware functionality without ever having to pick up a breadboard. Field Programmable Gate Array (FPGA) providing the sensor systems new capabilities with different functions likes self-diagnosis, signal processing, communications in a WSN, etc. This paper reviews the Field Programmable Gate Array (FPGA) and also focus on FPGA-based systems. This paper has overview of FPGA in the previous recent years.

Keywords: WSN, FPGA, reprogrammable, signal processing.

I. INTRODUCTION

In the modern electronics and communication, Processing capabilities in sensor nodes are typically based on Digital Signal Processors (DSPs). For the different needs developer needs programmable or re-programmable microcontrollers. Field Programmable Gate Arrays (FPGAs) provides specific hardware technology, which can also be reprogrammable thus providing a reconfigurable sensor system. Field Programmable Gate Arrays (FPGAs) architectures allow not only implementation of simple combinational and sequential circuits, but also the inclusion of high-level soft processors, and also provide different benefits to the user like performance, customization, time to market, obsolescence mitigation, reliability, component and cost reduction and hardware acceleration. FPGA embedded processors use FPGA logic elements to build internal memory units, data and control busses, internal and external peripheral and memory controllers[3].

Field Programmable Gate Array (FPGA) devices and high-level hardware development languages represent a new and exciting addition to traditional research tools, where simulation models can be evaluated by the direct implementation of complex algorithms and processes [8]. Field-programmable gate arrays (FPGAs) are drawing ever increasing interest from designers of embedded wireless communications systems [9]. The FPGA architecture consists of three types of configurable elements IOBs (provide a programmable interface between the CLBs and the device's external package pins), Configurable Logic Block i.e. CLBs (programmable logic blocks of FPGA are called Configurable Logic Block) and Resources for interconnection [6]. Also FPGA-based hardware emulation and rapid prototyping have become an attractive solution, which can run up to 106 times faster than software simulation at the same level of modeling complexity [10]. Figure 1 shows Basic FPGA structure, which consists of an array of programmable logic blocks of potentially different types, including

general logic, memory and multiplier blocks. These blocks are surrounded by a programmable routing fabric that allows blocks to be programmable (term means an ability to program a function into the chip after silicon fabrication is complete) interconnected. labeled I/O in the figure are the arrays, which is surrounded by programmable input/output block that connect the chip to the outside world [7].

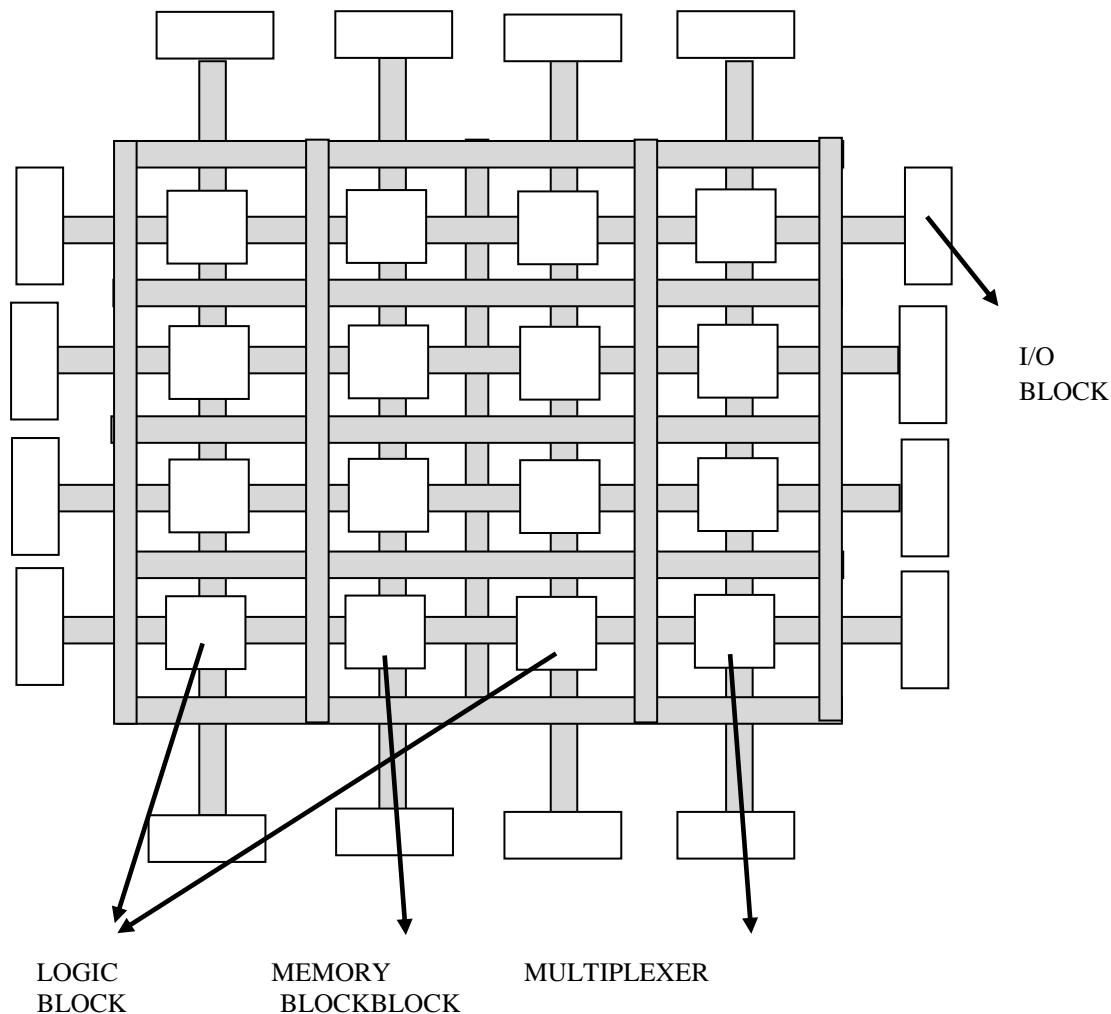
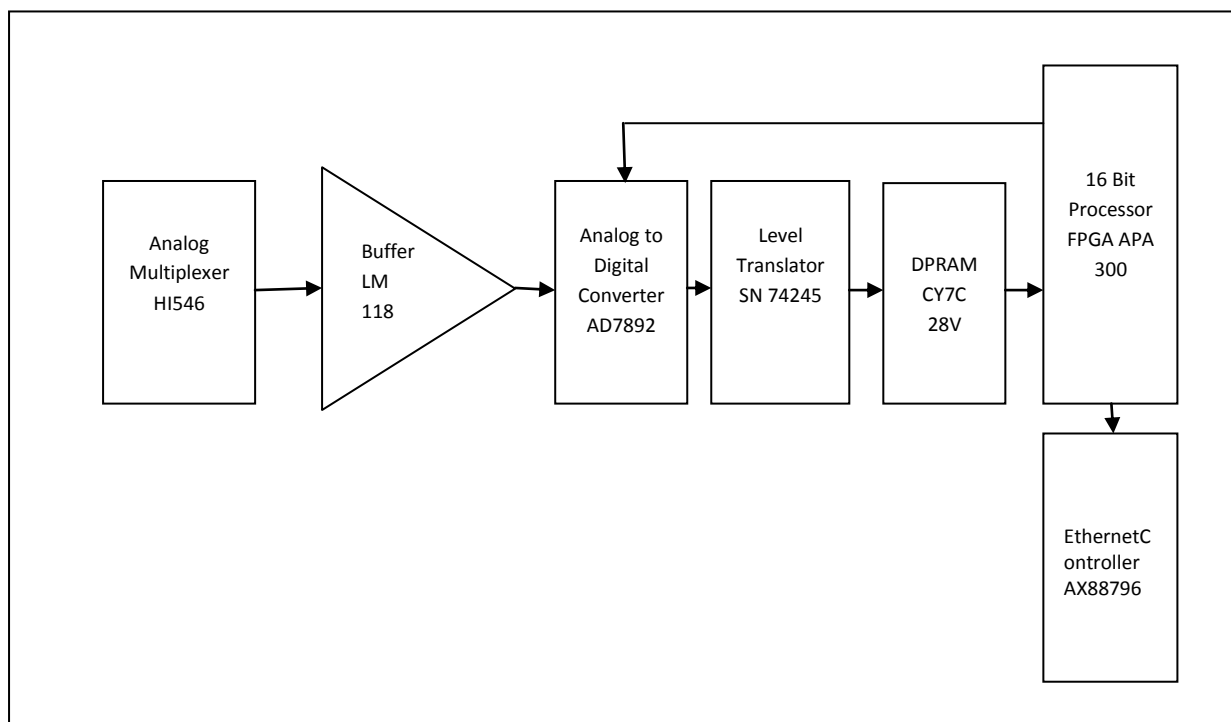


Fig. 1
Basic
FPGA
structure
[7]

II. Related Work

Suma G. S [1] presents develop FPGA based 16 channel high speed Data Acquisition System with Ethernet interface. This system consists of Analog Multiplexer, Buffer, and Analog to Digital Converter, Level Translator, DPRAM, Ethernet Controller and 16 bit processor implemented in FPGA with VHDL as shown in the figure 2. In this system input data will acquired through 16 channels and in the first Analog Multiplexer will given for Analog to Digital converter, where multiplexer select lines are generated according to the input from data is to be acquired. Buffer is used to store the digital data. In the third block i.e. analog to digital converter AD7892 multiplexed input signals are digitalized and translated to the new voltage level and in the next step, level translation is used to make the input voltage compatible to the FPGA. These compatible voltage inputs are stored in the DPRAM. Design of control unit on FPGA consists of 16 bit processor (16 bit separate data bus for

input and output and also has 64K address space), RAM (it is required for the storing of the program as well as data and implemented as 2048 X 16 supporting synchronous read and write operations in VHDL with 11 address lines), ROM (is implemented as 2048 X 16 supporting read operations in VHDL with 11 address lines), Buffer (The buffer multiplexes the internal input and output data line, to form multiplexed IO lines externally and also it de-multiplexes the external IO lines to form separate input and output data lines to use internally) and address decoder (decoder module having the input read, write and address lines signal which are generated from CPU).



realtime remote monitoring using Bluetooth between FPGA based embedded system and android smart phones. Figure 3 shows the block diagram of system implementation and the proposed system consist of a hardware and software part. Hardware part consists of distinctive sensors (like LM35 as temperature sensor, MQ-7 as smoke sensor and XA001 as heartbeat sensor), FPGA (XC3S100E is also a FPGA and having high clocking speed and great interfacing feature which will berequired for sensors and Bluetooth module), Bluetooth module and android Smartphone. Here The output of LM35D temperature sensing element is in voltage and is applied to the ADC0808, which regenerate to the digital equivalent and is then processed by the FPGA that shows the temperature value, Similarly, for smoke sensing element also. Software part consists of Xilinx ISE (it provides is a design environment for FPGA. It is used for circuit synthesis and design while the models logic simulator is used for system level testing) and android studio.

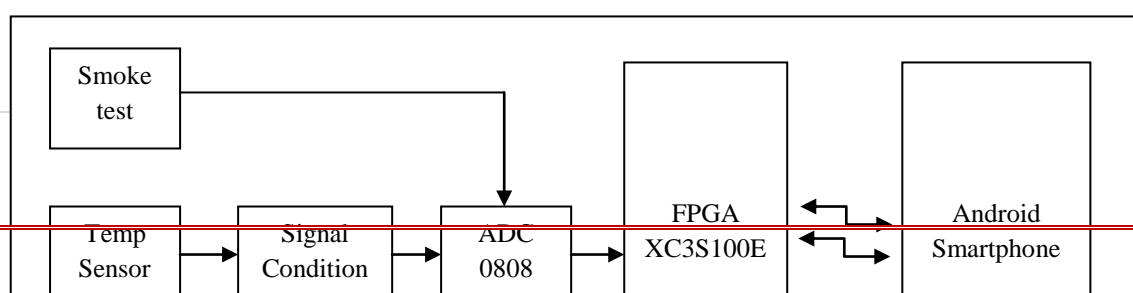
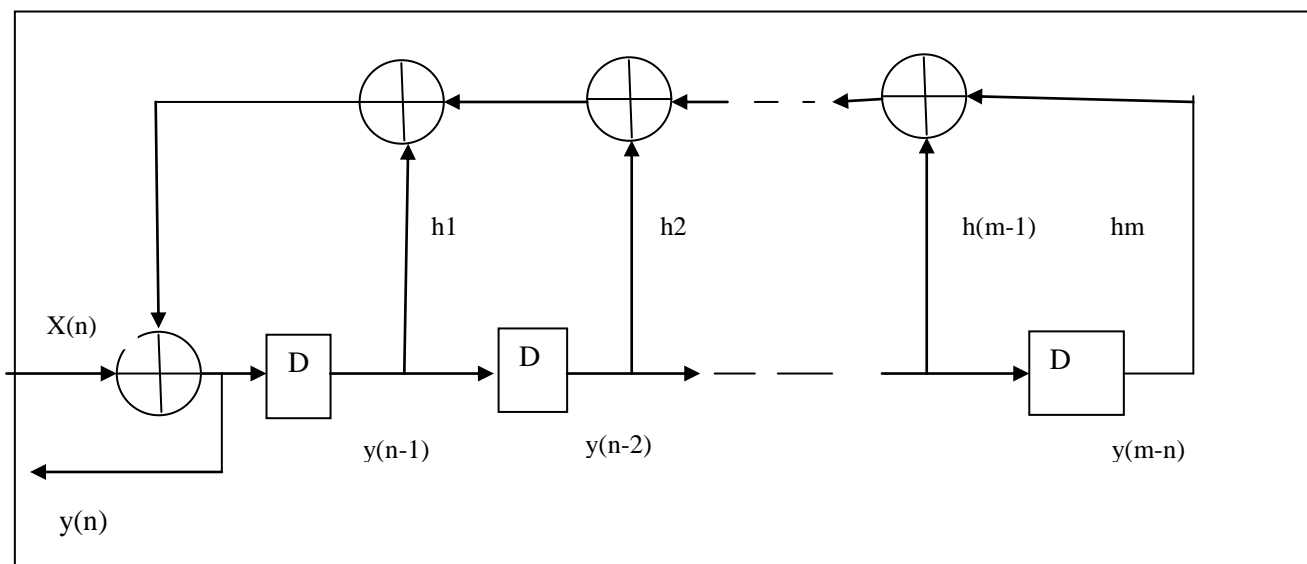


Fig.3 Block diagram of system implementation [2].

Davinder Pal Sharma [4] provides FPGA based Data Scrambler for Ultra-Wideband Communication Systems, these systems not only provide transfer data from a rate of 110Mbps to 480Mbps in realistic multipath environment but also they consume very little power and silicon area. Synchronization plays very critical role in this type of system, for this problem scrambler is used. Scrambler for UWB communication systems has been modeled and simulated using Matlab and Xilinx's System Generator for DSP. Data scrambler is generally made up of linear sequential filters with feedback paths, counters, storage elements and peripheral logic in their discrete form. **Figure 4 shows the Basic structure of a data scrambler.**

**Fig.4 Basic structure of a data scrambler [4]**

S. Thanee S. et al [5] proposed a data acquisition system with high speed USB interface using FPGA chip as the main processing unit. Figure 5 shows the overall proposed system, which contains the four different ADC (analog to digital converter) sensors with four different protocols: Parallel, SPI, I2C and One-Wire, and FPGA processing unit i.e. EP1K10TC144-3 (supports the power supply at 3 levels, which are 5V, 3.3V and 2.5V and maximum operating frequency is 180 MHz). The FPGA collects the individual data from all ADC sensors and processes it individually. After that it produces a stream of data through the output USB port. A specific

application program is written to control the PC and also having a function to communicate to the FPGA so that the PC could prepare itself for the data transfer. The PC will check the FPGA for data availability on the system and it will send a set of the instructions to the FPGA for getting these data from USB port.

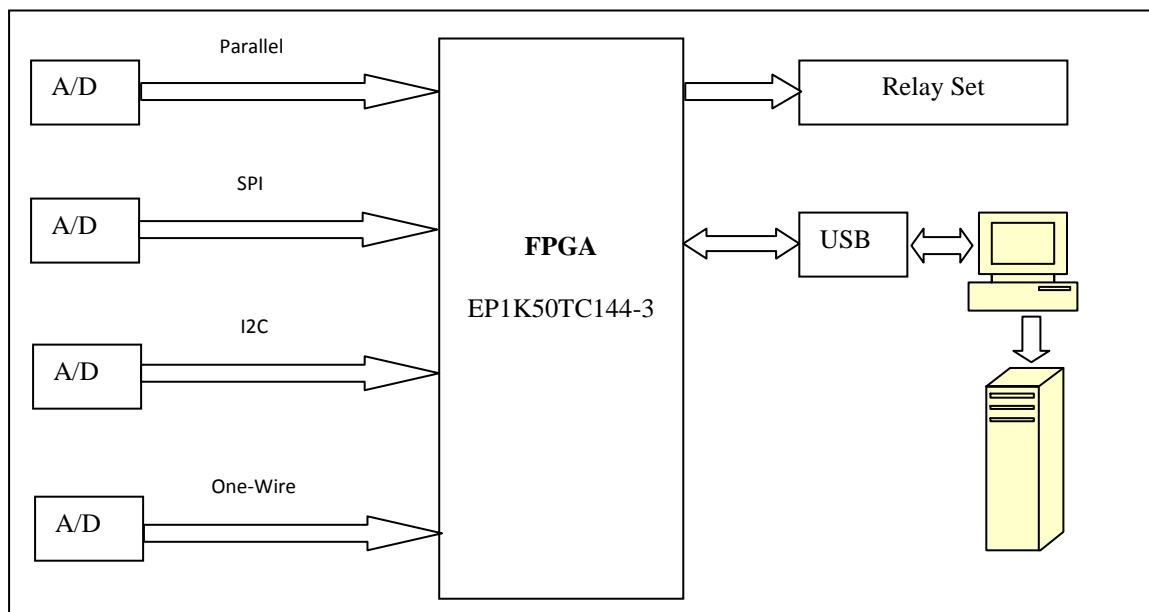


Fig.5 Overall system diagram [5].

III. FIGURES AND TABLES

List of Figures

FIG. Number	Title
Fig. 1	Basic FPGA structure
Fig. 2	Block diagram of Proposed Design
Fig. 3	Block diagram of system implementation
Fig. 4	Basic structure of a data scrambler
Fig. 5	Overall system diagram

IV. CONCLUSION

FPGA devices have reached a high level of development that puts them in competition with the traditional application specific integrated circuits (ASICs). Field Programmable Gate Array (FPGA) providing the sensor systems new capabilities with different functions likes self-diagnosis, signal processing, communications in a WSN, etc. This paper reviews the Field Programmable Gate Array (FPGA) and also focus on FPGA-based systems.

REFERENCES

Journal Papers:

- [1] Suma G. S. “FPGA Based High Speed Data Acquisition System with Ethernet Interface”, International Journal of Advances in Science Engineering and Technology, Volume- 2, Issue-3, July-2014, pp.99-102.
- [2] Piyush V. Savaliya, Sunil B. Somani, and Virendra V. Shete, “FPGA Based Real Time Bluetooth Communication for Tele health, Household Security and Industry Safety”, International Journal of Innovative Research in Computer and Communication Engineering, Vol. 3, Issue 8, August 2015, pp. 7209-7215.
- [3] Gabriel J. Garcia, “Carlos A. Jara, Jorge Pomares, Aiman Alabdo, Lucas M. Poggi, and Fernando Torres, “A Survey on FPGA-Based Sensor Systems: Towards Intelligent and Reconfigurable Low-Power Sensors for Computer Vision, Control and Signal Processing”, Multidisciplinary Digital Publishing Institute (MDPI), 31 march 2014.
- [4] Davinder Pal Sharma, “FPGA based Data Scrambler for Ultra-Wideband Communication Systems”, Proc. of Int. Conf. on Recent Trends in Information, Telecommunication and Computing, 2013.
- [5] S. Thanee S. Somkuarnpanit and K. Saetang, “FPGA-Based Multi Protocol Data Acquisition System with High Speed USB Interface”, Proceedings of the international Multiconference of Engineers and Computer Scientists, 2010.
- [6] <http://www.srmuniv.ac.in/ramapuram/sites/ramapuram/files/part2.pdf>
- [7] Ian Kuon, Russell Tessier and Jonathan Rose, “FPGA Architecture: Survey and Challenges”, Electronic Design Automation Vol. 2, No. 2, 2007, pp. 135–253.
- [8] Marcus Robert Perrett, “Wireless multi-carrier communication system design and implementation using a custom hardware and software FPGA platform”, Doctoral thesis, 2012.
- [9] Constantin Siriteanu, Steven D. Blostein, and James Millar, “FPGA-Based Communications Receivers for Smart Antenna Array Embedded Systems”, EURASIP Journal on Embedded Systems Volume, Article ID 81309, 2006, Pages 1–13.
- [10] Chen Chang, Kimmo Kuusilinna, Brian Richards, Allen Chen, Nathan Chan, Robert W. Brodersen, and Borivoje Nikoliu, “Rapid Design and Analysis of Communication Systems Using the BEE Hardware Emulation Environment”, Proceedings of the 14th IEEE International Workshop on Rapid Systems Prototyping (RSP’03), 2003.