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SINGLE PHASE HYBRIDIZED NINE-LEVEL INVERTER

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ABSTRACT

The main objective of this paper is to analyze two different types of nine level inverters. This paper depends on the multilevel converters with multiple numbers of DC sources and presents cascaded H-bridge nine level inverter and multi string nine level inverter topologies with four input DC sources. The purpose of this paper is to show the differences between these two converters in terms of modulation scheme, switching losses. These comparisons were never made between cascaded H-bridge multi-level converter (CHBMC) and multi string multi-level inverter (MMC). The modulation schemes and the determination of unipolar PWM modulation signals of these two converters are discussed. The switching losses between these two converters are also discussed. Simulation and experimental results of the two converters validate the proposed analysis.

Keywords: Multilevel inverter, LS - PWM, modulation index.

I. INTRODUCTION

In the last few years, the necessity of increasing the power level in the industry has sustained the continuous development of multilevel converters due to their capability of handling voltages up to 6.9kv and power of several megawatts. Since the presentation of multilevel cascade H-bridge (CHBMC) in

1975 [2], the converter has received much research attention due to their several advantages compared to other multilevel converter topologies in terms of simplicity, modularity, reliability and the number of levels with a minimum number of power semiconductor devices Environmental friendly distributed energy resources (DERs) are very well desired in the light of global warming and climate change. The integrating interface converters of DERs are used for photovoltaic panels (PV), wind power, micro turbines and fuel cells. These converters deliver electric power in terms of high efficiency and reliability. Multi-level inverters are generally used as an interface between the photovoltaic panels and the utility grid. So there is a need to find the effective converter that can be used as an interface. When compared with the present available multi-level converters, the both cascaded H-bridge (CHBMC) and multi string multi-level inverters (MMC) would be better and efficient interfaces.

The CHBMC has been employed to develop different applications, such as synchronous rectifiers, inverters, STATCOM, active filters, renewable energy integration systems, motor drives, etc. Moreover, specific control strategies and modulation techniques, associated with those applications, have been designed for this converter configuration. The behavior of the CHBMC during transient and steady-state operations can be estimated from

the model of the inverter. Multi-level cascaded H-bridge single phase DC-AC converter with reduced voltage ripple can be an advantageous utility as an interface between the photovoltaic panels and the utility grid.

II. TOPOLOGIES OF CASCADED H-BRIDGE AND MULTI STRING NINE-LEVEL INVERTERS CHBMC

A multilevel cascaded inverter consisting of four H bridges is shown in Fig. 1. The individual output voltages of the each cells are *Vabi*, and *Tapi*, *Tbpi* and *Tani*, *Tbni* are the switching functions of the upper and lower switches, respectively (where *i=1, 2, 3* and *4*). The equations for the output voltages of individual cells in terms of input DC voltages are given as follows.

$$\begin{aligned} V_{ab1} &= V_{dc1}\left(S_{ap1} - S_{bp1}\right), \\ V_{ab2} &= V_{dc2}\left(S_{ap2} - S_{bp2}\right) \\ V_{ab3} &= V_{dc3}\left(S_{ap3} - S_{bp3}\right), \\ V_{ab4} &= V_{dc4}\left(S_{ap4} - S_{bp4}\right) \end{aligned} \qquad (1)$$

Therefore $VAB = Vab1 + Vab2 + Vab3 + Vab4$

$$V_{AB} = \begin{bmatrix} V_{dc1}\left(S_{ap1} - S_{bp1}\right) + V_{dc2}\left(S_{ap2} - S_{bp2}\right) \\ + V_{dc3}\left(S_{ap3} - S_{bp3}\right) + V_{dc4}\left(S_{ap4} - S_{bp4}\right) \end{bmatrix} \qquad (2)$$

The equations for the input currents are also given by

$$\begin{aligned} I_{s1} &= I_{o1}\left(S_{ap1} - S_{bp1}\right), \\ I_{s2} &= I_{o2}\left(S_{ap2} - S_{bp2}\right) \\ I_{s3} &= I_{o3}\left(S_{ap3} - S_{bp3}\right), \\ I_{s4} &= I_{o4}\left(S_{ap4} - S_{bp4}\right) \end{aligned} \qquad (3)$$

Where *Io*1, *Io*2 , *Io*3, *Io*4 are the individual output currents from beach inverter cell. *Io*1 = *Io*2 = *I o*3 = *I o*4 when the cells are connected in cascade.

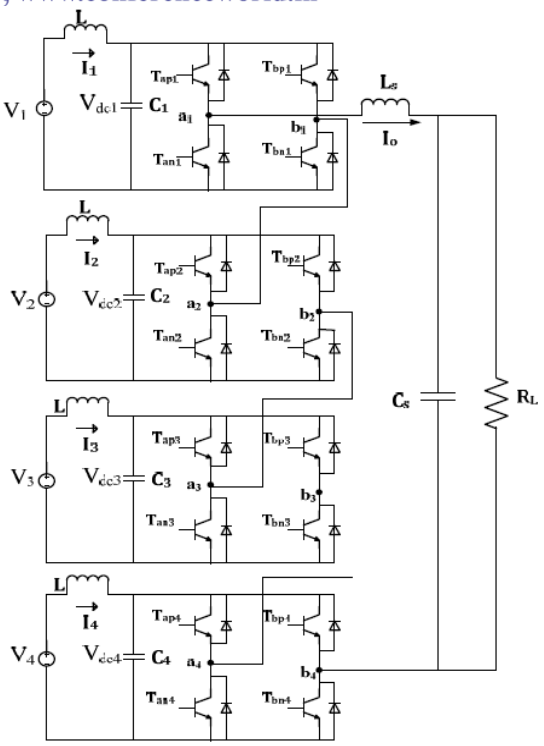

Fig.1. Four level cascaded H-bridge converter

III.MODULATION PROCESS

CHBMC (Phase Shifted PWM):

Consider an 'n' level converter, then the total number of switches in 'n' level converter are 2(n −1). For generating the carrier based PWM, minimum two modulation signals and(n-1)/2 carrier waveforms are required. The modulation strategy developed in this work is a phase shifted unipolar pulse width modulation scheme. The two legs of the full-bridge inverter are controlled separately by comparing a high frequency triangular carrier with two line frequency modulating signals which are displaced by 180° out of phase from each other. As shown in Fig. 2, mai, mbi are the modulation signals for each leg of the single inverter. T1,T2 ,T3 and T4 are the triangle carrier signals corresponding to each H-bridges and they all are displaced by 45 from each other. Each switching pulses are generated as follows

$S_{api} = 1$ if $m_{ai} > T_i$ and 0 otherwise
$S_{bpi} = 1$ if $m_{bi} > T_i$ and 0 otherwise
$S_{ani} = 1$ if $m_{ai} < T_i$ and 0 otherwise
$S_{bni} = 1$ if $m_{bi} < T_i$ and 0 otherwise
Where $i=1, 2, 3$ and 4

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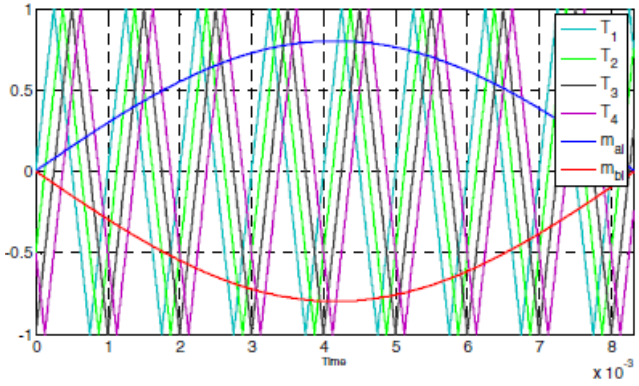

Fig. 2. Modulation Scheme of CHBMC

MULTI STRING MC (Level Shifted PWM):

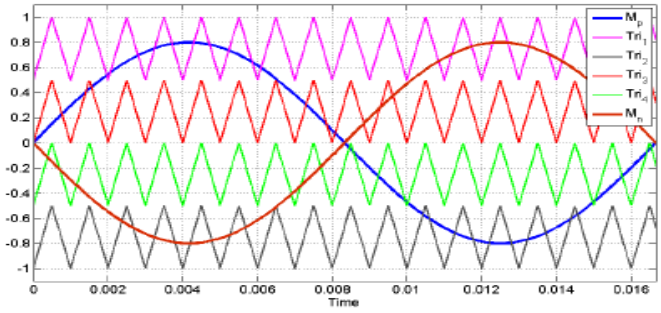

Fig. 3. Modulation Scheme of multi string mc

For modulation scheme, level shifted carrier based PWM is used. In level shifted PWM, the carrier waveforms are one above another with equal amplitude. If the switching pulses of switches in one leg are generated, then their complementary will be respectively the switching pulses of switches in another leg. The generation of switching pulses ifollows:

$$S_{ap} = \begin{cases} 1 \text{ when } \begin{pmatrix} Tri_1 < M_p < Tri_2 \text{ for } M_p > 0, \\ M_p > Tri_3, M_p < Tri_4 \text{ for } M_p < 0 \end{pmatrix} \\ 0 \text{ when } \begin{pmatrix} M_p > Tri_1, M_p < Tri_2 \text{ for } M_p > 0, \\ Tri_3 < M_p < Tri_4 \text{ for } M_p < 0 \end{pmatrix} \end{cases}$$

$$S_{am} = \begin{cases} 1 \text{ when } M_p > Tri_2 \text{ for } M_p > 0 \text{ and } M_p > Tri_3 \text{ for } M_p < 0 \\ 0 \text{ when } M_p < Tri_2 \text{ for } M_p > 0 \text{ and } M_p < Tri_3 \text{ for } M_p < 0 \end{cases}$$

$$S_{an} = \begin{cases} 1 \text{ when } M_n > 0 \\ 0 \text{ when } M_n < 0 \end{cases}$$

$$S_{ao} = \begin{cases} 1 \text{ when } M_n < Tri_2 \text{ for } M_n > 0 \text{ and } M_n < Tri_3 \text{ for } M_n < 0 \\ 0 \text{ when } M_n > Tri_2 \text{ for } M_n > 0 \text{ and } M_n > Tri_3 \text{ for } M_n < 0 \end{cases}$$

$$S_{ar} = \begin{cases} 1 \text{ when } \begin{pmatrix} Tri_3 < M_n < Tri_4 \text{ for } M_n < 0, \\ M_n < Tri_2, M_n > Tri_1 \text{ for } M_n > 0 \end{pmatrix} \\ 0 \text{ when } \begin{pmatrix} Tri_1 < M_n < Tri_2 \text{ for } M_n > 0, \\ M_n > Tri_3, M_n < Tri_4 \text{ for } M_n < 0 \end{pmatrix} \end{cases}$$

Where M p and Mn are the modulation signals and Tri1 ,Tri2 , Tri3 and Tri4 are the four carrier waveforms used to generate switching pulses by level shifted carrier based PWM. The modulation signals and carrier waveforms can be seen in Fig. 3.

IV. SIMULATION RESULTS

CHBMC:

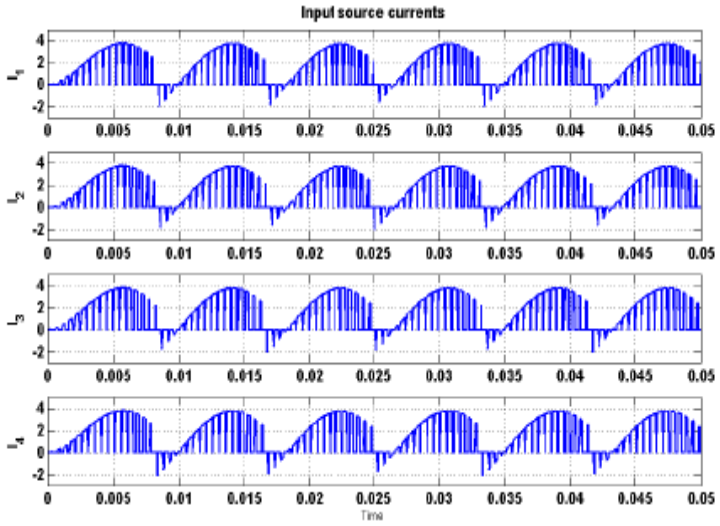

Fig 4: Input current source

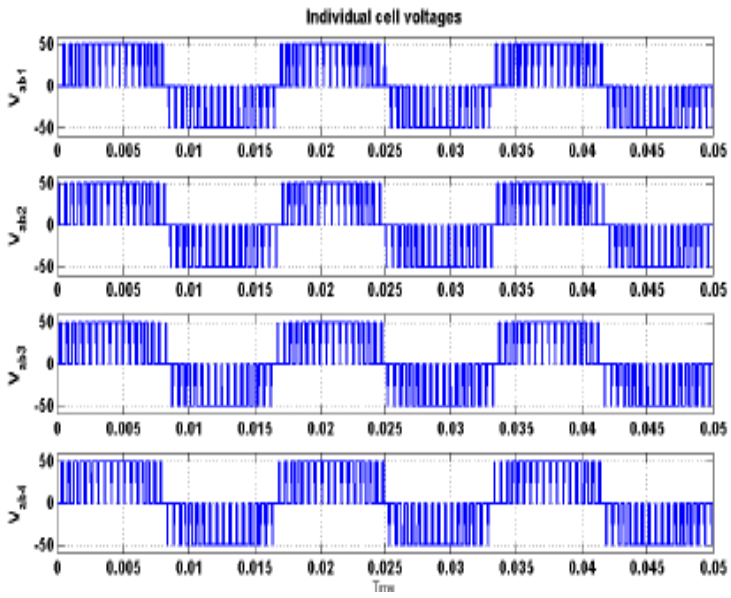

Fig. 5. Individuall cell voltages of CHBMC

The proposed modulation scheme is implemented on four cell cascaded H-Bridge Multi level converter. Simulation Results are done on Four cell cascaded H-Bridge Single phase AC-Dc converter is used to generate AC voltage when each of four cell is fed with 50v dc.

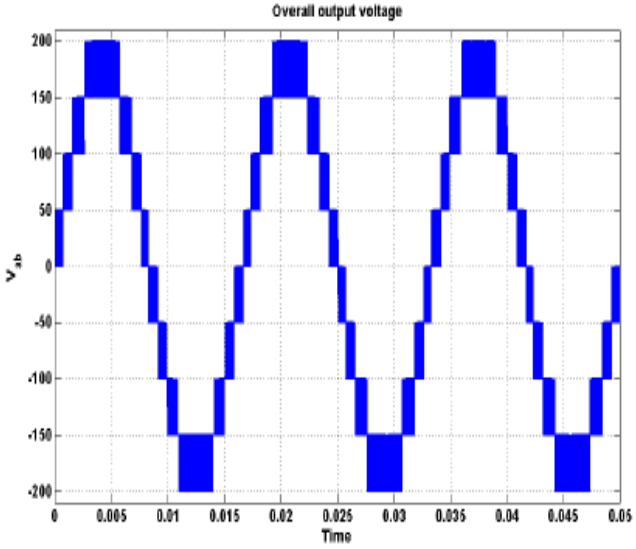

Fig. 6. Overall output voltage of CHBMC

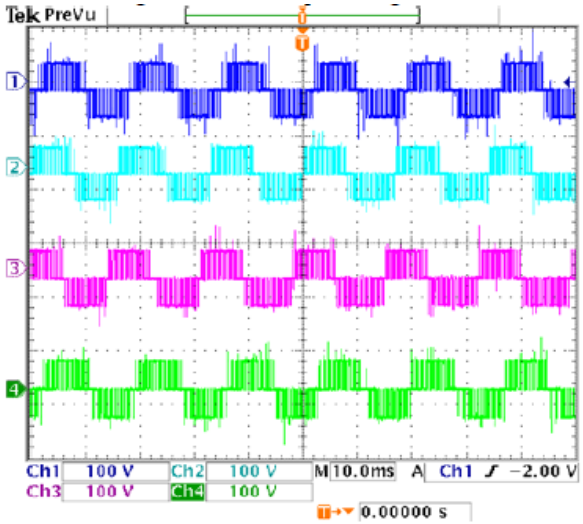

Fig. 7. Experimental waveform of Individual cell voltages of CHBMC

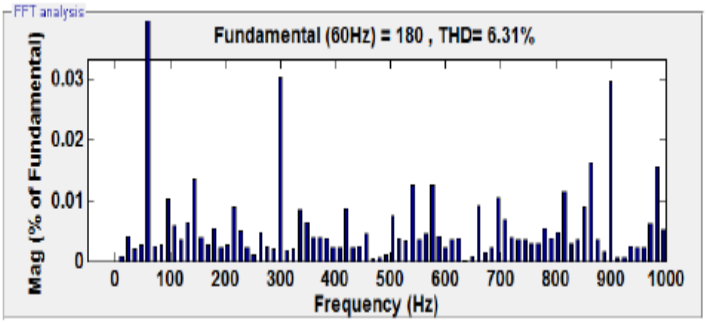

Fig. 9. Experimental waveform of overall output voltage of CHBMC

Fig. 5, and Fig. 6 shows the simulation results of individual output voltage of each cell and the overall output voltage of the inverter based on the proposed method.

Fig. 7, and Fig. 8 validate the simulation results of individual output voltage of each cell and the overall output voltage of the inverter. The Fourier spectrum analysis of the overall output voltage is seen in Fig. 9. As we can

see from this Fourier spectrum that the harmonic magnitude of the 3rd, 5th. 7th and9th harmonics is less than 0.05% of fundamental voltage. Therefore, this result verifies that the modulation indices calculated based on the proposed technique results in the minimization of harmonics.

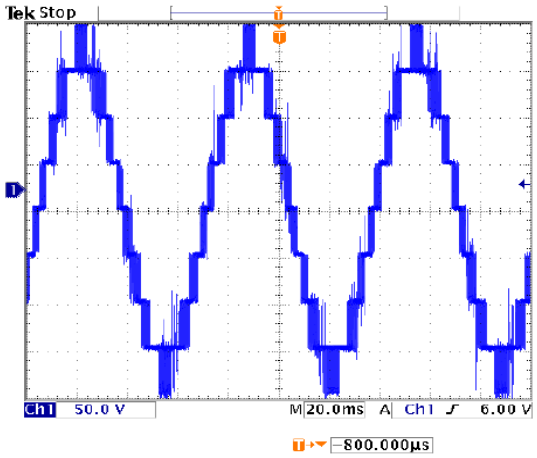

Fig. 10. Experimental waveform of Output voltage of multi string ninelevel converter

IV CONCLUSION

This paper presents two single-phase DC-AC multi-level converters which utilizes same number of DC sources. The topologies of both the inverters are presented and compared. The phase shift carrier based PWM for CHBMC and level shift carrier based PWM for multi string multi-level converters are also presented. The unipolar PWM modulation signals using double Fourier series for CHBMC and double Fourier series approximation of switching functions for multi string multi-level converter are determined. The switching losses between two converters are approximated and are also compared. Simulation and experimental results of both the converters are carried out and they validate each other and also the proposed analysis. The only disadvantage with this type of converter when compared with cascade H bridge multi-level converter is rating of middle switches which should be twice of other four switches.

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