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COTS BASED LOW ENERGY MULTIPROCESSOR EMBEDDED SYSTEM

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ABSTRACT

The real-time embedded systems have to meet their timing constraints in all circumstances. Besides, in these systems, increased productivity and reduced time to market are fundamental for product success. To design complex embedded systems while reducing the development time and cost, there is a great tendency to use commercial off-the-shelf ("COTS") devices. At system level, dynamic voltage and frequency.scaling (DVFS) is amongst the best systems for energy reduction. In any case, many broadly utilized COTS processors either don't have DVFS or apply DVFS only to processor cores. In this paper, an easy-to-implement COTS-based evaluation platform for low-energy embedded systems is introduced. To accomplish energy saving, DVFS is provided for the whole microcontroller (including core, phase-locked loop, memory, and I/O). Furthermore, facilities are provided for experimenting with fault-tolerance techniques. The platform is equipped with energy measurement and debugging equipment. Physical experiments demonstrate that applying DVFS on the whole microcontroller provides up to 47% and 12% energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively. Although the platform is designed for ARM-based embedded systems, our approach is general and can be applied to other types of systems.

Keywords: DPM,DVFS, Energy management, Embedded systems, hardware platform.

I. INTRODUCTION

The real-time embedded systems have to meet their timing constraints in all conditions. Additionally these frameworks often operate in harsh environments and may have a limited energy budget. Therefore, both fault-tolerance and low energy consumption should be carefully considered in the design of these systems. Nonetheless, high fault tolerance and low energy utilization are conflicting objectives and also they are generally in contrast to timing requirements. Hard real-time systems often require hardware redundancy (replication), but the imposed redundancy leads to more energy consumption. Then again, most popular system level energy-management techniques, e.g., Dynamic Voltage Scaling (DVS), have negative impacts on the system reliability. Accordingly, in designing safety-critical hard real-time systems, it is inevitable to consider fault-tolerance and energy consumption jointly.

Embedded systems are ubiquitous, and demand for these systems is developing dynamically. An extensive variety of embedded systems are battery operated. As, for a considerable of these systems, there is no possibility of frequently charging or replacing their batteries, they are highly energy constrained [1], [2]. Therefore, for

these systems, low energy utilization has become one of the major design objectives. Examples include mobile robots and handheld devices such as personal digital assistants, cell phones, and portable medical care devices. Furthermore, the complexity of embedded systems is increasing as the number of parts and the number and types of interactions among them are increasing [2], [3]. Accordingly, embedded system designers are always conducted at the request of designing complex embedded systems with several design objectives.

In this paper, to meet the design requirements of multiobjective embedded systems, we propose a hardware platform for experimenting with energy management techniques (i.e., dynamic power management (DPM) [7] and DVFS). Compared with previous related works (that proposed platforms for embedded systems), our platform:

1) gives DVFS capability for the microcontrollers, including not only the processor cores but also PLL, memory, and I/O; it should be noted that many existing designs either do not have DVFS or apply DVFS only to processor cores [6], [8], [9].

2) includes circuitry to accurately and independently measure energy/power consumption of various parts of the microcontroller, including the processor core, PLL, memory, and I/O; this gives the ability to determine the most energy-consuming part for a given application;

3) is general and in view of an ARM-based COTS microcontroller; thus, it can be used for an extensive variety of existing microcontrollers (e.g., [8], [9], and [10]–[11]) and many other COTS devices. The paper is organised as follows: Section I is the introduction of the paper. Section II and section III contains literature survey and proposed methodology. Finally Section IV gives conclusion of the paper.

II. LITERATURE SURVEY

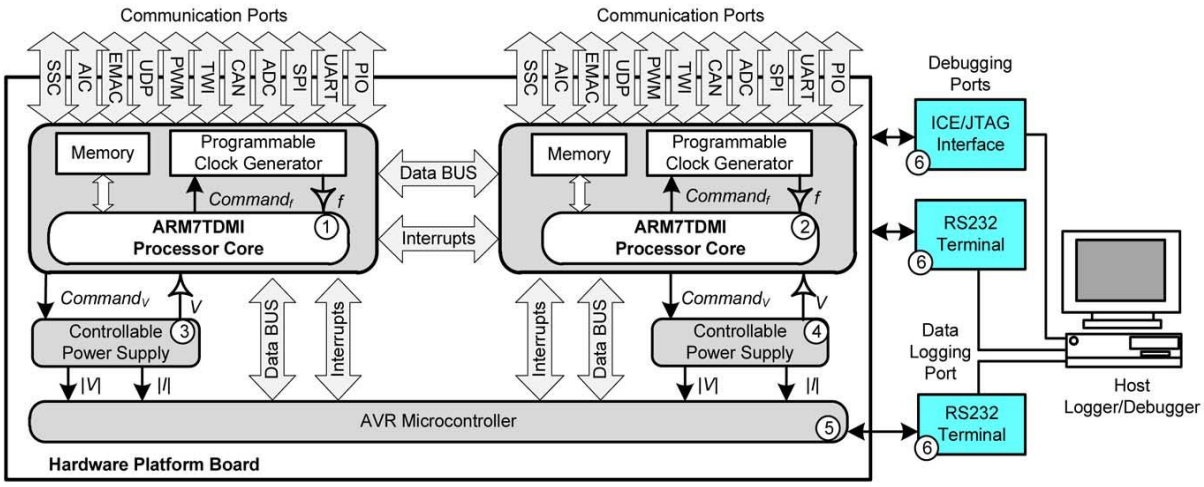
As the proliferation of ubiquitous computing environments becomes a reality, the requirement for high speed data processing and intelligent system management increases rapidly. Specifically, the requirement for low-power designs and power-aware system management is getting stronger. While multicore systems are deployed in many embedded system areas, an effective power management technique for multicores is not accessible yet. They propose a novel power management technique based on a parallel programming model. OpenMP is a well-known programming paradigm for shared memory multicore systems. We implemented this technique by adding capabilities in an OpenMP-compliant compiler and conducted experiments with various benchmarks. We wer could decrease the power consumption by 18% on average compared to other conventional power management methods[7].

They introduce analytical models for energy utilization and reliability. They additionally propose to use Markov models to acquire systematic models for reliability and energy consumption[2]. Embedded systems usually consist of a microcontroller that contains a microprocessor integrated with memory elements and peripherals in a single chip [3]–[5]. Reference [4] has reported a laboratory activity on a microcontroller-based platform. Reference [13]has presented a prototyping platform for ARM-based embedded systems. In any case, these platforms don't give facilities to experiment with energy management techniques. Reference [12] has presented a platform for dynamic voltage and frequency scaling (DVFS) [6] in an ARM-based processor. Be that as it may, this work exploits DVFS just for the processor (and not for the other parts, e.g., phase-locked loop (PLL), memory, and I/O).

III. PROPOSED SYSTEM

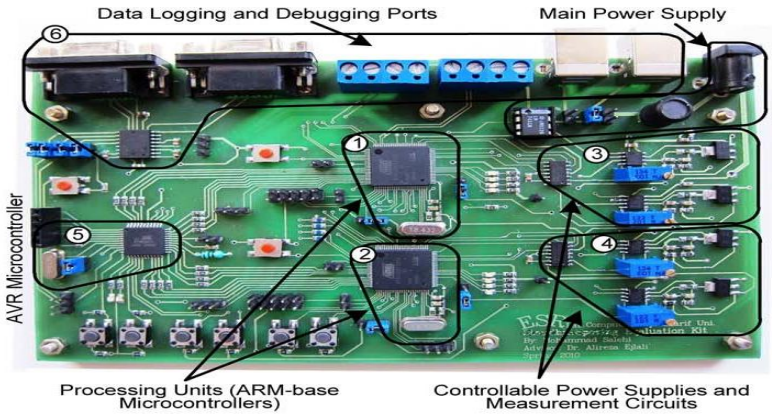
3.1. Hardware platform design

The architecture and physical implementation of the hardware platform are shown in Fig. 1(a) and (b), separately.



(a)

Fig (a)



(b)

Fig (b)

Fig. 1 Hardware platform. (a) Block diagram. (b) Implementation.

The architecture and physical implementation of the hardware platform. The platform contains two AT91SAM7x256 microcontrollers connected via a bus. ARM7TDMI is the most broadly used COTS processor incontemporary embedded systems because it is a low-cost, high performance, and versatile processor Based on the facilities gave by AT91SAM7x series, this bus can be easily configured as SPI, UART, CAN, or a 16-bit parallel bus. AT91SAM7x256 contains an ARM7TDMI processor with in-circuit emulation (ICE), debug communication channel support, 64-KB internal SRAM, and 256-KB internal Flash memory. Two controllable power supplies are incorporated into the board to provide power to the peripherals and the processor core of

each of the microcontrollers. Flash memory devices, and I/O peripherals. By the use of the measured current and the supply voltage of each part of the microcontrollers (the voltages are set by the controllable power supplies and reported to the measurement unit), the power consumption of each part is obtained. Furthermore, the execution time of applications running by the processors is reported to measure the consumed energy. The use of independent supply voltages not only helps conduct experiments with different DVFS schemes (where different supply voltages can be applied to each processor independently) but also can be utilized to shut off one processor to switch into a single-processor configuration.

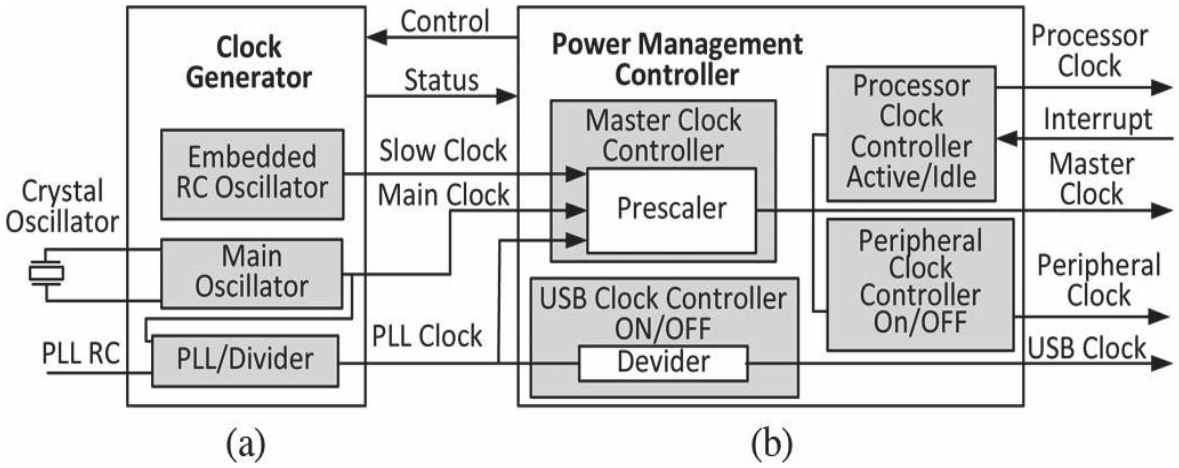


Fig. 2.Power management unit. (a) Clock generator. (b) Power management controller.

3.2. Energy Management Units

To manage the energy consumption, DVFS [6] and DPM [7] have been viably used. DVFS varies the components' voltage and, subsequently, frequency based on the system workload and other run-time factors. DPM selectively turns off the system components when they are idle.

3.2.1. DPM

AT91SAM7x (like many microcontrollers such as [10]–[11]) only supports DPM (just controls the processor and peripheral clocks) and can't exploit DVFS (does not give variable supply voltage to its processor core and peripherals). The AT91SAM7x enhances power consumption by controlling (enabling/disabling or scaling) the clock of processor and peripherals. The block diagram of the power management controller is appeared in Fig. 2(b). It uses the clock outputs [see Fig. 2(a)] to supply clocks to the processor, USB, peripherals, and master clock, which is the clock provided to the memory controller and all the peripherals.

The processor power consumption can be lessened by turning off the processor clock when it enters to idle mode while waiting for an interrupt. After resetting the device or by any interrupt, the processor clock is automatically re-enabled. To decrease the power of each peripheral, the user can individually enable and disable the peripheral clock by controlling the master clock on each peripheral by the use of the peripheral clock controller.

3.2.2. DVFS

DPM normally has only two operational states for systems components, namely active and idle. The active power utilization of a clock-enabled component can be determined by its operating frequency and supply voltage, as denoted by P_{Active} , as [1]

$$P_{Active} = I_{Leakage}V + C_{eff}V^2 f \quad (1)$$

where $I_{Leakage}V$ is the static leakage power, and $C_{eff}V^2 f$ is the dynamic power consumption (C_{eff} is the effective switched capacitance). The dynamic power consumption can be efficiently eliminated by putting the component into the idle state by disabling the clock.

frequencyscalingfor system components can be utilized to exploit idle times for power saving. The active energy consumed by executing a task with N cycles at frequency f can be computed as $P_{Active}N/f$. As a result, although frequency scaling reduces the dynamic power consumption straightly, it has no impact on the static leakage power consumption. Voltagescalingtechniques employ software-controlled adjustable voltage regulators to set the supply voltage of the processor core and clock-enabledcomponents. Software-controlled clock generators and voltage regulators allow the system to use DVFS. The basic idea behind DVFS techniques is to determine the minimum frequency that satisfies all timing constraints and then to adjust the lowest possible voltage that allows this speed.

3.2.3. Power Measurement Unit

To provide power measurement equipment to the platform, a resistor is set between each microcontroller power pin and the power supply line, and the voltage drop across the resistor is measured. The measured value gives the current drawn by the power pin. The power measurement setup is shown in Fig. 3. As the current drawn by the power pins of the microcontroller is less than 100 mA and this value cannot be digitized by the ADC of microcontrollers, the voltage value is amplified using an operational amplifier. The amplified value is digitized by a 10-bit ADC, and the data are sent to the host computer.

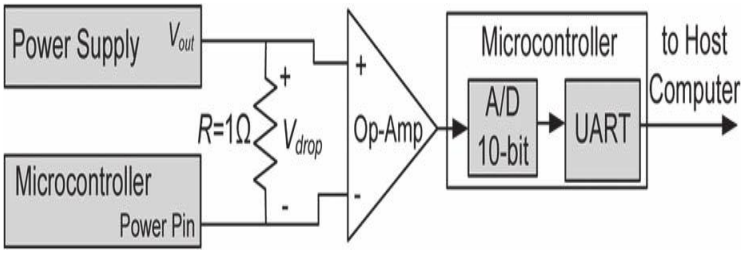


Fig. 3.Power measurement setup.

For instance, the platform can be utilized to experiment with fault-tolerance techniques as a direction for future work by the use of these facilities.

1) The two microcontrollers are connected such that they can interrupt, restart, and turn on/off each other.

2) Each of the microcontrollers can get the internal parts of the other via JTAG. This is useful to implement fault detection mechanisms that require comparing parts of a processor with their correspondents in the other one.

3) There are interconnections to transfer data, internal states, and checkpoints between the microcontrollers.

4) A third smaller microcontroller is placed in the platform that can be utilized to implement fault-tolerance techniques. These facilities provide the possibility of implementing fault tolerance techniques such as standby sparing [1].

IV. CONCLUSION

This paper has exhibited a hardware platform that consists of two ARM-based microcontrollers, each fed independently by variable voltages. Low energy consumption and fault-tolerance are two major objectives in

designing hard real-time embedded systems. In this platform, we give DVFS ability for the whole microcontroller (including the processor core, PLL, memory, and I/O). Physical experiments demonstrate that applying DVFS on the whole microcontroller is extensively more proficient in diminishing power/energy consumption compared with applying DVFS only on the processor core or using power-down policies that are currently used by most embedded processors. Although the platform is intended for ARM-based microcontrollers, it is general, and other COTS devices and embedded platform.

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