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ROBOTIC SENSOR: CONTACT AND NON-CONTACT SENSOR

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ABSTRACT

Robots are widely used in any industries and play a major role in manufacturing. Sensors are most important component of robots to determine actual values of parameters of interest. This paper deals with the Sensing and Control system to allow the robot to move around its environment, using Ultrasound Sensors to detect obstacles. Sensors used in robots provide intelligence to the robot and improve their performance.

Keywords: Robot, Robotic Sensor, Contact Sensor, Non-Contact Sensor

I. INTRODUCTION

In industries, robots are widely used and a sensor makes the working of a robot very effective. Sensors are able to obtain data from the interaction between robotic hands and their environment. It is very difficult for a robot, without sensor to sense the existence of objects and its actual parameter of interest to perform the various tasks such as for pick and place an object. A human is able to find a specified object by sensing it and this human sensing is done by their brain and past experiences. To operate a robot effectively it is necessary to provide them sensor and vision system to sense a object and about its parameter to perform the job. Robot sensing is a very tedious job because it required teaching the robot. Robotic sensors are used in robotic system for a variety of tasks such as to detect the work piece, its existence and obstacles present in the environment.

Greater use of sensors and more intelligence should lead to a reduction of this uncertainty and because the machines can work 24 hours a day, should also lead to higher Productivity [1]. A sensor is a type of transducer. The definition of sensor according to the Instrument Society of America is “A device which provides a usable output in response to a specified measure and”. Here the output is an ‘electrical quantity’ and measure and is a ‘physical quantity, property Or condition which is measured’ [2]. Robotic sensor may be contacting (tactile) or non-contacting type. Contact sensor detect the change in position, acceleration, force, torque etc. at the end effecter, whereas non-contacting sensor detect presence, distance, features of work piece etc.

II. MOBILE ROBOTIC SENSOR

Robotics has come a long way, especially for mobile robots. In the past, mobile robots were controlled by heavy, large, and expensive computer systems that could not be carried and had to be linked via cable or wireless devices. Today, however, we can build small mobile robots with numerous actuators and sensors that are controlled by inexpensive, small, and light embedded computer systems that are carried on-board the robot

[3]. Mobile robots are designed to move from one place to another. Wheels, tracks, or legs allow the robot to traverse a terrain. Mobile robots may also feature an arm like appendage that allows them to manipulate objects. Of the two stationary or mobile the mobile robot is probably the more popular project for hobbyists to build [4].

III. CONTACT OR TACTILE SENSORS

Contact sensor uses transducer for the sensing operation. Some mostly used sensors are potentiometer, strain gauge etc. Contact or touch sensors are one of the most common sensors in robotics. These are generally used to detect a change in position, velocity, acceleration, force, or torque at the manipulator joints and the end-effecter. There are two main types, bumper and tactile. Bumper type detect whether they are touching anything, the information is either Yes or No. They cannot give information about how hard is the contact or what they are touching. Tactile sensor are more complex and provide information on how hard the sensor is touched, or what is the direction and rate of relative movement. [5]

Tactile sensors that measure the touch pressure rely on strain gauges or pressure sensitive resistances. Variations of the pressure sensitive resistor principle include carbon fibers, conductive rubber, piezoelectric crystals, and piezodiodes [6, 7]. These resistances can operate in two different modes: The material itself may conduct better when placed under pressure, or the pressure may increase some area of electrical contact with the material, allowing increased current flow. Pressure sensitive resistors are usually connected in series with fixed resistances across a DC voltage supply to form a voltage divider. The fixed resistor limits the current through the circuit should the variable resistance become very small. The voltage across the pressure variable resistor is the output of the sensor and is proportional to the pressure on the resistor. The relationship is usually non-linear, except for the piezodiode [6,7], which has a linear output over a range of pressures. An analog to digital converter is necessary to interface these sensors with a computer. Different contact sensing as [8] are:

(1). Touch and force sensing.

(2). Proximity or displacement sensing.

(3). Slip sensing.

3.1 Three Axis Tactile Sensor

Three-axis tactile sensors as et al [9] the robotic hand was composed of two robotic fingers equipped with three axis tactile sensors. Using the robotic hand, it was found that tri-axial tactile data generated the trajectory of the robotic fingers, even if a simple initial trajectory was provided for the control program. In the verification test, the robotic hand screwed a bottle cap to close it. The tactile sensor is composed of a CCD camera, an acrylic dome, a light source, and a computer as shown in Fig. 1. The light emitted from the light source is directed into the acrylic dome. Contact phenomena are observed as image data, which are acquired by the CCD camera and transmitted to the computer to calculate the three-axis force distribution. The sensing element presented in this paper is comprised of a columnar feeler and eight conical feelers. The sensing elements, which are made of silicone rubber, are designed to maintain contact with the conical feelers and the acrylic dome and to make the columnar feelers touch an object. [10].

When the three components of the force vector, Fx , Fy , and Fz , are applied to the tip of the columnar feeler, contact between the acrylic dome and the conical feelers is measured as a distribution of gray-scale values, which are transmitted to the computer. Fx , Fy , and Fz values are calculated using integrated gray-scale value G and the horizontal displacement of the centric of gray-scale distribution. We are currently designing a multi-

fingered robotic hand for general-purpose use in robotics. The robotic hand includes links, fingertips equipped with the three-axis tactile sensor, and micro actuators (YR-KA01-A000, Yasukawa). Each micro actuator, which consists of an AC servo-motor, a harmonic drive, and an incremental encoder, is particularly developed for application to a multi-fingered hand. Since the tactile sensors must be fitted to a multi-fingered hand, we are developing a fingertip that includes a hemispherical three-axis tactile sensor [9, 11]

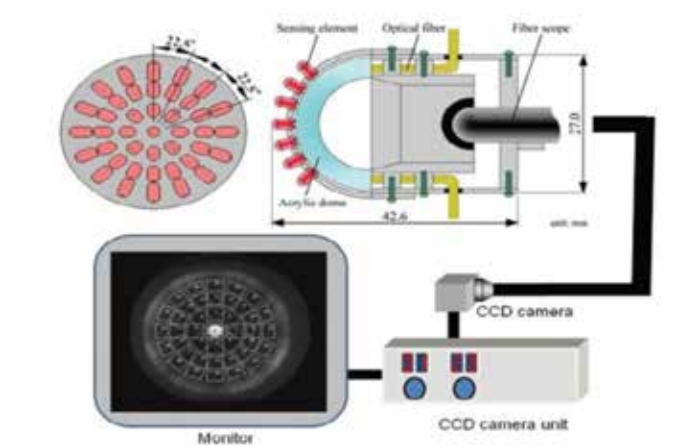

Fig. 1 Three-Axis Tactile Sensor System [10]

Fig. 2 Two-hand-arm robot equipped with optical three axis tactile sensor [10].

IV. NON-CONTACTING SENSOR

Non-contacting sensors are also a very important type of sensor, which detect parametric information about the environment of the object. It is used to detect the existence, distance and features of the object.

There are mainly six types of non-contacting sensor are as [8]:

(1). Visual and optical sensor.

(2). Magnetic and inductive sensor.

(3). Capacitive sensor.

(4). Resistive sensor.

(5). Ultrasonic and sonar sensor.

(6). Air pressure sensor.

Visual and optical sensors operate by transforming light into an electrical signal. The photo detectors can be as simple as a single photo diode or as complex as a television camera. With stereo cameras, robotic vision systems are analogous to the human sense of sight. [8].

Magnetic sensor is a type of non-contacting sensor which converts the magnetic energy into electrical signal. By this electrical signal it is able to determine the velocity, proximity of any metallic object.

Capacitive sensor is similar to magnetic sensor. The most common capacitive probes are flat disks or flat metal sheets. Probes are electrically isolated from their housings by guard electrodes insuring that the electric field produced is perpendicular to the sensor. Systems can make measurements in 100 microseconds with resolutions of 1/10 of a micron, and probe diameters range from thousandths of an inch to several feet [12].

Resistive sensing determines the distance between a robot arc welder and the welding seam. This sensing is done by means of varying resistance of the welding are. Figure 3 shows the basic technique for through the arc position sensing.

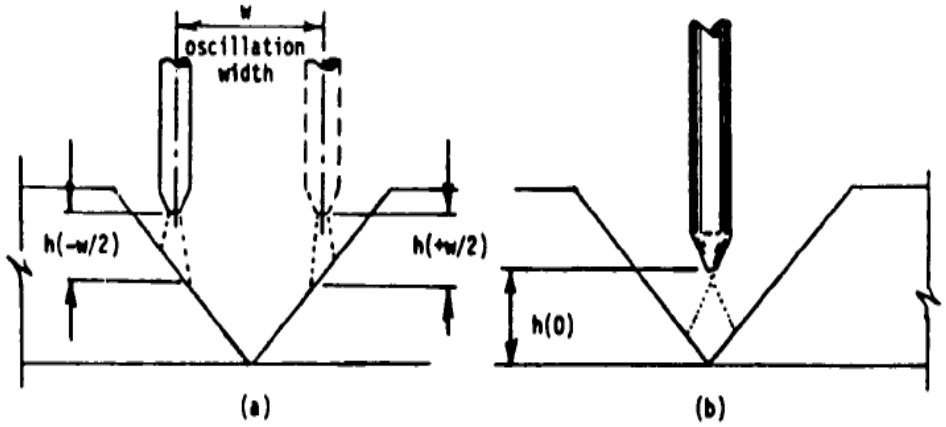

Fig.3 Welding Technique For Through he Arc Sensing [13].

Ultrasonic and sonar sensors are detected position, velocity, orientation etc. using high frequency acoustic waves.

V. CONCLUSION

It is concluded that, robotic sensor is the most important device for a robot to perform various tasks. Sensor makes the working of a robot very effective, which is able to obtain information from the interaction between robotic hand and their environment. Sensors used in robots provide intelligence to the robot and improve their performance. To operate a robot effectively it is necessary to provide them sensor and vision system to sense a object and about its parameter to perform the job. Robotic sensor may be contacting (tactile) or non-contacting type. Contact sensor detect the change in position, acceleration, force, torque etc. at the end effecter, whereas non-contacting sensor detect presence, distance, features of work piece etc. contact sensing may be of various types such as, touch and force sensing, proximity or displacement sensing, slip sensing. Non-contacting sensors are also of various types mainly six such as, visual and optical sensor, magnetic and inductive sensor, capacitive sensor, resistive sensor, ultrasonic and sonar sensor, air pressure sensor. A sensor can be choosing according to the requirement and the working environment of the robot.

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SCALABLE DATA SHARING IN CLOUD STORAGE USING KEY-AGGREGATE CRYPTOSYSTEM

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ABSTRACT

Data sharing is an important functionality in cloud storage. In this paper, we show how to securely, efficiently, and flexibly share data with others in cloud storage. We describe new public-key cryptosystems that produce constant-size cipher texts such that efficient delegation of decryption rights for any set of cipher texts is possible. The novelty is that one can aggregate any set of secret keys and make them as compact as a single key, but encompassing the power of all the keys being aggregated. In other words, the secret key holder can release a constant-size aggregate key for flexible choices of cipher text set in cloud storage, but the other encrypted files outside the set remain confidential. This compact aggregate key can be conveniently sent to others or be stored in a smart card with very limited secure storage. We provide formal security analysis of our schemes in the standard model. We also describe other application of our schemes. In particular, our schemes give the first public-key patient-controlled encryption for flexible hierarchy, which was yet to be known.

Keywords: Cloud Storage, Data Sharing, Key-Aggregate Encryption, Patient-Controlled Encryption

I. INTRODUCTION

CLOUD storage is gaining popularity recently. In enterprise settings, there is a rise in demand for data outsourcing, which assists in the strategic management of corporate data. It is also used as a core technology behind many online services for personal applications. Nowadays, it is easy to apply for free accounts for email, photo album, file sharing and/or remote access, with storage size more than 25 GB (or a few dollars for more than 1 TB). Together with the current wireless technology, users can access almost all of their files and emails by a mobile phone in any corner of the world.

By using Key Aggregate Cryptosystem, we can generate unique aggregate keys for a single file or multiple files. In existing system, they generate unique keys for a single file, but in this paper, we propose aggregate key for multiple files. Data sharing is an important functionality in cloud storage. For example, bloggers can let their friends view a subset of their private pictures, an enterprise may grant her employees access to a portion of sensitive data. The challenging problem is how to effectively and efficiently share encrypted data. Of course users can download the encrypted data from the storage, decrypt them, then send them to others for sharing, but it loses the value of cloud storage. Users should be able to delegate the access rights of the sharing data to others so that they can access these data from the server directly. However, finding an efficient and secure way to share partial data in cloud storage is not trivial. Below we will take Dropbox as an example for illustration.

Assume that Alice puts all her private photos on Dropbox, and she does not want to expose her photos to everyone. Due to various data leakage possibility Alice cannot feel relieved by just relying on the privacy protection mechanisms provided by Dropbox, so she encrypts all the photos using her own keys before uploading. One day, Alice's friend, Bob, asks her to share the photos taken over all these years which Bob appeared in. Alice can then use the share function of Dropbox, but the problem now is how to delegate the decryption rights for these photos to Bob. A possible option Alice can choose is to securely send Bob the secret keys involved. Naturally, there are two extreme ways for her under the traditional encryption paradigm. Alice encrypts all files with a single encryption key and gives Bob the corresponding secret key directly. Alice encrypts files with distinct keys and sends Bob the corresponding secret keys. Obviously, the first method is inadequate since all unchosen data may be also leaked to Bob. For the second method, there are practical concerns on efficiency. The number of such keys is as many as the number of the shared photos, say, a thousand. Transferring these secret keys inherently requires a secure channel, and storing these keys requires rather expensive secure storage. The costs and complexities involved generally increase with the number of the decryption keys to be shared. In short, it is very heavy and costly to do that.

Encryption keys also come with two flavors—symmetric key or asymmetric (public) key. Using symmetric encryption, when Alice wants the data to be originated from a third party, she has to give the encrypter her secret key. Obviously, this is not always desirable. By contrast, the encryption key and decryption key are different in public key encryption. The use of public-key encryption gives more flexibility for our applications. For example, in enterprise settings, every employee can upload encrypted data on the cloud storage server without the knowledge of the company's master-secret key. Therefore, the best solution for the above problem is that. Alice encrypts files with distinct public-keys, but only sends Bob a single (constant-size) decryption key. Since the decryption key should be sent via a secure channel and kept secret, small key size is always desirable. For example, we cannot expect large storage for decryption keys in the resource-constraint devices like smart phones, smart cards or wireless sensor nodes. Especially, these secret keys are usually stored in the tamper-proof memory, which is relatively expensive. The present research efforts mainly focus on minimizing the communication requirements (such as bandwidth, rounds of communication) like aggregate signature [5]. However, not much has been done about the key itself.

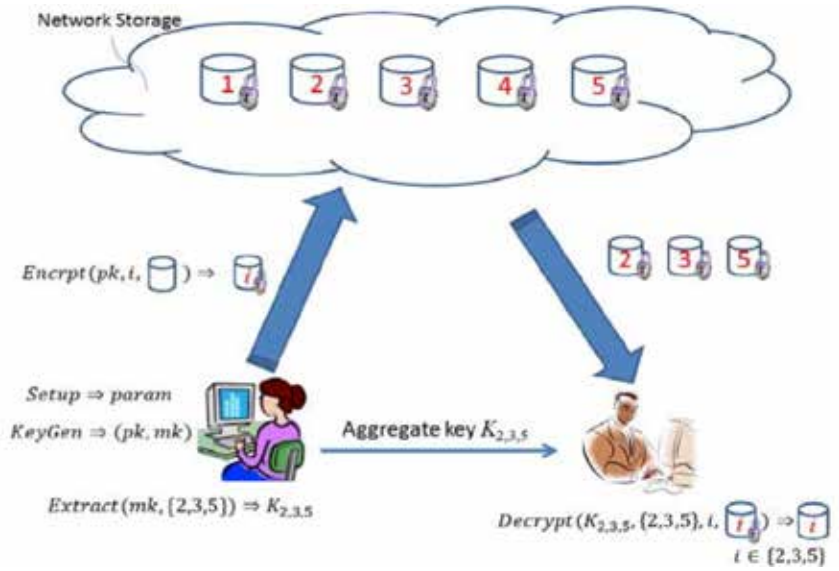

Fig 1: Using KAC for Data Sharing in Cloud Storage

II. KEY-AGGREGATE ENCRYPTION

In this paper, we study how to make a decryption key more powerful in the sense that it allows decryption of multiple cipher texts, without increasing its size. Specifically, our problem statement is:

"To design an efficient public-key encryption scheme, this supports flexible delegation in the sense that any subset of the cipher texts (produced by the encryption scheme) is decryptable by a constant-size decryption key (generated by the owner of the master-secret key)."

We solve this problem by introducing a special type of public-key encryption which we call key-aggregate crypto system (KAC). In KAC, users encrypt a message not only under a public-key, but also under an identifier of cipher text called class. That means the cipher texts are further categorized into different classes. The key owner holds a master-secret called master-secret key, which can be used to extract secret keys for different classes. More importantly, the extracted key have can be an aggregate key which is as compact as a secret key for a single class, but aggregates the power of many such keys, i.e., the decryption power for any subset of cipher text classes. With our solution, Alice can simply send Bob a single aggregate key via a secure e-mail. Bob can download the encrypted photos from Alice's Dropbox space and then use this aggregate key to decrypt these encrypted photos. The scenario is depicted in Fig. 1.

A key-aggregate encryption scheme consists of five polynomial-time algorithms as follows. The data owner establishes the public system parameter via Setup and generates a public/master-secret3 key pair via KeyGen. Messages can be encrypted via Encrypt by anyone who also decides what cipher text class is associated with the plaintext message to be encrypted. The data owner can use the master-secret to generate an aggregate decryption key for a set of cipher text classes via Extract. The generated keys can be passed to delegates securely (via secure e-mails or secure devices) finally, any user with an aggregate key can decrypt any cipher text provided that the cipher text's class is contained in the aggregate key via Decrypt.

- **Setup (1^{λ}, n):** Executed by the data owner to setup an account on an untrusted server. On input a security level parameter 1^{λ} and the number of cipher text classes **n** (i.e., class index should be an integer bounded by 1 and **n**), it outputs the public system parameter param, which is omitted from the input of the other algorithms for brevity.
- **KeyGen**: executed by the data owner to randomly generate a public/master-secret key pair (pk, msk).
- **Encrypt (pk, i, msk):** executed by anyone who wants to encrypt data. On input a public-key **pk**, an index i denoting the cipher text class, and a message **m**, it outputs a cipher text **C**.
- **Extract (msk, S):** executed by the data owner for delegating the decrypting power for a certain set of cipher text classes to a delegatee. On input the master-secret key msk and a set **S** of indices corresponding to different classes, it outputs the aggregate key for set **S** denoted by KS.
- **Decrypt (KS, S, I, C):** executed by a delegatee who received an aggregate key KS generated by **Extract**. On input KS, the set **S**, an index i denoting the cipher text class the cipher text **C** belongs to, and **C**, it outputs the decrypted result m if **I € S.**

III.RELATED WORK

[1] In a proxy re-encryption (PRE) scheme, special information is given to the proxy that allows it to translate a cipher text under one key into a cipher text of the same message under a different key. The proxy did not learn

anything about the messages that was encrypted under either key. PRE schemes have many practical applications, including distributed storage, email, and DRM.

[2] This paper proposed a new variant of PRE, named TR-CPBRE, which achieves conditional delegation, broadcast re-encryption and timed-release property simultaneously. In this paper for the first time they introduced a new notion Timed Release Conditional Proxy Broadcast Re-Encryption (TR-CPBRE).We also showed that our scheme can be proved IND-sID-CCA secure in the random oracle model under the (P; Q; f)-GDDHE assumption. This paper also motivates some interesting open problems, for example, how to construct a CCA-secure TR-CPBRE scheme in the adaptive identity model, i.e. achieving IND-aID-CCA security.

[3] Users should be able to use the cloud storage without worrying about the need to verify its integrity. Thus, enabling public auditability for cloud storage is of critical importance so that users can resort to a third-party auditor (TPA) to check the integrity of outsourced data and be worry free. To securely introduce an effective TPA, the auditing process need not bring new vulnerabilities towards user data privacy, and need not introduce additional online burden to user. This paper proposed a privacy-preserving public auditing system for data storage security in cloud computing. They utilize the homomorphic linear authenticator and random masking to guarantee that the TPA would not learn any knowledge about the data content stored on the cloud server during the efficient auditing process, which not only eliminates the burden of cloud user from the tedious and possibly expensive auditing task, but also alleviates the users' fear of their outsourced data leakage.

[4] This paper, introduced a right approach to achieve anonymity in storing data to the cloud with publicly verifiable data-integrity in mind. This approach decouples the anonymous protection mechanism from the provable data possession mechanism via the use of security mediator (SEM). This solution not only minimizes the computation and bandwidth requirement of this mediator, but also minimizes the trust placed on it in terms of data privacy and identity privacy. The efficiency of the system is also empirically demonstrated. The distinctive features of this scheme also include data privacy, such that the SEM does not learn anything about the data to be uploaded to the cloud at all, and thus the trust on the SEM is minimized. In addition, this scheme extends their work with the multi-SEM model, which can avoid the potential single point of failure. Security analyses prove that this scheme is secure and efficient.

[5] An aggregate signature scheme is a digital signature that supports aggregation. Given n signatures on n distinct messages from n distinct users, it is possible to aggregate all these signatures into a single short signature. This single signature (and the n original messages) will convince the verifier that the n users did indeed sign the n original messages. This paper introduced the concept of an aggregate signature, present security models for such signatures, and gives several applications for aggregate signatures. They construct an efficient aggregate signature from a recent short signature scheme based on bilinear maps. Aggregate signatures are useful for reducing the size of certificate chains and for reducing message size in secure routing protocols such as SBGP. This paper also shows that aggregate signatures give rise to verifiably encrypted signatures. Such signatures enable the verifier to test that a given cipher text C is the encryption of a signature on a given message M. Verifiably encrypted signatures are used in contract-signing protocols. Finally, this paper shows that similar ideas can be used to extend the short signature scheme to give simple ring signatures.

IV. COMPARISION

In PRE scheme, previously proposed re-encryption schemes achieved only semantic security in contrast, applications often require security against chosen cipher text attacks. They propose a definition of security

against chosen cipher text attacks for PRE schemes, and present a scheme that satisfies the definition. Their construction is efficient and based only on the Decisional Bilinear Diffe-Hellman assumption in the standard model. It also formally captures CCA security for PRE schemes via both a game-based definition and simulation-based definitions that guarantee universally composable security.

In a Conditional Proxy Broadcast Re-encryption scheme, when compared with the existing CPBRE and TR-PRE schemes, this scheme not only requires less number of pairings and achieves better efficiency in communication, but also enables the delegator to make a fine-grained delegation of decryption rights to multiple delegatees without losing CCA security.

In privacy preserving public auditing scheme compared to previous one, considering TPA may concurrently handle multiple audit sessions from different users for their outsourced data files, this scheme further extend their privacy-preserving public auditing protocol into a multiuser setting, where the TPA can perform multiple auditing tasks in a batch manner for better efficiency. Extensive analysis shows that these schemes are provably secure and highly efficient.

In SEM scheme, previous methods either unnecessarily reveal the identity of a data owner to the untrusted cloud or any public verifiers, or introduce significant overheads on verification metadata for preserving anonymity. This paper proposed a simple, efficient, and publicly verifiable approach to ensure cloud data integrity without sacrificing the anonymity of data owners not requiring significant overhead. Specifically, we introduce a security-mediator (SEM), which is able to generate verification metadata (i.e., signatures) on outsourced data for data owners.

In Aggregate signature scheme, previous signature constructions using bilinear maps only required a gap Diffie-Hellman group (i.e., DDH easy, but CDH hard). The signature constructions in this paper require the extra structure provided by the bilinear map. These constructions are an example where a bilinear map provides more power than a generic gap Diffie-Hellman group.

V. CONCLUSION

How to protect users' data privacy is a central question of cloud storage. With more mathematical tools, cryptographic schemes are getting more versatile and often involve multiple keys for a single application. In this paper, we consider how to "compress" secret keys in public-key cryptosystems which support delegation of secret keys for different cipher text classes in cloud storage. No matter which one among the power set of classes, the delegatee can always get an aggregate key of constant size. Our approach is more flexible than hierarchical key assignment which can only save spaces if all key-holders share a similar set of privileges. Key Aggregate cryptosystem is an efficient method and it also reduces cost.

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ADVANCE DRIVER ASSISTANCE SYSTEM BY USING WIRELESS TECHNOLOGY

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ABSTRACT

Manufacturing automobiles to keep drivers safe and accident free while operating their vehicles is the need of the day. These technologies are known in the industry as Advance Driver Assistance. In order to reach this objective, human-centered design principles have to be considered. To avoid collision with unexpected obstacles, the vehicle uses ultrasonic range finders for detection and mapping. The direction system for monitoring driver's vigilance is presented. The level of vigilance is determined by integrating head movement parameters. The estimated parametric values are collected and analyzed every fixed time interval to provide a real-time vigilance level of the driver. Vehicles thefts are increasing, alarmingly around the world are being set for vehicle manufacturers to make their products more secure. Therefore, a system is made to provide vehicle security and doesn't allow unknown person to handle the vehicle.

I. INTRODUCTION

With the increasing adoption of ultrasonic sensor systems for accident control, cars have gained the ability to detect the speed and position of obstacles in front or behind the vehicle. In this paper, we will focus on the development of a specific active safety system, that of brake assistance. This will utilize sensor subsystem to extract informational cues about the vehicle, vehicle surround, as well as driver state. An analysis module will consider these inputs to access the need for braking and situational criticality, and will provide signals which can trigger appropriate alarms or can even be used to initiate automatic braking. In each of the figures, an intelligent vehicle is approaching a slow moving truck with different levels of awareness of the driver. At time=t1, the distance is not critical hence nor the braking is planned neither the buzzer is generated. At time=t2, it just warns the driver but does not brakes the vehicle. At time=t3, driver fails to apply brake and system apply them automatically.

In this paper, we focus on an important component specific to our example: estimating the orientation of a driver's head. A driver's field-of-view can be reasonably approximated from the pose of his head, which can unobtrusively monitored by an accelerometer (ADXL 335) .The 3-axis accelerometer attached to the transmitter side is used to recognize gestures (dynamic head positions) in x, y directions and postures (static head positions) in z direction. The head position in x, y direction indicates that the driver is in the sleep or tired mode and the transmitter section gives the alarm to the driver to be attentive and then if the head position is not straight then the signal is transmitted to the receiver to break the vehicle.

Today, vehicles have been an essential part of our daily life. Unfortunately, we are also facing the high possibility of vehicle theft. Car alarm systems are very popular these days. In our system, without the transmitter section car does not run. It is necessary that the driver must have the transmitter section to start the vehicle. In such way, the thieves won't be able to steal the vehicle.

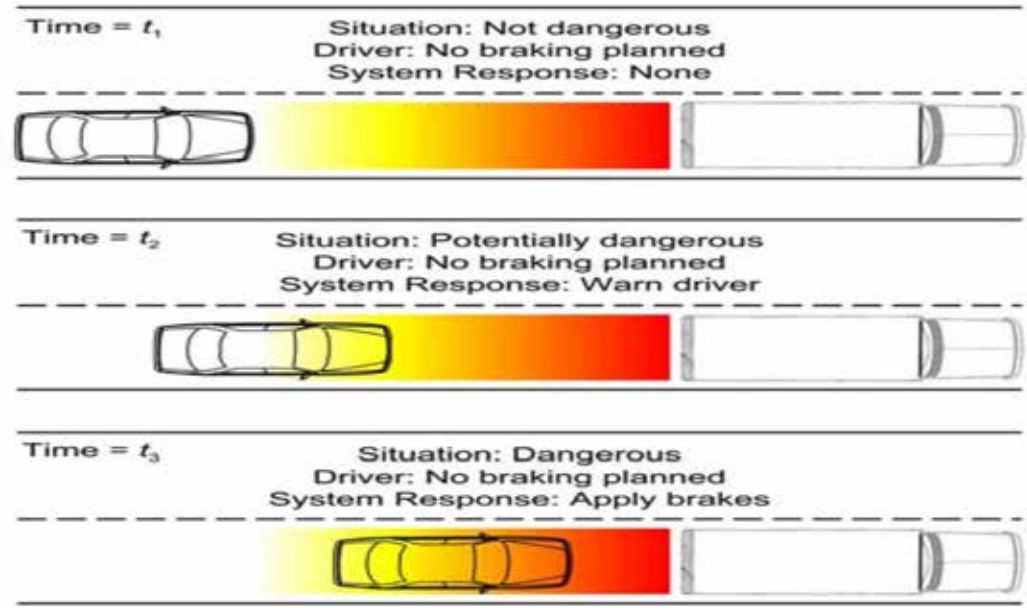

Fig1. Automated Braking System

1.1 MEMS Technique

MEMS has been identified as one of the most promising technologies from the 21st Century and has the potential to revolutionize both industrial and consumer products by combining silicon-based microelectronics with micromachining technology. Its techniques and micro system-based devices have the potential to dramatically affect of all of our lives and the way we live. MEMS deal with the emerging field of micro-electromechanical systems, or MEMS. MEM is a process technology used to create tiny integrated devices or systems that combine mechanical and electrical components. They are fabricated using integrated circuit (IC) batch processing techniques and can range in size from a few micrometers to millimeters. These devices (or systems) have the ability to sense, control and actuate on the micro scale, and generate effects on the macro scale.

II. BLOCK DIAGRAM

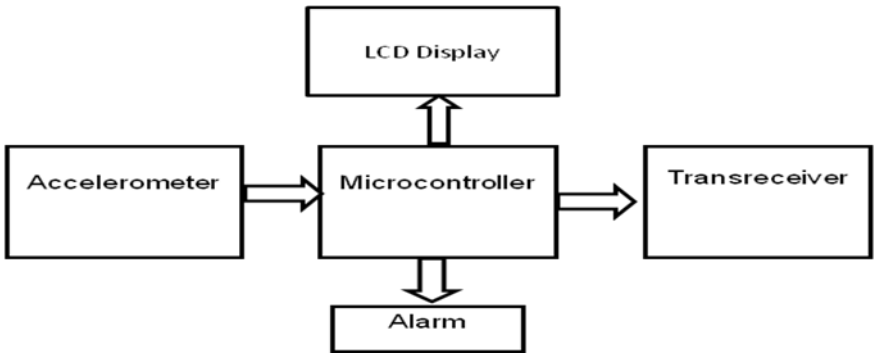

Fig2. Block Diagram of Transmitter

2.1 Working

Transmitter section consists of ATMEGA 16 microcontroller which is 40 pin DIL and with inbuilt ADC at port A. The 3 axis accelerometer is attached to the port A so that analog output is converted to digital form. The inclination of driver's head beyond the limit (x>400//x<320//y>400//y<320) gives an alarm to the driver to be attentive. If he fails to correct his position then after 2000msec the microcontroller will send the signal via cc2500 transreceiver which is at port D to the receiver side and then stops the vehicle gradually. The slowing

down of vehicle indicates that the driver is in the sleep mode and is not attentive. For the working of the microcontroller, ADXL335 and CC2500 5v is required which is given by 7805. Buzzer needs 12v to work hence L293D amplifier is used to amplify 5v to 12v.

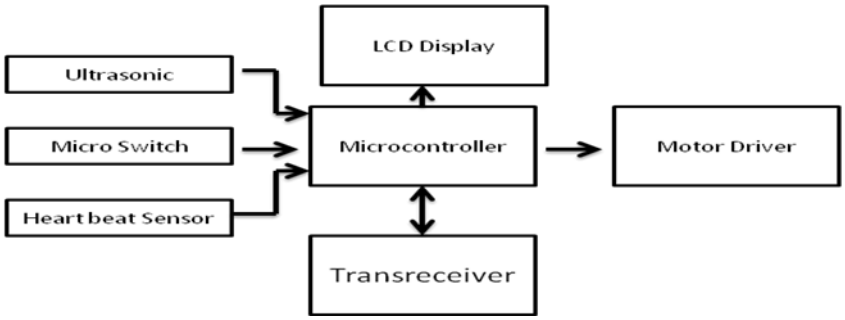

Fig3. Block diagram of receiver

2.2 Working

In the receiver section, LCD display is connected to the port B. It is a 16 pin IC used to show the indication like 'PLEASE WAKE UP'. Signal transmitted to the receiver section by the accelerometer shows that the driver is not attentive and slowly stops the vehicle. 4 pin ultrasonic sensors detect the range of few meters from the vehicle. If the distance between the two vehicles is dangerous then it gives alarm to the transmitter section and after few seconds if he fails to break the vehicle then the motor is stopped slowly.

III. HARDWARE DESCRIPTION

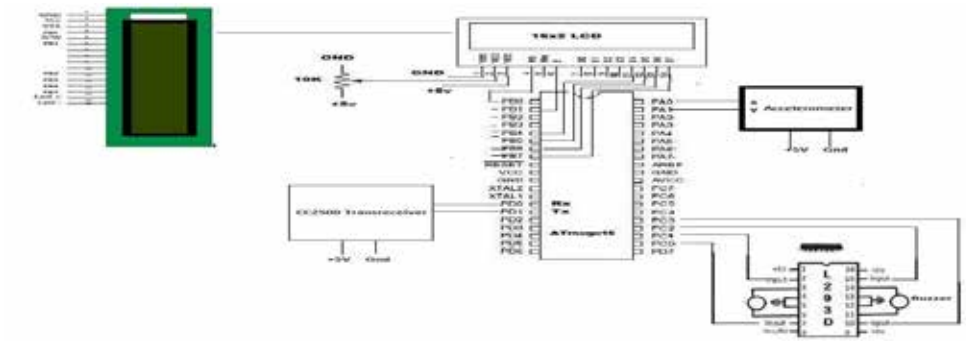

Fig4. Circuit Diagram of Transmitter

ATmega16 is a 40 dual in line IC with four ports A, B, C, D each containing 8 pin. Pin 40-pin 33 is port A with analog to digital converter inbuilt in it. Pin 32 is the analog pin for analog to digital converter and pin 30 is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to Vcc, even if the ADC is not used. If the ADC is used, it should be connected to Vcc through a low-pass filter. Three pins X, Y, Z of ADXL335 are connected to PA0-PA2 and two pins are connected to ground and vcc. Transreceiver CC2500 is the four pin IC Rx pin of CC2500 is connected to Tx (pin 15) of microcontroller and similarly Tx pin of CC2500 is connected to Rx (pin 14) of microcontroller. The other two pins of CC2500 are Gnd and Vcc. 7805 voltage regulator IC is used to give 5v supply to the entire circuit. Buzzer at port B requires more than 5v to generate high volume alarm so L293D IC is connected to amplify 5v.LCD display is interfaced with port B of microcontroller to show status result.

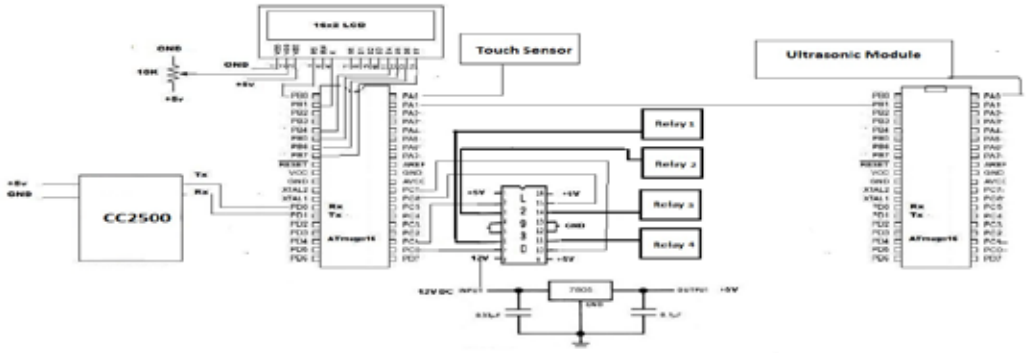

Fig5. Circuit Diagram of Receiver

The receiver section has two ATmega16 microcontrollers. L293D IC is connected to port D as an amplifier because the motor requires 12v to operate. Relays are connected to stop the reverse current coming back from motor. Ultrasonic sensor is connected to port A of second microcontroller. An ultrasonic car braking system includes; an ultrasonic wave emitter provided in a front portion of an automatic braking car producing and emitting ultrasonic waves frontward in a predetermined distance in front of the car. Ultrasonic receiver also formed in a front portion of the car operatively receiving a reflective ultrasonic wave signal as reflected by obstacles positioned within the pre-determined distance in front of the automatic braking car. LCD is interfaced with port A.

IV. WORKING

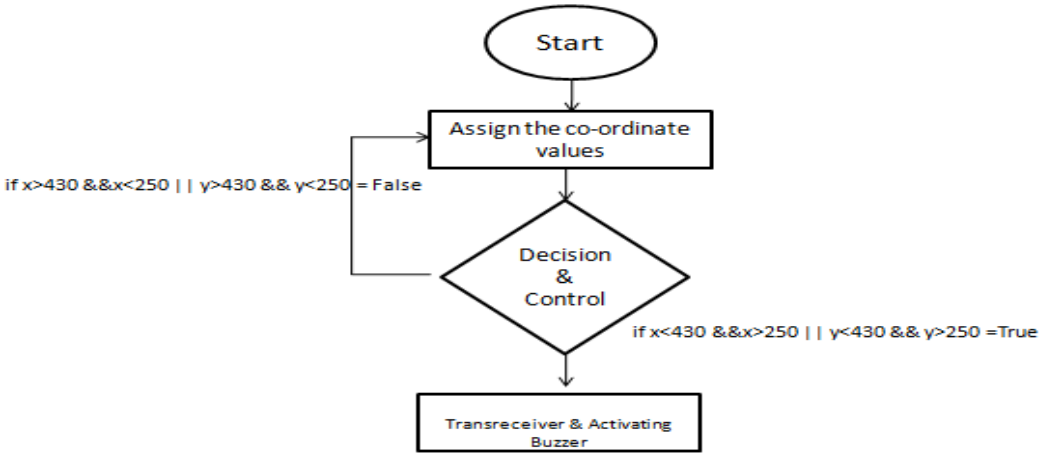

Fig6. Flow Chart of Transmitter

Transmitter section consists of ATmega16 microcontroller which is 40 pin DIL and with inbuilt ADC at port A. The 3 axis accelerometer is attached to the port A so that analog output is converted to digital form. The inclination of driver's head beyond the limit (x>430//x<250//y>430//y<250) gives an alarm to the driver to be attentive. If he fails to correct his position then after 2000msec the microcontroller will send the signal via CC2500 transreceiver which is at port D to the receiver side and then stops the vehicle gradually. The slowing down of vehicle indicates that the driver is in the sleep mode and is not attentive. For the working of the microcontroller, ADXL335 and CC2500 5v is required which is given by 7805. Buzzer needs more than 5v to generate the loud alarm hence L293D amplifier is used to amplify 5v to 12v.Heart beat sensor detects the pulse

of the driver. If the rate is normal then the receiver section starts the motor. Transmitter also gives security to vehicle as the only availability of it would give access to unlock the vehicle.

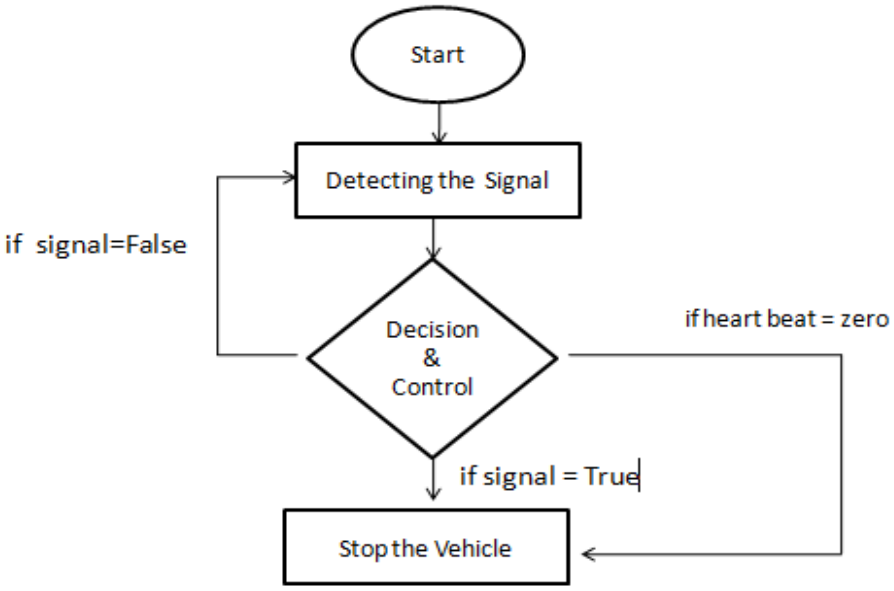

Fig7. Flow Chart of Receiver

In the receiver section, LCD display is connected to the port B. It is a 16 pin IC used to show the indication like 'START THE MOTOR' at the time of safe situation or 'STOP THE MOTOR' at the time of accidental situation. Signal transmitted to the receiver section by the accelerometer shows that the driver is not attentive and then the vehicle is stopped automatically. Four pin ultrasonic sensors detect the range of few meters from the vehicle. If the distance between the two vehicles is dangerous then it gives alarm to the transmitter section and after few seconds if he fails to brake the vehicle then the motor is stopped slowly. An ultrasonic car braking system includes; an ultrasonic wave emitter provided in a front portion of an automatic braking car producing and emitting ultrasonic waves frontward in a predetermined distance in front of the car. Ultrasonic receiver also formed in a front portion of the car operatively receiving a reflective ultrasonic wave signal as reflected by obstacles positioned within the pre-determined distance in front of the automatic braking car. The reflected wave (detection pulse) was measured to get the distance between the vehicle and the obstacle. Then microcontroller is used to control servo motor based on detection pulse information to push pedal brake to brake the car intermittently for automatically braking the car for a safe braking purpose.

V. RESULTS

- Results are obtained from the Accelerometer and then classified as driver is asleep or not based on their acceleration magnitude and power spectrum of the x, y, and z axis.
- The result shows the anti-collision braking system has substantial potential to reduce forward collision. It can also reduced rear-end collisions assuming the device is installed in all vehicles.
- Anti-theft sensor and pulse detection sensor also proves to be effective in limiting car theft as well as drivers physical state.

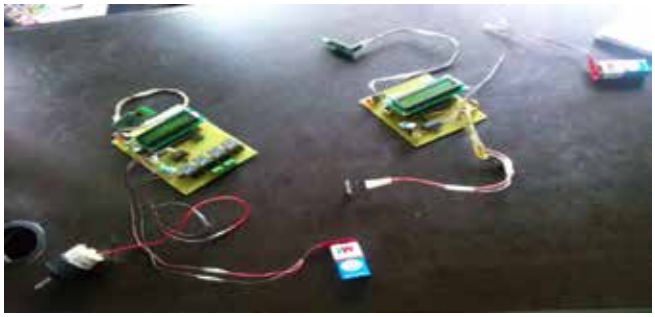

Fig8. Implemented Picture of Transmitter and Receiver

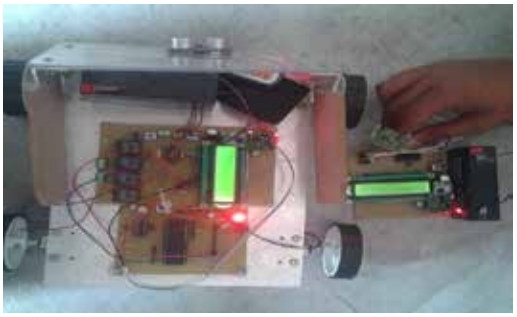

Fig9. Model Car

VI. CONCLUSION

We have been able to accomplish our baseline goals and implement some of our extras. Even though along the way we ran into many problems, our system was flexible enough to adapt to the problems we encountered. We were able to build a successful accident prevention unit. In the process we learned about functioning of the hardware and software. During the monitoring, the system is able to decide if the driver is asleep or not. If the driver is asleep system will issue a warning signal to the driver and vehicle will be stopped gradually. In addition, during monitoring, the system is able to automatically detect an obstacle and have ability to stop vehicle thus preventing accident.

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DESIGN ANALYSIS OF AREA EFFICIENT 4 BIT SHIFT REGISTER USING CMOS TECHNOLOGY

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ABSTRACT

In this paper a detailed area and power analysis of 4- bit shift register is carried out. Three methods are compared in terms of area and the method with least area requirement is suggested for the design. First method is by using DSCH software followed by generating the Verilog file and then compiling the same in Microwind software. The result will be an auto generated circuit of 4- bit shift register. The circuit is then simulated and the area is measured. Second method follows the implementation of 4 bit shift register using Microwind software by using the available P-MOS and N-MOS in the software. Circuit is simulated and the power is measured again. Third method involves the implementation of the circuit by generating our own N-MOS and PMOS transistors and then simulating the circuit and then measuring the area and then the final comparison of all is done.

Key Words: 4 bit shift register-P-MOS, N- MOS, flip flop, semiconductors

I.INTRODUCTION

The rapid growth in semiconductor device industry has led to the development of high performance portable systems with enhanced reliability [1]. In such portable applications, it is extremely important to minimize area [2] and current consumption due to the limited availability of battery power [1]. Therefore,area utilization,power dissipation becomes an important design issue in VLSI circuits[4][5].

In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. More generally, a shift register may be multidimensional, such that its“data in” and stage outputs are themselves bit arrays. This is implemented simply by running several shift registers of the same bit-length in parallel. Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in serial-out' (PISO). Shift registers produce a discrete delay of a digital signal or waveform. A waveform synchronized to a clock, a repeating square wave, is delayed by "n" discrete clock times where "n" is the number of shift register stages. Thus, a four stage shift register delays "data in" by four clocks to "data out". The stages in a shift register are delay stages, typically type "D" Flip-Flops or type "JK" Flip-flops. Formerly, very long (several hundred stages) shift registers served as digital memory. This obsolete application is reminiscent of the acoustic mercury delay lines used as early computer memory [6]. Serial data transmission, over a distance of meters to kilometres, uses shift registers to convert parallel data to serial form. Serial data communications replaces many slow parallel data wires with a single serial high speed circuit.

Some specialized counter circuits actually use shift registers to generate repeating waveforms. Longer shift registers, with the help of feedback generate patterns so long that they look like random noise, pseudo-noise.The suggested methods in this paper can be implemented for linear feedback shift registers [6] and in counters also.

Basic shift registers are classified [7]by structure according to the following types:

- Serial-in to Parallel-out (SIPO) - The register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

II.SHIFT REGISTER-WORKING

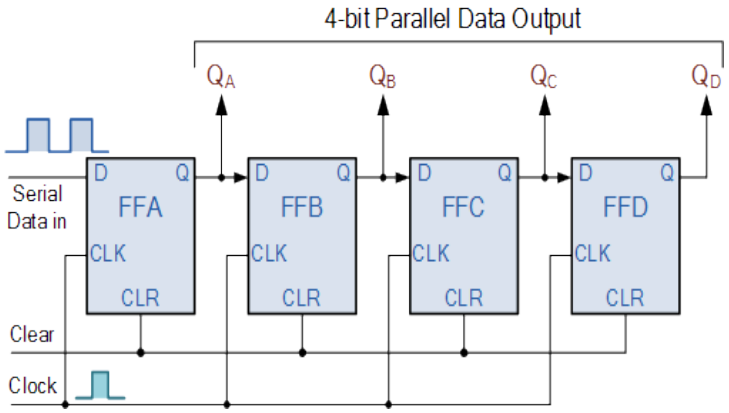

Fig1. 4-bit Serial-in to Parallel-out Shift Register[7].

The operation is as follows. Let's assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level "0" i.e., no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic "1" with all the other outputs still remaining LOW at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and Q_B HIGH to logic "1" as its input D has the logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_A.When the third clock pulse arrives this logic "1" value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D.Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from left to right as follows.

	CLK	$D_n = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	1	1	1	1	0
(iv)	↓	1	1	1	1	1

→ Direction of data travel

Table1. Basic Data Movement through A Shift Register

Note that after the fourth clock pulse has ended the 4-bits of data (0-0-0-1) are stored in the register and will remain there provided clocking of the register has stopped. In practice the input data to the register may consist of various combinations of logic “1” and “0”.

III. ANALYSIS OF LAYOUT USING THREE DIFFERENT TECHNIQUES

The first method is the designing of the ring counter in DSCH and generating its Verilog file. Now in Microwind this Verilog file is compiled and an autogenerated layout is created. We can select different foundries available in the library of Microwind software. Here the selected foundry is 90 nm. Figure2 represents this auto generated layout.

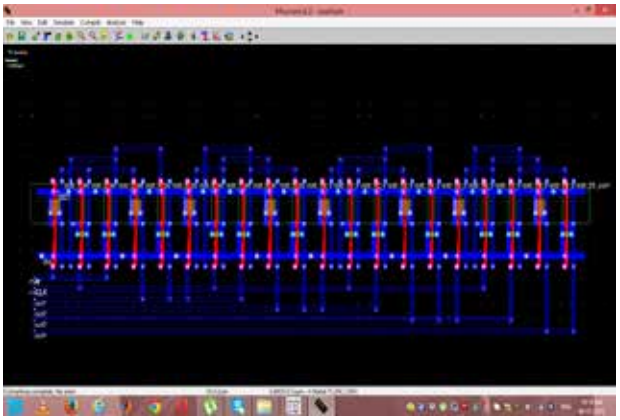

Figure 2. Auto Generated 4 bit shift register

This layout is checked for DRC and if there is no errorpresent in the layout then the layout is simulated. Theoutput of the simulation is checked and if the outputmatches the output of the 4 bit shit registerthen wefurther check the power and the area of this auto generated layout of 4- bit shift register. Figure 3 showsthe output of the 4 bit shift register. Also power canbe measured from the result of simulation.

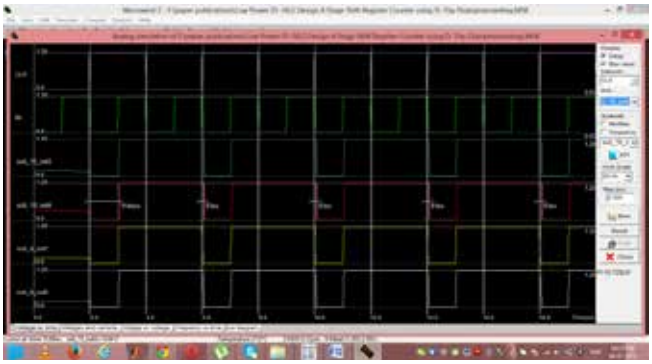

Figure 3. Output of Auto Generated 4 bit shift register

The measured power here is 10.725µW. The area consumed here is 251.1µm^2.Now the second step is to directly make use of in built transistors available in the Microwind software.In this method the connections are made by thedeveloper and hence there is a large possibility thatarea may get reduced. Figure 4 represents the layoutusing the in- built transistors i.e. N- MOS and PMOS.

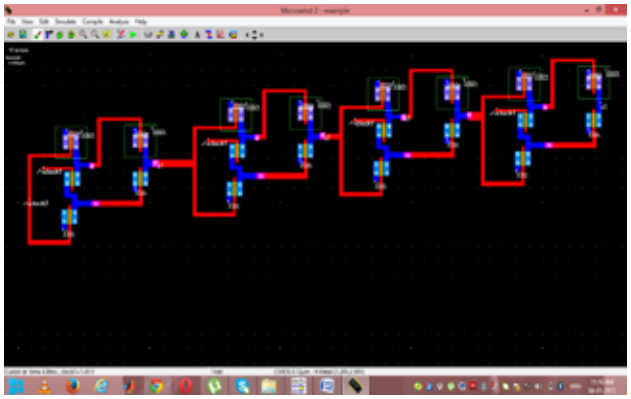

Figure 4. Layout of 4 bit shit register with in- built transistors

When the layout is ready it is again checked for DRCand if there is no error present in the layout, the circuitis simulated and the outputs are obtained. Theobtained output is verified with the truth table of 4 bit shift register. If the truth table is verified we canfurther check the power and area consumed by thissecond method. Figure 5 shows the output obtained bysimulating the above circuit.

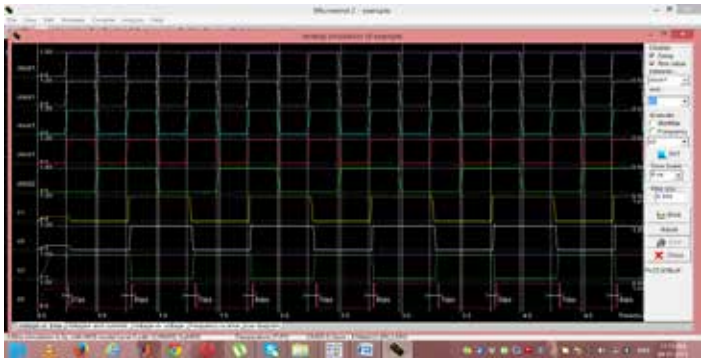

Figure 5.Outputs of 4 Bit Shift Register Using In- Builttransistors

Now check the results for power and area. Here thepower consumed is 24.003 µW. The area consumed bythis layout is 203.0 µm^2.The third method is to create our own N- MOS and PMOStransistors. Here the created transistors are made using palette. Here the area measured is 183.8µm.

This new layout is shown in figure 6.

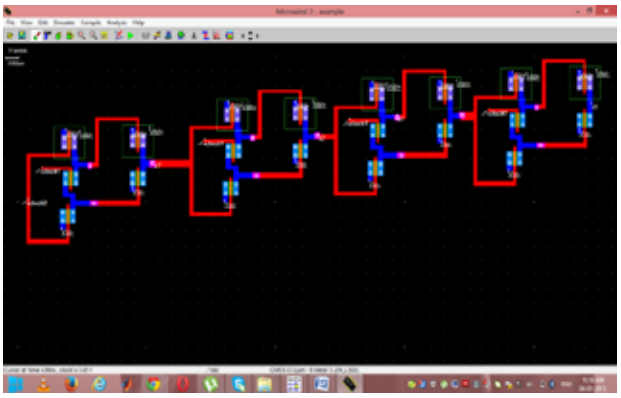

Figure 6. Layout of 4 Bit Shift Register Using Own Created NMOSAND P-MOS

IV. COMPARATIVE ANALYSIS

A comparative study can be done on analyzing the above results for power and area obtained by using three different methods.

TABLE 2: Comparative analysis of Power and Area

METHODS	POWER	AREA
Auto Generated Layout	10.725 µW	251.1µm^2
Layout using in-built transistors	24.003 µW	203.0µm^2
Layout using own created transistors	.279 mW	183.8µm^2

comparative analysis of this table shows that in terms of power, the layout generated using in- built transistors are increasing. But on the other hand in terms of area the auto generated layout is using more area in comparison to the layout using in- built transistors and the self created transistors. There is a reduction of 19.15% in area when auto generated layout is compared to layout using in- built transistors. When auto generated layout is compared to layout using self created transistors then there is a reduction of 26.8% in the area. Now when both the layout with inbuilt and self created transistors is compared in terms of area then there is a reduction of 9.4% in the area.

V. CONCLUSION

From the above analysis it can be said that the layout with self created transistors is more efficient in terms of area. So this design can be implemented in the applications where area reduction is the main consideration. Hence area is decreased at the cost of power. So it can be efficiently used for applications requiring minimum area.

VI. ACKNOWLEDGEMENT

The authors would also like to thank Director, National Institute of Technical Teachers‟ Training &Research, Chandigarh, India for their support during work.

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REVIEW ON HIGH TEMPERATURE APPLICATION COMPOSITES

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ABSTRACT

Composites are materials composed of at least two different solids, which exist as separate phases in the final material. thus a material can be manufactured to sustain at high temperature by combining the properties of two different solid in the form of composites. At higher temperature the driving force as thermal energy is more active due to more entropy thus ordinary exposed materials they starts to become soften consequently they may loose their property during service condition, therefore we need to look up one the combination of material in the form of composites. extensive research have been carried out in the field of aircraft industries body parts as they must possess the combination of strength and high temperature sustainability. Through this paper an attempt has been made to bring out the all research in the form of review to impart the knowledge of material and their applicability at the high temperature.

I. INTRODUCTION

1.1 History and Brief of Composites

All the engineering material obtained in this world has certain limitation i,e, metal, alloy, plastics because a single material can not possess all the desired properties of engineering application, due to which a concept off composite material comes into the exhistence. A composte is the mixture of two or more matters in fixed and calculated proportion to impart the specific property desired by the service condition, here combination of two properties performed by each matter combined will gives rise the desired property.

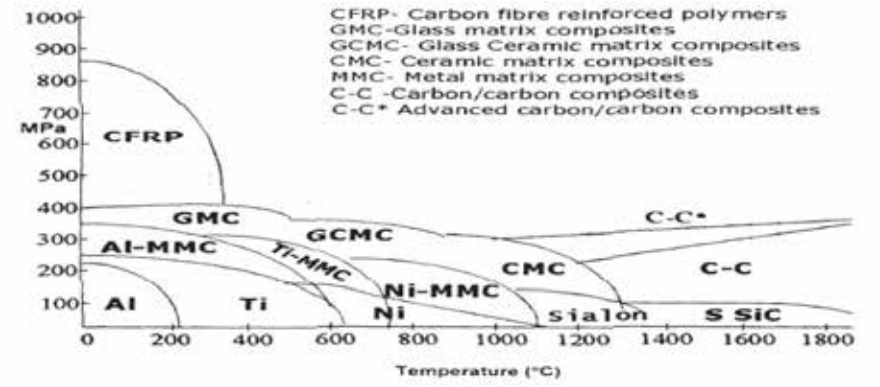
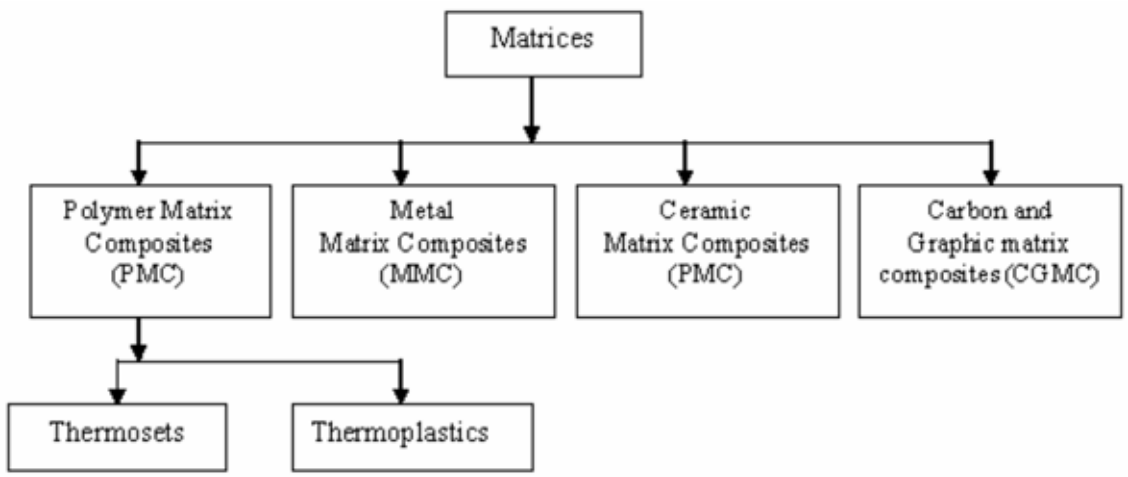


Fig 1 The Above Figure Shows The Sustainability of Different Material With Temperature,

Similarly the idea of composite material for higher temperature comes into the virtue. It is very difficult for the metal or alloy to sustain at the higher temperature because of their limited property and melting point due to which they become soft when exposed to high temperature usually above 1000°C. But the composite material with proper matrix and fibre can be utilized to achive the combination of two distinct properties required for higher temperature application. A composite material can be classified into three different categories usually:-

1. Metal matrix composites
2. Polymer matrix composites
3. Ceramic matrix composite



This classification is often on the basis of its matrix their might be several modes of classification, and to sustain at the higher temperature either the matrix or the fibre needs to be modified.

Composites cannot be made from constituents with divergent linear expansion characteristics. The interface is the area of contact between the reinforcement and the matrix materials. In some cases, the region is a distinct added phase. Whenever there is interphase, there has to be two interphases between each side of the interphase and its adjoint constituent. Some composites provide interphases when surfaces dissimilar constituents interact with each other. Choice of fabrication method depends on matrix properties and the effect of matrix on properties of reinforcements. One of the prime considerations in the selection and fabrication of composites is that the constituents should be chemically inert non-reactive.

"Advanced composites" or so-called "high performance composites" are mostly based on reinforcement by continuous fibres . Rarely short fibres and whiskers are used for this purpose, **The** best reinforcement is obtained by the use of continuous fibres with a volume fraction above 50 usually 60 % and strictly controlled geometric arrangement of the fibres within the composite (" tailored material"). **The** special case of fibre arrangement in one direction. i . s easy to understand and offers the possibility for pre calculation of the strength and stiffness of the composites using the rule of mixture (1) . The disadvantage of such u unidirectionall reinforced (UD) composites i s the strong dependence of the composite properties on the fibre direction. In practical application two dimensional reinforcement is applied with fibre arrangement in different directions. The reinforcement by short fibres or whiskers and is catastrophic distribution of the fibers lead to a reinforcement effect of 1/6 of the precalculated values using the rule of mixture.

In the Eighties this new material was used in commercial aircrafts already. It is applied for the vertical stabilizer in the Airbus A 310; at the moment the largest part of industrially produced carbon fibre reinforced composites. The present world wide use of carbon fibre s is in the order of 5.000 t o 10.000 tons per year with a stongly

increasing tendency. The expected broad application in surface transportation such as railways and cars in machinery, in pipelines s and apparates, i n sporting goods as well as in building materials was described in more detail last year here in Rome during the European Conference **on** Thermophysical Prop properties(2) . Most exciting for this material is the low energy need for raw material preparation in fabrication as compared with high energy consumption by conventional materials. There is however severe limitation for application of fibre reinforced polymer, that is the limitation in temperature caused by the softening or thermal decomposition of the polymers. The high temperature resistivity of the carbon fibre is not used by far in combination with the epoxy. For solving the future problem in aerospace and energy field, in industrialization in general and especially for the technology, composite for high temperature is needed.

1.2 What are the Needs at High Temperature Application

When we use the world high temperature that means we generally we take the temperature higher than the usual temperature i.e. above 800o C above which an epoxy resin cannot be utilized.

1.2.1 Light Weight

Any engineering material requires high specific strength i.e. strength to weight ratio thus strength with light weight is the primary concern for any material, take the example of aircraft industry, it is believed that 1kg reduction in weight can save the money in the order of 100 INR.

In supersonic aircrafts, for instance, the surface temperature can arise up to 500^{o}C that is a temperature range where no today's resin for fibre reinforced composites can withstand. In the space shuttle with surface temperatures above 1000 "C during the period of entering the earth atmosphere, this heat attack problem was solved by the use of thermal insulation bricks. On the tip cone and in the edges of the wings, however, the temperatures arose up t o 1500 "C. Here only carbon/carbon composites were applicable. The additional problem arising by this application is heat attack by the oxygen in the atmosphere and carbon materials without surface coating are not resistant against oxidation at those temperatures.

1.2.2 High Refractoriness

Refractoriness is the measure of ability of any material to withstand at the higher temperature, thus more will be the refractoriness more will be the high temperature sustainability.

1.2.3 Low Thermal Conductivity

A material with high thermal conductivity will conduct more, thus more heat transfer will takes place which is not desirable for high temperature application material, low thermal conductivity ensure the less heat transfer and thus the hightemperature sustainability will be more imparted.

1.2.4 Low Thermal Expansion

It is defined as the ability oof any material to retai its shape at high temperature working condition, this parameter for aircraft parts are specially considered as a little expansion while flight may cause the thin section at the expanded area which may lead to the ductile failure, and aircraft part may fail catastrophically to couse the fatal accidents.

1.2.5 High Temperature Corrosion

In addition to oxide ceramics, which include not only the SOFC materials along with new sensors and high temperature superconducting materials, silicon-based ceramics such as SiC, Si3N4, and sialons along with other borides, carbides, nitrides, silicides, and diamond and diamond-like materials are now common high temperature materials of scientific and technological interest in both bulk and coating configurations.[6]

II. AREA OF INNOVATIONS

2.1 High Performance Carbon–Carbon Composites

Carbon is a truly remarkable element existing as four allotropes, viz. diamond, graphite, carbynes and fullerenes, each having significant scientific and technological importance. Its most abundant allotrope, graphite, can take many forms with respect to microstructure, amorphous to highly crystalline structure, highly dense with density 2_2 g/cm3 to highly porous with density 0_5 g/cm3 and different shapes. These types of graphites are called synthetic carbons and in technical terms, engineered carbons. Examples are cokes, graphite electrodes, mechanical carbons, glassy carbons, carbon black, porous carbons, activated carbons, carbon fibres and composites etc.. Solid carbons are preferred for structural applications under extreme environmental conditions of temperature or corrosion (liquid as well as gaseous) etc. This is mainly because, theoretically, carbon materials with covalently bonded atoms possess very high specific strengths (40–50 GPa) and retain this strength at high temperatures in the temperature range over 1500_C (Ref 3).The strength and fracture of carbon/carbon composites are governed by the Cook–Gorden theory for strengthening of brittle solids (Cook & Gorden 1964), which states that if the ratio of the adhesive strength of the interface to the cohesive strength of the solid is in the right range, a large increase in strength and toughness of otherwise brittle material is achieved. Extensive work has been done in achieving highest possible translation of fibre properties in carbon/carbon composites.

2.2 Dielectromagnetic Composites for Microwave Applications

A lot of work has been done by Thanh Ba Do (Ref 4) according to him The combination of a ceramics with a polymer can be utilized because it provides a flexibility to control physical, dielectric, and magnetic properties of formulated composites. Advantages of this combination are lower costs, more facile processing, and low temperature production. Ceramics-polymer composites also contain properties that may not be present in their individual components

High-temperature composites are a major area of research today. Composite materials have been successfully used in many applications where temperature resistance is not an issue (i.e. exposed to temperatures under 300ºC), while helping reduce the weight of components and optimize their design.

2.3 Exhaust Ducts for Motorsports

An extensive work was done by Christopher buckler (Ref 5) on exhaust duct system for motorsports According to which Race car exhausts are complex systems where the use of composite was hardly thinkable less than 10 years ago.

Fig 2.3.1 Motorsport Duct Made of Composite Material

The elevated exhaust gas temperatures (600ºC to 1000ºC), part complexity and high levels of stress and vibration were major challenges that made Inconel or steel the only viable options for headers, collectors, mufflers and tailpipes. In 2006, Pyromeral Systems considered using Pyro Sic glass-ceramic matrix composites to manufacture composite components for exhaust systems, with the objective to reduce exhaust weight, improve thermal management, and give more flexibility to engineers when designing the components.

2.4 Heat Shields

Heat shields and fire barriers are important components of motorsports and aerospace systems. They are also one of the most difficult applications for traditional materials, especially when structural properties are also needed. Heat shields made of PyroSic are frequently used in motorsports applications, where the material has proven to be a reliable solution for lightweight structural heat shields located in tight spaces and exposed to both extreme heat (close to 800ºC in some areas) and high vibrations.

Fig 2.4.1 Heat Shield Made of Composite

The technical attributes of heat shields made of PyroSic glass-ceramic matrix composites include: - thin walls, typically ranging from 0.6 mm to 1.2 mm others are as follows.

1. possibility to design and manufacture complex shapes,
2. dimensional stability and absence of distortion, even in case of fast temperature increases,
3. no burn-through, even in case of fire,
4. possibility to combine the high-temperature composite with another composite to improve durability and mechanical performance (hybrid composites),
5. possibility to apply coatings to improve thermal management, e.g. reflective coatings for improved shielding against radiant heat.

III.FUTURE ASPECTS

Composite material retains the vast subject and its future is very bright due to combination of its properties desirable to any situation however right now we have a limited applicability of the same over the service condition. further research in the area of thermal conductivity of the composite material and its expansion at high temperature may lead to great advantages in the aircraft and high temperature exposure parts.

IV.CONCLUSION

Through this paper we finally reach to a conclusion that if any material has to withstand at high temperature then it requires certain specific properties, which if fulfilled than material can be withstand and composite material are one of them.

1. Modification of either matrix or the fiber reinforcement in the form of different refractory material can be selected to obtain the desired properties.

2. Reinforcement either in the form of particulates or the dispersed phase distribution can be altered to achieve the desired property.

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A BRIEF STUDY ABOUT ADVANCEMENT IN ROCKET NOZZLE USED IN AIRCRAFT SCIENCE

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ABSTRACT

Several nozzle concepts that promise a gain in performance over existing conventional nozzles are discussed in this paper. It is shown that significant performance gains result from the adaptation of the exhaust flow to the ambient pressure. Special attention is then given to altitude-adaptive nozzle concepts, which have recently received new interest in the space industry. Current research results are presented for dual-bell nozzles and other nozzles with devices for forced flow separation and for plug nozzles with external free stream expansion. In addition, results of former research on nozzles of dual-mode engines such as dual-throat and dual-expander engines and on expansion– deflection nozzles are shown. In general, flow adaptation induces shocks and expansion waves, which result in exit pro. Less that is quite different from idealized one-dimensional assumptions. Flow phenomena observed in experiments and numerical simulations during different nozzle operations are highlighted, critical design aspects and operation conditions are discussed, and performance characteristics of selected nozzles are presented. The consideration of derived performance characteristics in launcher and trajectory optimization calculations reveal significant payload gains at least for some of these advanced nozzle concepts.

Nomenclature

A = area

F = thrust

h = height altitude

I = impulse

l = length

$\dot{m}$ = mass flow rate

p = pressure

$\bar{r}$ = mass ratio oxidizer/ fuel mixture

r = radius

x , y = coordinates

ε = nozzle area ratio

Subscripts

amb = ambient

c = combustion chamber

cr = critical

e = exit plane

geom = geometrical

ref = reference

sp = specific

t = throat

vac = vacuum

w = wall

I. INTRODUCTION

The reduction of Earth-to-orbit launches costs in conjunction with an increase in launcher reliability and operational efficiency are the key demands on future space transportation systems, like single-stage-to-orbit vehicles (SSTO). The realization of these vehicles strongly depends on the performance of the engines, which should deliver high performance with low system complexity. Performance data for rocket engines are practically always lower than the theoretically attainable values because of imperfections in the mixing, combustion, and expansion of the propellants. The examination and evaluation of these loss effects is and has for some time been the subject of research at scientific institutes and in industry. Table-1 summarizes performance losses in the thrust chambers and nozzles of typical high-performance rocket engines:

The SSME- and Vulcain 1 engine shuttle main engine, Rocketdyne hydrogen– oxygen engine and hydrogen–oxygen core engine of European Ariane-5 launcher). Among the important loss sources in thrust chambers and nozzles are viscous effects because of turbulent boundary layers and the nonuniformity of the flow in the exit area, whereas chemical nonequilibrium effects can be neglected in H_2–O_2 rocket engines with chamber pressures above p_c = 50 bar. Furthermore, the nonadaptation of the exhaust flow to varying ambient pressures induces a significant negative thrust contribution (see Figs. 1– 3). Ambient pressures that are higher than nozzle wall exit pressures also increase the danger of flow separation inside the nozzle, resulting in the possible generation of side loads. A brief description of state-of-the-art prediction methods for both phenomena is given.

Table 1 Performance losses in conventional rocket nozzles

Losses	**Vulcain 1, %**	**SSME %**
Chemical nonequilibrium	0.2	0.1
Friction	1.1	0.6
Divergences, nonuniformity of exit flow	1.2	1.0
Imperfection in mixing and combustion	1.0	0.5
Nonadapted nozzle flow	0-15	0-15

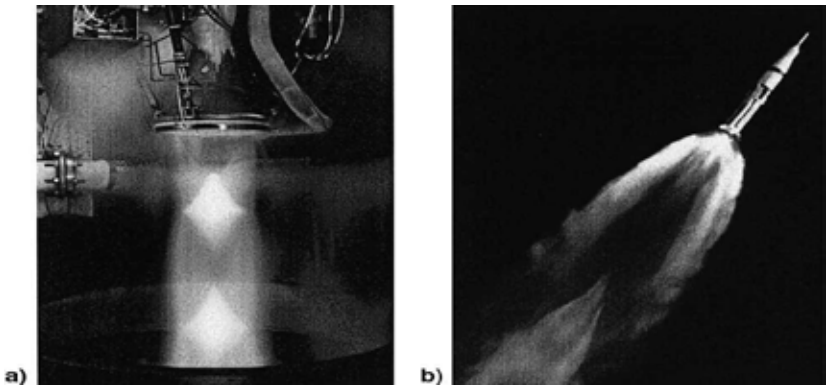

Fig. 1 - Rocket nozzle flow fields during off-design operation

a) Over expanded flow RL10A-5 engine and

b) Under expanded flow Saturn-1B, Apollo-7 (Photographs, United Technologies' Pratt & Whitney, NASA).

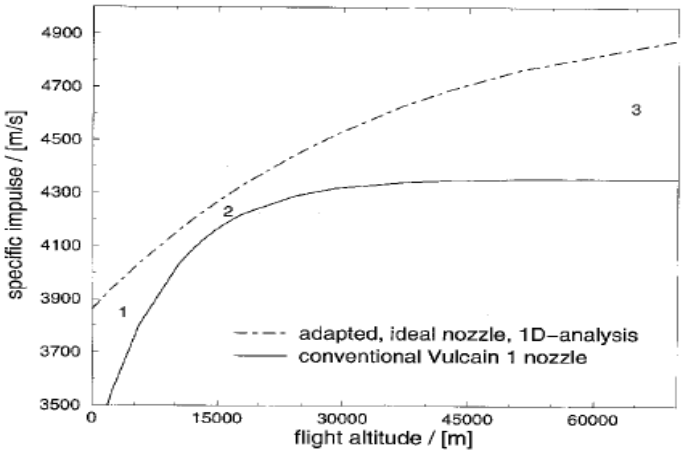

Fig. 2 - Performance Data For Nozzle of Vulcain 1 Engine (Design Parameters of Vulcain 1 Nozzle: $\varepsilon = 45$, $p_c / p_{amb} = 555$, $\bar{\gamma} = 5.89$).

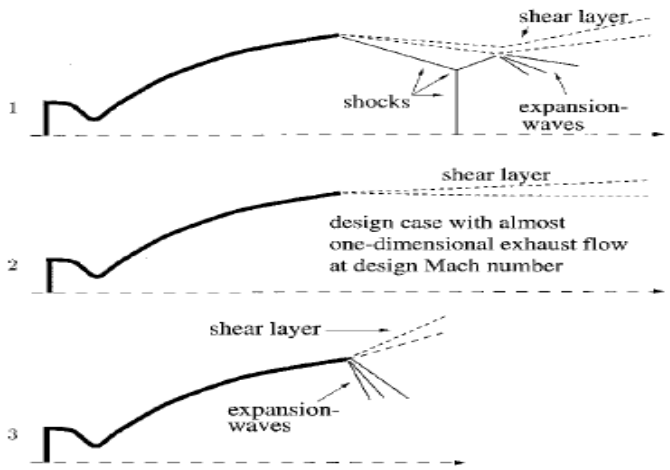

Fig. 3 -Flow Phenomena For A Conventional Rocket Nozzle

II. CONVENTIONAL NOZZLES

Conventional bell-type rocket nozzles, which are in use in practically all of today's rockets, limit the overall engine performance during the ascent of the launcher owing to their fixed geometry. Significant performance losses are induced during the off-design operation of the nozzles, when the flow is over expanded during low-altitude operation with ambient pressures higher than the nozzle exit pressure, or under expanded during high-altitude operation with ambient pressures lower than the nozzle exit pressure. Figure 1 shows photographs of nozzle exhaust flows during off-design operation. In the case of over expanded flow, oblique shocks emanating into the flow field adapt the exhaust flow to the ambient pressure. Further downstream, a system of shocks and expansion waves leads to the characteristic barrel-like form of the exhaust flow. In contrast, the under expansion of the flow results in a further expansion of the exhaust gases behind the rocket. Off-design operations with either over expanded or under expanded exhaust flow induce performance losses. Figure 3 shows calculated

performance data for the Vulcain 1 nozzle as function of ambient pressure, together with performance data for an ideally adapted nozzle. Flow phenomena at different pressure ratios p_c / p_{amb} are included in Fig. 3. [The sketch with flow phenomena for the lower pressure ratio p_c / p_{amb} shows a normal shock (Mach disk). Depending on the pressure ratio, this normal shock might not appear, see, e.g., Fig. 1.] The Vulcain 1 nozzle is designed in such a manner that no uncontrolled flow separation should occur during steady-state operation at low altitude, resulting in a wall exit pressure of $p_{w,e} \approx 0.4$ bar, which is in accordance with the Summerfield criterion. [8] The nozzle flow is adapted at an ambient pressure of $p_{amb} \approx 0.18$ bar, which corresponds to a flight altitude of $h \approx 15{,}000$ m, and performance losses observed at this ambient pressure are caused by internal loss effects (friction, divergence, mixing), as Table 1. Losses in performance during off-design operations with over- or under expansion of the exhaust flow rise up to 15%. In principle, the nozzle could be designed for a much higher area ratio to achieve better vacuum performance, but the flow would then separate inside the nozzle during low-altitude operation with an undesired generation of side-loads. Induce an oblique shock wave near the wall, which leads to a recompression of the flow.

III. ALTITUDE ADAPTIVE NOZZLES

A critical comparison of performance losses shown in Table 1 reveals that most significant improvements in nozzle performance for first-stage or SSTO engines can be achieved through the adaptation of nozzle exit pressures to the variations in ambient pressure during the launcher's ascent through the atmosphere. Various concepts have been previously mentioned and will be discussed in detail in the following text.

3.1 Nozzles with Devices for Controlled Flow Separation

Several nozzle concepts with devices for controlled flow separation have been proposed in the literature, with primary emphasis on the reduction of side-loads during sea level or low-altitude operation. But the application of these concepts also results in an improved performance through the avoidance of significant overexpansion of the exhaust flow.

3.1.1 Dual-Bell Nozzle

This nozzle concept was first studied at the Jet Propulsion Laboratory17 in 1949. In the late 1960s, Rocket dyne patented this nozzle concept, which has received attention in recent years in the U.S. and Europe. Figure 4 illustrates the design of this nozzle concept with its typical inner base nozzle, the wall inflection, and the outer nozzle extension. This nozzle concept offers an altitude adaptation achieved only by nozzle wall inflection. In low altitudes, controlled and symmetrical flow separation occurs at this wall inflection (Fig. 5), which results in a lower effective area ratio. For higher altitudes, the nozzle flow is attached to the wall until the exit plane, and the full geometrical area ratio is used. Because of the higher area ratio, an improved vacuum performance is achieved. However, additional performance losses are induced in dual-bell nozzles,

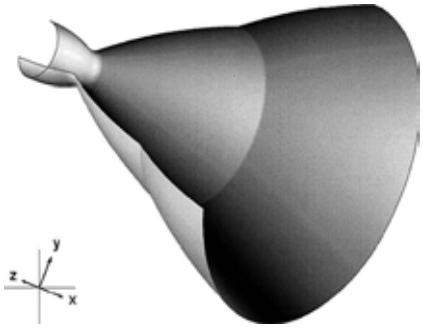

Fig. 4- Sketch of A Dual-Bell Nozzle

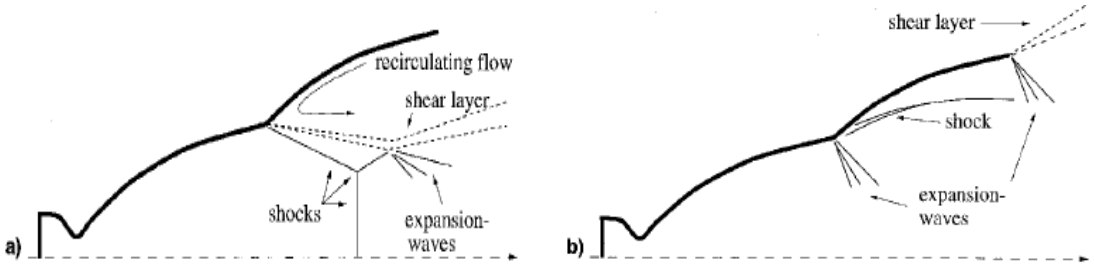

Fig. 5- Flow Field Phenomena In Dual-Bell Nozzles: a) Sea-Level Mode With Flow Separation At The Wall Inflection Point and b) Altitude Mode With A Full-Flowing Nozzle.

3.1.2 Two-Position or Extendible Nozzles

Nozzles of this type with extendible exit cones are currently used only for rocket motors of upper stages to reduce the package volume for the nozzle, e.g., at present for solid rocket engines such as the inertial upper stage (IUS), or for the liquid rocket engine RL10. The main idea of the extendible extensions to use a truncated nozzle with low expansion in low-flight altitudes and to have a higher nozzle extension at high altitudes. Figure 6 illustrates this nozzle concept. Its capability for altitude compensation is indisputable and the nozzle performance is easily predictable. The whole nozzle contour including the extendible extension is contoured for maximum performance at the high-area ratio with either the method of characteristics or a variational method. The area ratio of the first nozzle section is then determined and the nozzle contour is divided into two parts: The fixed nozzle part and the extendible extension. Investigations conducted at the Keldysh Center have shown that this nozzle-contouring method is not only the simplest but also provides a good overall trajectory performance. A minor performance loss is incorporated during low-altitude operations because of the truncated inner nozzle, which has a nonoptimal contour for this interim exit area ratio.

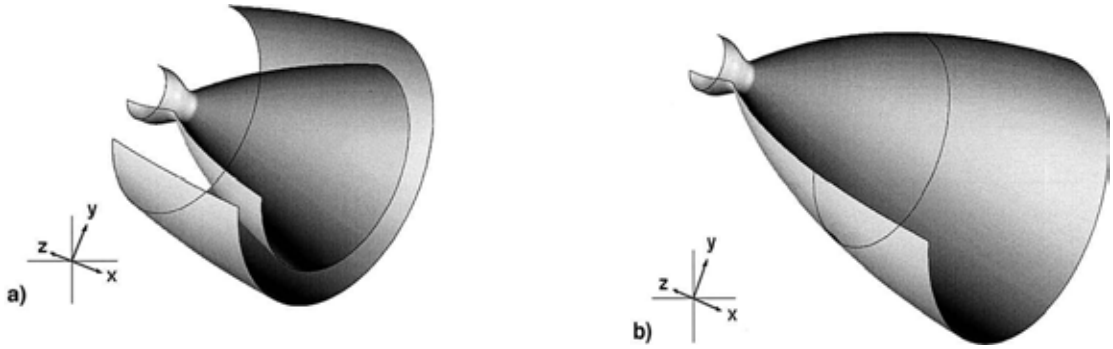

Fig. 6 - Sketch of a two-position nozzle during a) sea-level and b) Vacuum operations.

IV. CONCLUSIONS

Several nozzle concepts that promise gains in performance over conventional nozzles were discussed in this paper, including performance enhancements achieved by slight modifications of existing nozzles, e.g., through cool gas injection into the supersonic nozzle part. It is shown that significant performance gains result from the adaptation of the exhaust flow to the ambient pressure, and special emphasis was given to altitude adaptive nozzle concepts. A number of nozzle concepts with altitude-compensating capability were identified and described. To assist the selection of the best nozzle concept for launch vehicle applications, the performance of the nozzles must be characterized. This can be done using computational fluid dynamics (CFD) and/or cold-flow tests. Existing CFD methods that are in use in the aerospace industry and at research institutes have been verified for a wide number of sub- and full-scale experiments, and provide sufficiently reliable performance

determination for the different nozzle types. Theoretical evaluations, numerical simulations, and test results showed that the different concepts have real altitude-compensating capabilities. However, the compensation capabilities are limited and there are some drawbacks associated with each of the concepts. Additional performance losses are induced in practically all of these nozzle concepts when compared to an ideal expansion, mainly because of the nonisentropic effects such as shock waves and pressure losses in recirculation zones. However, these additional performance losses are less than 1– 3%, depending on the different nozzle concepts.

In addition to aerodynamic performance, other technical issue (weight, cost, design, thermal management, manufacturing, system performance, and reliability) must be addressed. Furthermore, before final decision can be made as to which nozzle concept offers the greatest benefits with regard to an effective payload mass injection, combined launcher and trajectory calculations must be performed and compared to a reference launcher concept with conventional nozzles. Different nozzle efficiencies, which account for the additional losses of advanced rocket nozzles and are extracted from numerical simulations and experiments, must be taken into account. At least for some of these nozzle concepts, the plug nozzle, the dual-bell nozzle, and the dual-expander nozzle, benefits. Ts with regard to lower overall launcher masses have been demonstrated in the literature. Furthermore, the plug nozzle concept will be the first in flight of all these advanced nozzle concepts, with the X-33 demonstrator vehicle.

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A REVIEW OF WIRELESS POWER TRANSMISSION VIA SOLAR POWER SATELLITE TECHNOLOGY

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ABSTRACT

A solar power satellite (SPS) is satellite dedicated to collecting solar energy on orbit, transforming it into microwave or laser energy, and beaming it to a receiving station on the ground. The recent increase in energy costs , predictions of the near-term exhaustion of oil and prominence of possible climate change due to the "green house effect" from burning of fossil fuels has again brought alternative energy sources to public attention, and the time is certainly appropriate to reexamine the economics of space based power. It mainly concerns about the conversion of energy obtained from the sun by satellite to microwaves using a externally placed device called magnetron. The DC power received on earth is converted into AC for various useful purposes. This paper gives a comprehensive study of various components of satellite based SPS and projects this technology as a bulk source of power generation in future.

Keywords: ***Microwaves, Magnetron, Photovoltaic, Rectenna, Wireless Power Transmission***

I. INTRODUCTION

The definition of Wireless Power Transmission (WPT) is efficient transmission of electric power from one point to another trough vacuum or an atmosphere without the use of wire or any other substance. This can be used for applications where either an instantaneous amount or a continuous delivery of energy is needed, but where conventional wires are un affordable, inconvenient, expensive , hazardous , unwanted or impossible. The power can be transmitted using microwaves, millimeter waves or lasers. WPT is a technology that can transport power to locations, which are otherwise not possible or impractical to reach [1].

The conventional methods for generating electrical power are insufficient for providing the increasing demand of electrical power. Thus, there is an urgent need to supplement the conventional sources. In “fig.1” shows Solar power generation with its associated technologies advanced few steps ahead in last several decades. It has been believed and investigated since last four decades that solar energy in space free from the weather conditions is quite different from that on the earth. The SPS system has great potential to harness solar power using bulk photovoltaic (PV) array in space and transmit it to the earth using microwave. The solar energy from sun while travelling a path to Earth is lost in the atmosphere because of the effects of reflection and absorption.

Therefore, it would be much beneficial to absorb solar energy from the geosynchronous orbit. A geosynchronous orbit is any orbit which has a period equal to the earth's rotational period. Accounting for efficiency, the PV cells produce 5 to 10% times more power at space than at ground [2].

Thus placing solar cells in space has a competitive advantage over solar power plants on the Earth. A photovoltaic cell can be placed on satellite revolving in geosynchronous orbit to absorb the solar energy. The

satellite is called as solar powered satellite. The generated DC by the photovoltaic cell can be converted into microwave by using magnetron, klystron or solid state devices. The generated microwave is transferred to the earth using antenna. The transmitted power is received by a device called rectenna. The received power is converted into DC power by filters and schottky diode. Power transmission using laser beam is also possible but, the power efficiency at both the transmitter and receiver of microwave transmission is more as compared with laser [3]

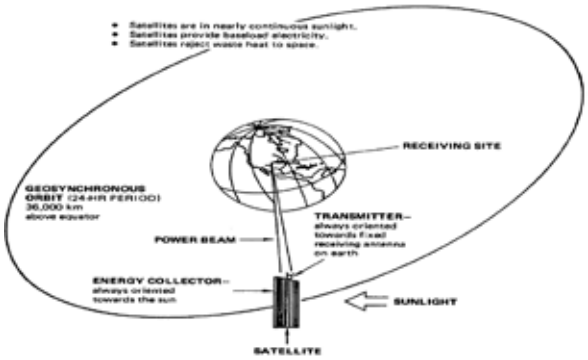

Fig.1 A Solar Power Satellite Concept

II. DESIGN OF THE SATELLITE BASES SYSTEM

The complete assembly of the satellite based system is shown in "Fig.2.1" and "Fig.2.2" shows the solar panels are connected on either sides of the satellite. These solar panels are the main source of DC power. Microwaves are generated using a device called magnetron powered by DC supply. Photovoltaic cells are used for converting solar radiations into DC power [3].

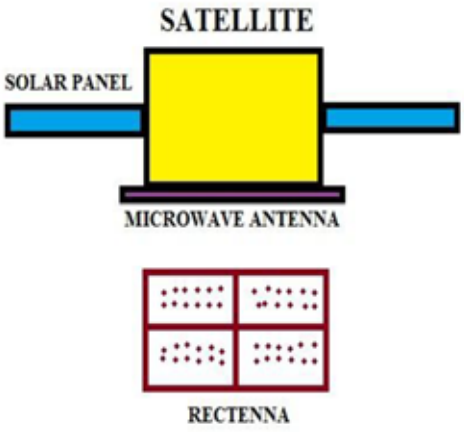

Fig.2.1 The Satellite Based System

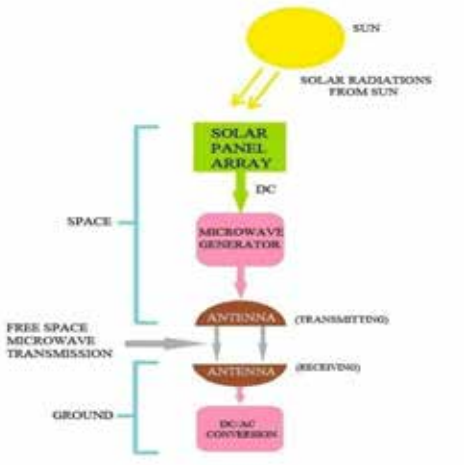

Fig.2.2 Block Diagram of Satellite Based System

III. Components and Specification

3.1 Magnetron

Magnetron is a high powered vacuum tube device that generates microwaves owing to the motion of clouds of electrons in a crossed electric and magnetic fields. Magnetron originally developed in 1916 as an alternative to grid control in vacuum tubes. It was discovered during the DEO/NASA study of SPS that the microwave oven magnetron along with the external passive circuitry can perform as phase locked high gain of 30dB amplifier for

direct use in the transmitting section. For ground based transmitter, the microwave oven magnetron can be used directly [5]. However for space use, based on the same principle, special space magnetron is required.

3.2 Construction

"Fig"3 shows the cut view of magnetron. It consists of a cathode which is placed at the centre. A ring shaped anode surrounds the cathode. In anode structure, there are resonant cavities. A permanent magnet is placed beneath the anode which produces magnetic field along the length of the cathode. The resonant cavities present in anode structure are channeled at one end of the magnetron where the produced microwaves are collected. This channeled section is called as a waveguide.

3.3 Working

Generally, in microwave magnetron the maximum anode voltage is 4.5kV and the maximum cathode filament voltage is3.75 V AC. There is a heated cathode at the centre. Hence electrons are released from it by the process called 'Thermo Ionic Emission'.

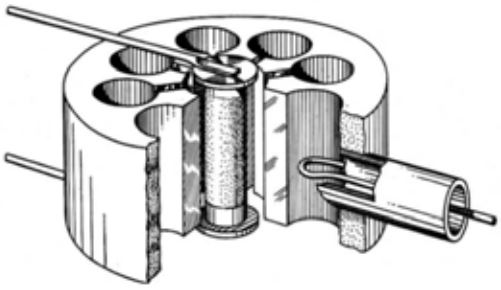

Fig. 3 Magnetron

The liberated electrons will try to move towards anode. But, because of the crossed electric and magnetic fields, they move in a circular path around anode. As they move in a circular path they pass the cavities of the anode. The cavities thus resonate and emit microwave radiations. Microwaves from all the cavities are summed up in a channel at the end of the tube. Hence, in this way the microwaves are collected from the one end of the magnetron.

3.4 Specifications

Table 1

Magnetron Rating [6]

	Minimum	Maximum	Unit
Filament voltage	2.85	3.75	V AC
Peak Anode Voltage	-	4.5	kVp
Output Frequency	2.45	2.75	GHz

IV. ANTENNA

The official definition of the antenna according to the IEEE (Institution of electrical and electronic engineers) is simply a means for radiating or receiving radio waves. An antenna or aerial is a system of elevated conductors which couples or matches the transmitter or receiver to free space.

4.1 Working

A transmitting antenna connected to a transmitter by a transmission line, forces electromagnetic waves into free space which travel in space with velocity of light, similarly, a receiving antenna connected to a radio receiver receives or intercepts a portion of electromagnetic waves travelling through space [7].In “fig. 3”. Shown the space based solar power using the Antenna.

Efficiency of Antenna

$$\eta = \frac{\text{Power Radiated}}{\text{Total input Power}}$$

$$\text{Directive gain } G_d = \frac{\text{Radiation Intensity}}{\text{Average Radiated Power}}$$

$$\text{Directive gain} = \frac{\emptyset(\theta, \phi)}{W_r/4\pi}$$

$$\text{Power Gain} = \frac{\text{Power Radiated}}{\text{Total input Power}}$$

$$\text{Power Gain} = \frac{\emptyset(\theta, \phi)}{W_r/4\pi}$$

4.2 Rectenna

Brown was the pioneer in developing the first 2.45GHz rectenna. Rectenna is the microwave to dc converting device and is mainly composed of a receiving antenna and a rectifying circuit. Fig .4 shows the schematic of rectenna circuit [8]. It consists of a receiving antenna, an input low pass filter, a rectifying circuit and an output smoothing filter.

The input filter is needed to suppress radiation of high harmonics that are generated by the nonlinear characteristics of rectifying circuit. Because it is a highly nonlinear circuit, harmonic power levels must be suppressed.

For rectifying Schottky barrier diodes utilizing silicon and gallium arsenide are employed. Diode selection is dependent on the input power levels. The breakdown voltage limits the power handling capacity and is directly related to series resistance and junction capacitance through the intrinsic properties of diode junction and

material for efficient rectification the diode cut off frequency should be approximately ten times the operating frequency.

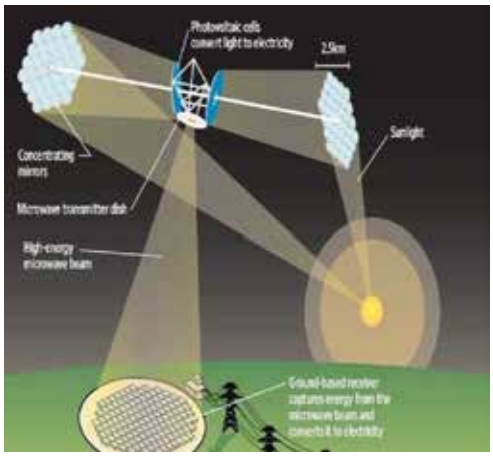

Fig. 3 Design of Space based Solar Power (SBSP) [4]

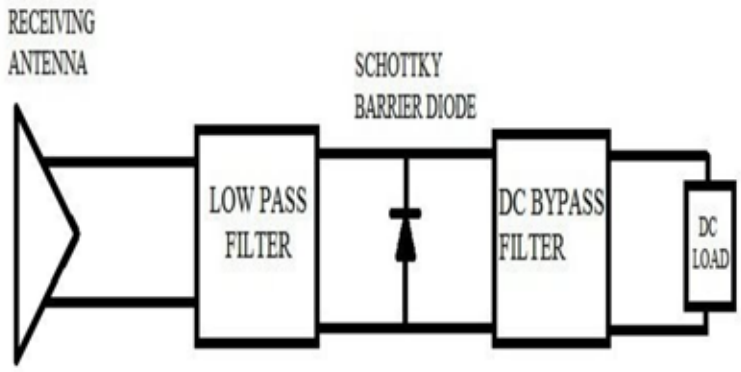

Fig. 4: Schematic of Rectenna Circuit. [9]

"Fig.5" shows Resent Trends In Power Systems (wireless power transmission system) Electricity plays a vital role in our day to day life & also there is a great demand for electricity today. Transmission losses are also one of the reasons for this demand .Since transmission is a main part of the power it should be more efficient. During trans mission there is a loss of 30%.To eliminate these losses we need a new technique which is called recent trend .The recent trend for efficient transmission of power is the wireless power trans mission system. This paper exposes a new method for wireless power trans mission using EM waves that comprises a transmitter and receiver in which we get a transmission efficiency of 95%.The receiver doesnot required an independent power source & it is comprised of an optical feedback to the transmitter & does not required a separate communication channel to the transmitter. The transmitter uses the optical feedback to locate and track the receiver. The transmitter can optionally employ a macro adjusters and micro adjusters that direct the beam on to the receiver for optimal power transmission. The system also optionally has a the tight loop beam detector to enhance the safety of the system. Either the receiver or transmitter may also encode data on the energy transmission, resulting in one -way or two- way data transmission.[10

V. ADVANTAGES

Energy delivered anywhere in the world. Zero fuel cost. Zero CO2 emission. Minimum long range environmental impact.[11] Unlike nuclear power plants, space solar power does not provide easy targets for terrorists. Unlike terrestrial solar and wind powerplants, space. Solar power is available 24 hours a day, 7 days a

Week in huge quantities. It works regardless of cloud over, daylight, or wind speed. Space solar power will provide true energy Independence for the nation that develop it, Eliminating a major source of national competition for limited Earth-based energy resource. Unlike oil, gas ethanol, and coal plants, space solar Power does not emit green house gases. [4]

VI. APPLICATION

There are many applications Example include fuel free airplanes, fuel free electric vehicles, moving robots and fuel free rockets, battery charging, car charging, remote control, game controller, headsets, sensors, computers, laptop charging, television and many more. [11]

VII. CONCLUSION

The solar power satellite would be in the earth's shadow for only a few days at the spring and fall equinoxes and even then for a maximum of an hour and a half late at night when power demands are at their lowest. As there are many storage systems like compressed air energy storage and battery storage available, the energy from SPS can be stored during low peak times and used efficiently during the peak load periods.

This concept offers greater possibilities for transmitting power with negligible losses and ease of transmission than any invention or discovery heretofore made. Dr. Neville of NASA states “You don’t need cables, pipes, or copper wires to receive power.

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 ISBN: 978-81-931039-3-7

AREA AND POWER EFFICIENT FULL ADDER DESIGN ON 50 NM TECHNOLOGY

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ABSTRACT

Full adder is an important component for the design and development of all types of processors such as digital signal processors (DSPs), microprocessors etc. Adders are the core element of complex arithmetic operations like addition multiplication, division, exponentiation etc. . In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper adder has been developed using Gate level, Circuit level. The performance of these different design has been analyzed and compare in term of power, delay, no. of Transistors used and area. The Simulation result show that circit level design is better by 46.78 percent in power and 53.29 percent in delay.

Keywords: Power Dissipation, MOS Devices, Computational Efficiency, Very Large Scale Integration (VLSI), Delay

I. INTRODUCTION

With the explosive growth in laptops, portable personal communication systems, and the evolution of the shrinking technology, the research effort in low-power electronics has been intensified. Today, there are an increasing number of portable applications requiring small-area[1] low-power high throughput circuitry[2,3]. Therefore, circuits with low-power consumption become the major candidates for design of systems. Technology trends show that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumptions raise chips' temperature and directly affect battery life. A higher temperature directly affects circuit operation and reliability; complicated cooling and packaging techniques are required. In addition, higher current density either shortens battery packs .Addition is the most commonly used arithmetic operation in microprocessors and DSPs, and it is often one of the speed-limiting elements . Hence optimization of the adder both in terms of speed and power consumption should be pursued. During the design of an adder we have to make two choices in regard to different design abstraction levels. One is responsible for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the specific design style at transistor level to implement the one-bit full adder. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability . Several works have been done in order to decrease transistor count and consequently decrease power consumption and area . In some designs, reducing transistor count has been resulted in threshold loss problem that causes non-full swing outputs , low speed and low noise immunity especially when they are used in cascaded fashion. Some of them has threshold loss problem that cause non-full swing outputs, the sentelow

speed and low noise immunity. However, usually they have less power consumption in comparison to full adders with full swing outputs. Not full swing full adders are useful in building up larger circuits as multiple bit input adders and multipliers[4,5]. In Integrated Circuits mainly two types of full adders (Static & dynamic) are used. Static full adders commonly are more reliable, simpler and lower power than dynamic ones. However, dynamic full adders are faster and some times more compact than static full adders. Dynamic full adders suffer from charge sharing, high power due to high switching activity, clock load and complexity.

II. FULL ADDER DESIGN

Gate level schematic of the one bit full Adder: A basic cell in digital computing systems is the 1-bit full adder which has 1-bit inputs (A, B, and C) and two 1-bit outputs (Sum and Carry). The addition of 2 bits (A and B) with input carry C generates the sum bit and the output carry bit. Boolean functions for the two outputs[6] can be manipulated to simplify the circuit as given below:

$S = ABCin + AB'C'in + A'B'Cin + A'BC'in$ (1)

$Cout = AB + ACin + BCin$ (2)

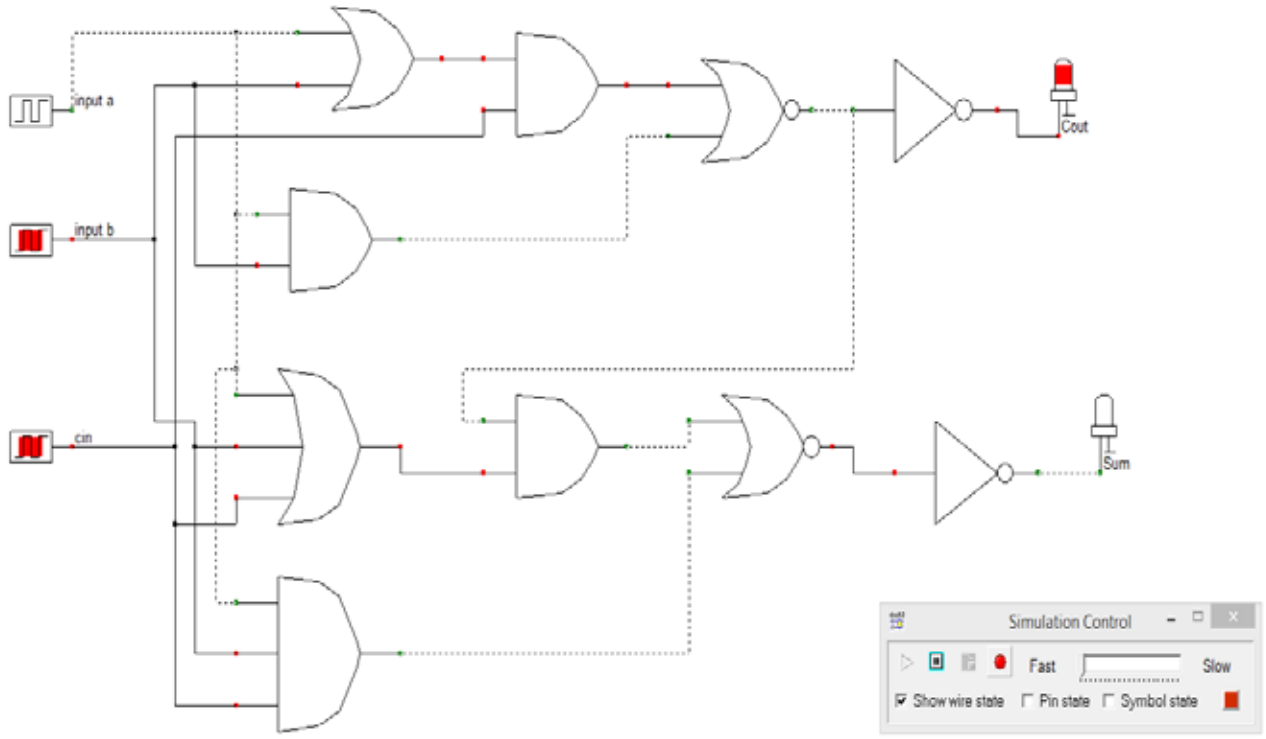

Fig. 1 Gate level schematic of the full Adder

Full Adder Using Two Half Adder: A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and OR the two carry outputs[9,10]. The critical path of a full adder runs through both XOR-gates and ends at the sum bit S.

Table.1 Truth Table of full adder

X	Y	C_{IN}	SUM	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

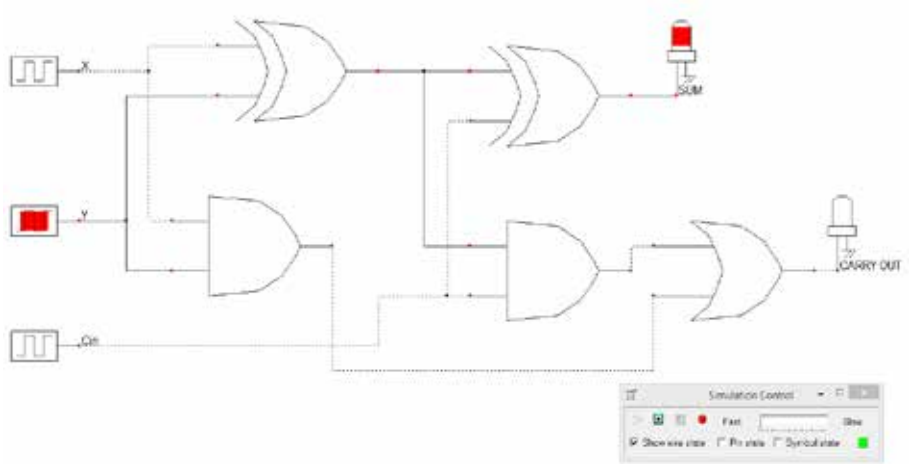

Fig.2 Full Adder using two half Adder

Static energy recovery Full Adder: In this type of adder the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic.[7,8]

Working principle: The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of thesecond stage XNOR circuit. The cout can be calculated by multiplexing a and cin controlled by (a ⊗ b). Let us consider that there is a capacitor at the output node of the first XNOR module. To illustrate static energy recovery let us consider an example where initially a=b=0 and then a changes to 1. When a and b both equals to zero the capacitor is charged by VDD. In the next stage when b reaches a high voltage level keeping a fixed at a low voltage level,the capacitor discharges through a. Somecharge is retained in a. Hence when a reaches a high voltage level we do not have to charge it fully. So the energy consumption is low here[10,11].

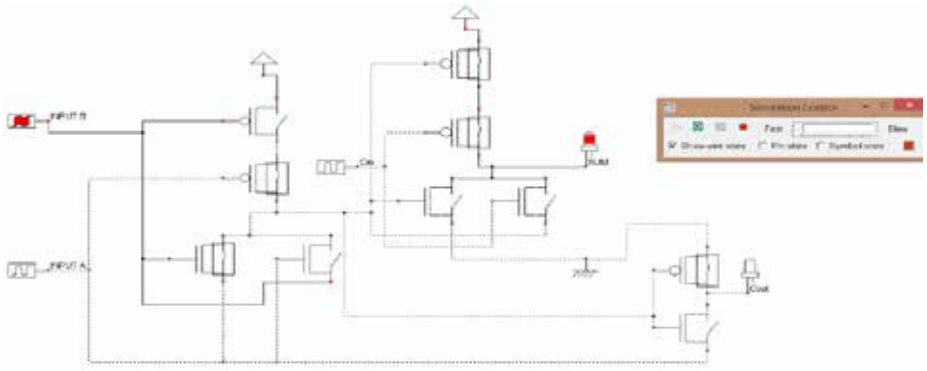

Fig.3 SERF Full Adder

Full adder with XOR and 2:1 Multiplexers : Hence Sum can be implemented using two XOR gates. Carry can be implemented using a 2:1 multiplexer with A and CIN as input lines and X as selection line.

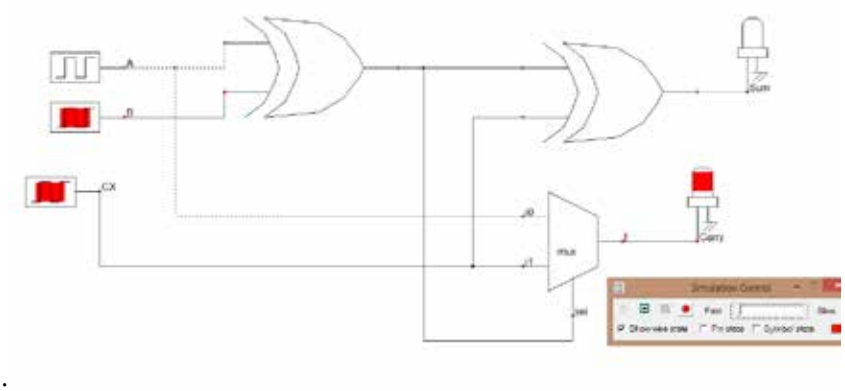

Fig. 4 Full adder with XOR and 2:1 Multiplexer

1-bit full adder using Two XNOR gates and one 2:1 Mux: Here Sum can be implemented using two XNOR gates. Carry can be implemented using a 2:1 multiplexer with A and CIN as input lines and X‘ as selection line

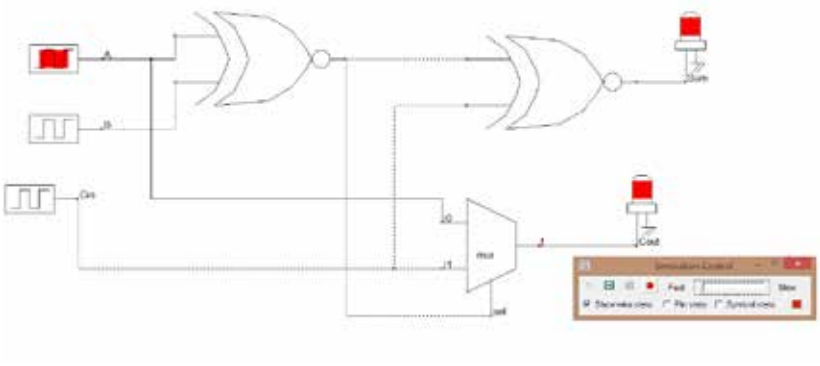

Fig. 5. Full adder with XONR and 2:1 Multiplexer

III. FULL ADDER LAYOUT SIMULATION

3.1 Logic Level Full Adder Implementation

The DSCH program is a logic editor and simulation .It provides user-friendly an fast simulation. Full adder using gates is implemented on DSCH[5] then its verilog file is generated and its layout and simulated result shown in Fig. below. It has been observe that for Gate level schematic of the full Adder average power

consumption is 55.064 µw, area is 116.8 µm2 Delay is found to be 0.283 ns and no transistor used is 26 Pmos and 26 Nmos.

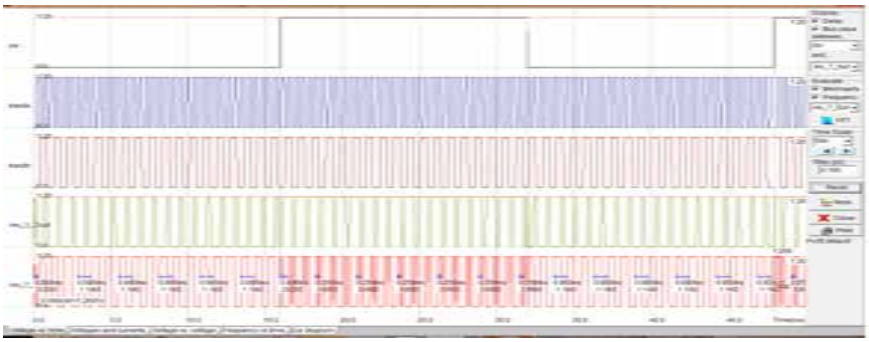

Fig. 6. Simulation Result of Gate Level Schematic of The Full Adder

Fig. 7 Layout of Gate Level Schematic of The Full Adder

3.2 Full Adder Using Two Half Adder

It has been observe that for Gate level schematic of the one bit full Adder average power consumption is 64.370 µw, area is 67.9 µm2 Delay is found to be 0.955 ns and no transistor used is 15 Pmos and 15 Nmos.

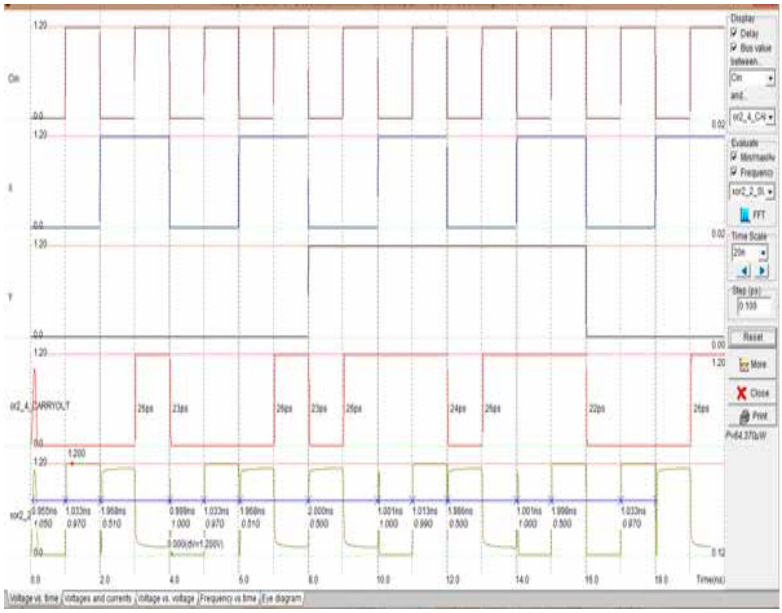

Fig. 8 Simulation Result Full Adder Using Two Half Adder

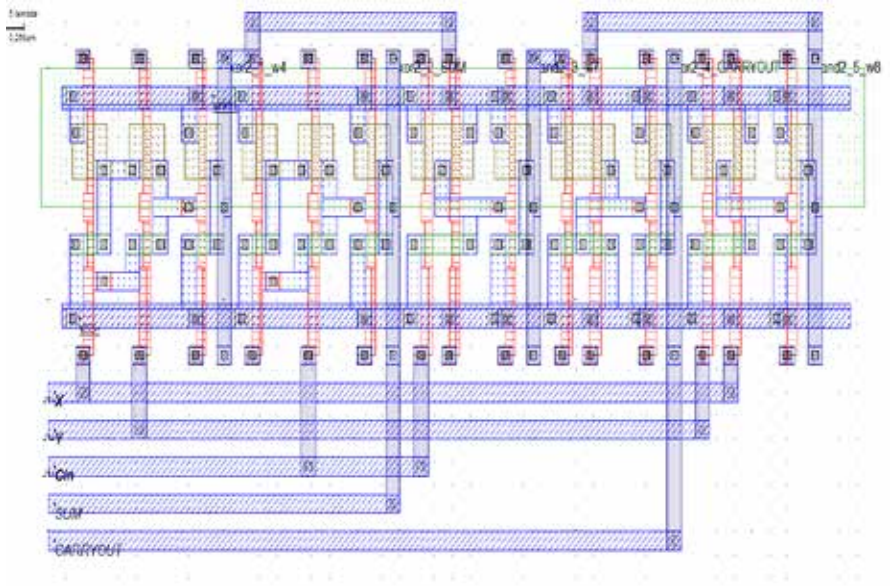

Fig. 8 Layout of Full Adder Using Two Half Adder

3.3 Circuit Level Full Adder Implementation

Static energy recovery Full Adder: It has been observe that for circuit level schematic of the one bit CMOS full Adder average power consumption is 34.252µw, area is 80 µm2 Delay is found to be 0.446 ns and no transistor used is 5 Pmos and 5 Nmos.

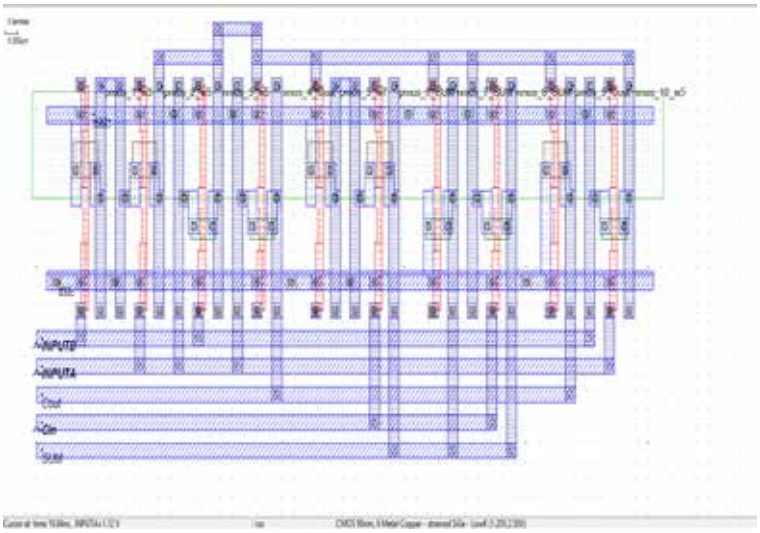

Fig. 9. Layout of Static energy recovery Full Adder:

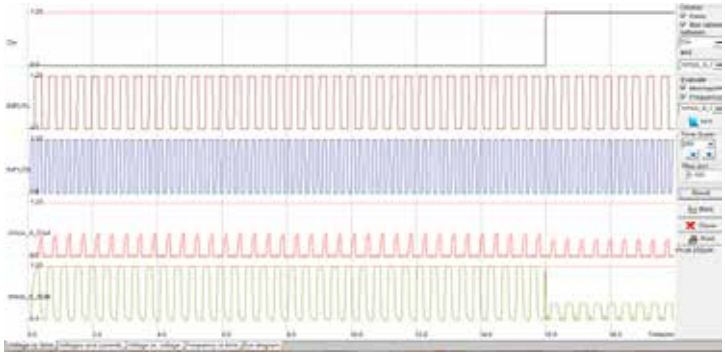

Fig. 10 Simulation result of Static energy recovery Full Adder

3.4 Full Adder with XOR And 2:1 Multiplexer

Full adder with XOR and 2:1 Multiplexers : It has been observe that for Hybrid level schematic of the full Adder average power consumption is 52.035µw, area is 74.6 µm2 Delay is found to be 8 ns and no transistor used is 9 Pmos and 9 Nmos.

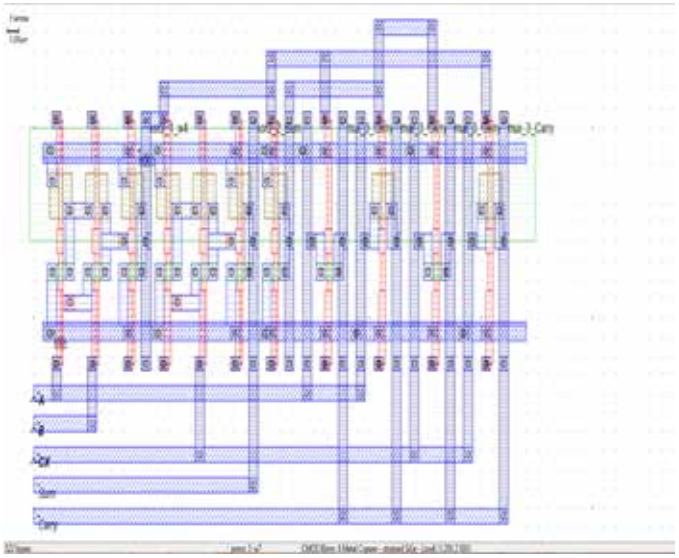

Fig. 11 Layout of of 1-bit Full adder with XOR and 2:1 Multiplexers

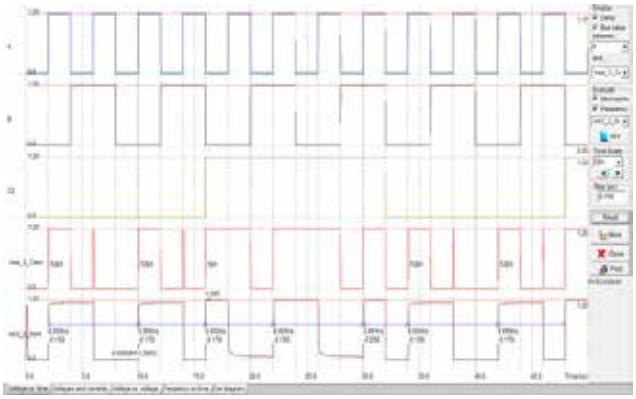

Fig. 12 Simulation result of 1-bit Full adder with XOR and 2:1 Multiplexers

Full adder with XNOR and 2:1 Multiplexers : It has been observe that for Hybrid level schematic of the one bit full Adder average power consumption is 52.035µw, area is 74.6 µm2 Delay is found to be 8 ns and no transistor used is 9 Pmos and 9 Nmos.

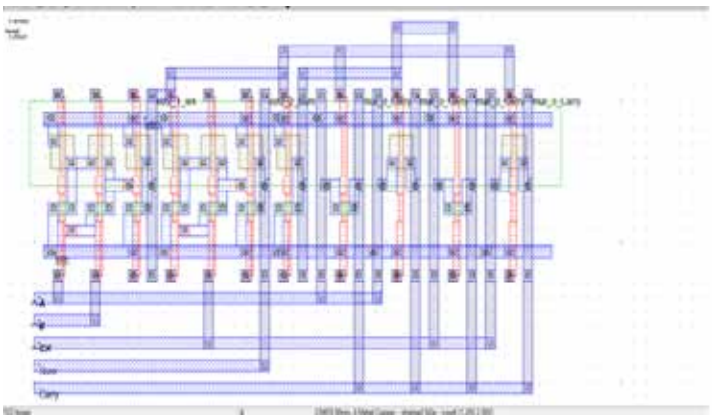

Fig. 13 Layout of of 1-bit Full adder with XOR and 2:1 Multiplexers

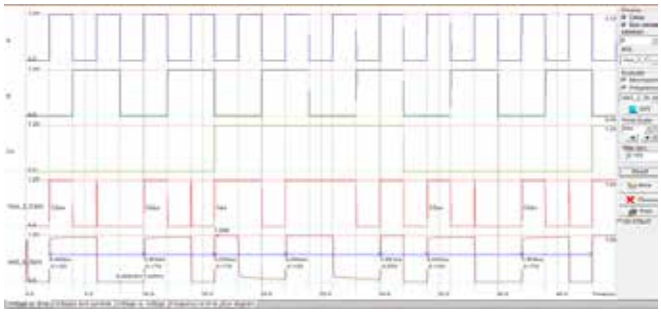

Fig. 14 Simulation result of 1-bit Full adder with XNOR and 2:1 Multiplexers

IV. RESULT ANALYSIS

Comparative analysis between various type of Full Adder is shown in Fig: No. of transistor is very less in Static energy recovery Full Adder as compared to gate level implementation. delay is maximum in Full adder with XOR and 2:1 Multiplexers and Full adder with XNOR and 2:1 Multiplexers, Gate level schematic of the full Adder has maximum no. of transistor.

Table.1 Comparative analysis of various type of Full Adder

S no.	FULL ADDER CIRCUIT	P (µW)	AREA (μm^2)	DELAY (ns)	NUMBER OF TRANSISTER
1.	Gate level schematic of the full Adder	**55.064**	116.8	0.283	26 nmos 26 pmos
2.	Full Adder Using Two Half Adder	**64.370**	67.9	0.955	15 nmos 15 pmos
3.	Static energy recovery Full Adder	**34.252**	80.0	0.446	5 nmos 5 pmos
4.	Full adder with XOR and 2:1 Multiplexers	**52.035**	74.6	8.000	9 nmos 9 pmos
5.	Full adder with XNOR and 2:1 Multiplexers	**52.035**	74.6	8.000	9 nmos 9 pmos

V. CONCLUSION

From the analysis of the above various type of Full Adder Circuits we can reach to a conclusion that the average power is low, area is increased to some extent and Power Delay Product is also low for Static energy recovery Full Adder among all types of adder. No. of transistor is very less in Static energy recovery Full Adder as compared to gate level implementation. For Optimization of Power (Average power) and Delay, we think that the best option is Static energy recovery Full Adder .

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AREA EFFICIENT CMOS DESIGN ANALYSIS OF SYNCHRONOUS UP COUNTER

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ABSTRACT

This paper presents the design of synchronous up counter which is one of the essential building block in very large scale integration design.Due to increase in demand of portable devices the research of less complex design also increased.Inthis paper Schematic and layout of 2 bit synchronous up counter has been designed using two schemes, one in which D flip flop is made by NMOS and other in which D flip flop is made by transmission gate.Performance of the 2 bit synchronous counter is also analysed in this paper by comparing the auto generated layout and proposed layout using 90nm CMOS technology.The proposed design of synchronous counter is 52.16% more area efficient than the auto generated layout.

Keywords: CMOS Integrated Circuit, Flip-Flops, Intergrationvlsi, Layout and Semiconductor Counter

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device [1].

A digital circuit is often constructed from small electronic circuits called logic gates that can be used to create combinational logic. Each logic gate represents a function of boolean logic. A logic gate is an arrangement of electrically controlled switches, better known as transistors.Counting is a fundamental function of digital circuits. A digital counter consists of a collection of flip-flops that change state (set or reset) in a prescribed sequence. The primary function of a counter is to produce a specified output pattern sequence [2]. A counter can play a vital role in several circuits ranging from a simple display to complex microcontroller circuits. Some of the apparent applications of a counter are: frequency divider in phase-locked loops, microcontrollers, digital memories and in digital clock and timing circuits [3].

Counter is one of the simplest but essential building blocks in very large scale integration design [1,4].Counters are usually classified into synchronous counters, such as up counter ,down counter ,ring counters and twisted counters, and asynchronous counters, such as ripple counter, up counter down counter and Mod N counter.[5] In

synchronous counter a common clock is used which is connected to each flip flop while in asynchronous counter clock is connected to first flip-flop only and the output of one flip-flop derive the input of the next one [6].Synchronous counter has many advantages over asynchronous counter.Asynchronous counter not useful at very high frequencies , especially for counter with large number of bits. Another problem caused by propagation delays in asynchronous counter occurs when we try to electronically detect (decode) the counter's output states.

II. SYNCHRONOUS COUNTER

Synchronous counter is the most popular type of counter. It typically consists of a memory element, which is implemented using flip-flops and a combinational element, which is traditionally implemented using logic gates. Logic gates are logic circuits with one or more input terminals determined by a combination of input signals. The use of logic gates for combinational logic typically reduces the cost of components for counter circuits to an absolute minimum, so it remains a popular approach[3].

The operation of conventional synchronous counters is usually based on a synchronous timing principle in which new data values of the entire counter bits are evaluated at every clock cycle and captured by associated flip-flops (FFs) at every triggering edge of the clock. Because the switching activity of counter bits in a binary counter is decreased by half as the significance of each bit increases, this type of operation apparently causes a lot of redundant transitions, particularly for counter bits having higher significance. Fine-grain clock-gating schemes [7,8] can be used to eliminate these redundant transitions.[9]. For the designing of counter circuit flip flops are used . Flip flops is a storage element based on gated latch principle, which can have its output changed only on the edge of the controlling clock signal. The combination of number of flip flops makes a sequential circuit. The Flip-Flop remains locked on an output of either 0 or 1 until it is given some sequence of inputs, in which case its output will change[10].

Synchronous counter are of two type on the basis of sequence of states i.e. up counter and down counter. In the proposed design of this paper synchronous up counter has been designed using D flip flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops [11].

The designing of synchronous counter first include to draw the state transition diagram showing all the possible states, including those that are not part of the desired counting sequence[12], then use the state transition diagram to set up a table that lists all present states and their nextstates and lastly add a column to this table for flip flop input ,simplify the expression using Karnaugh map. so truth table for synchronous up counter shown in table 1. The proposed synchronous 2-bit up counter has one NOT gates, 1 XOR gates and 2 D flip-flops. Same clock pulse is given to each flip-flop so proposed design is implemented [13].

Table 1: Truth table of 2 Bit Synchronous up Counter

Present state		Next state		Flip flop input	
A	B	A_{n+1}	B_{n+1}	D_A	D_A
0	0	0	1	0	1
0	1	1	0	1	0

1	0	1	1	1	1
1	1	0	0	0	0

III. SCHEMATIC AND LAYOUT

Proposed counter is implemented using DSC 3.1 tool. Transistor level design is implemented using Microwind 3.1 tool. Optimized design is also made by Microwind 3.1. Design of proposed counter 2 bit synchronous up counter using DSCH 3.1 according to the truth table shown in section II can be shown in fig. 1 that is the first schematic design.

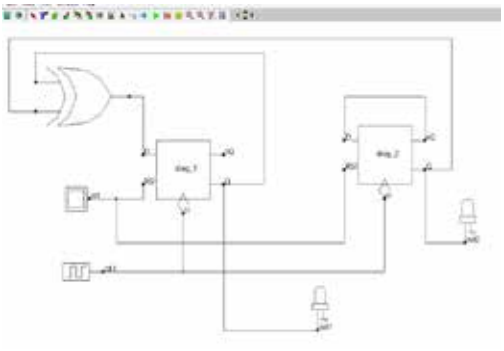


Fig.1: Schematicof 2-Bit Synchronous Up Counter

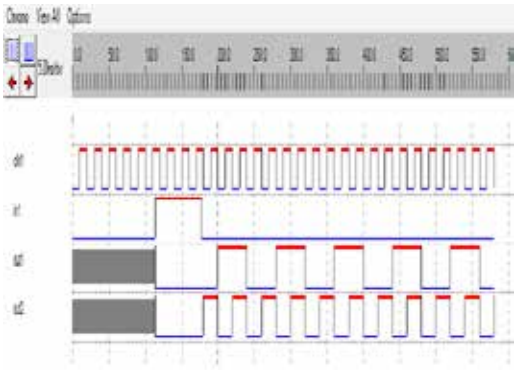


Fig.2:2-Bit Synchronous Up Counter Waveform

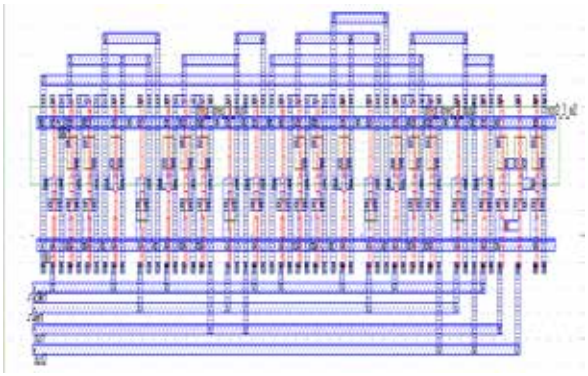


Fig.3: Layout of 2 Bit Synchronous up Counter

The auto generated layout of 2 bit synchronous up counter is obtained by making Verilog file and compile that Verilog file using microwind 3.1 tool. Which is shown in above fig. 3.

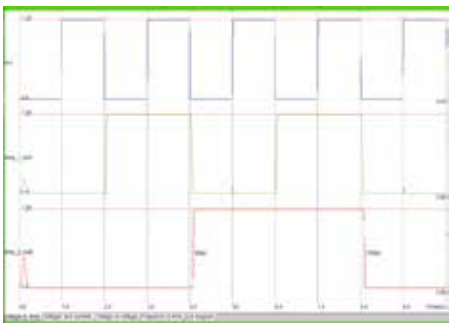
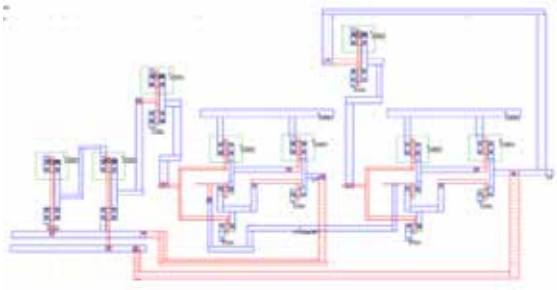


Fig.4: 2 Bit Synchronous up Counter Waveform

Fig.4 shows the output waveform of 2 bit synchronous up counter which is obtained by microwind 3.1 from the autogenerated layout of 2 bit up counter.D flip flop can be made either of transmission gate or by nmos transistor. So For making the area efficient optimized design of 2 bit synchronous up counter 2 layout has been

prepared.As 2 bit synchronous up counter is made by d flip flop in this paper ,so in first case layout is made by transmission gate ,which is shown in fig.5. Syncronous up counter which is made by Transmission gate d flip flop is used 18 transistors.



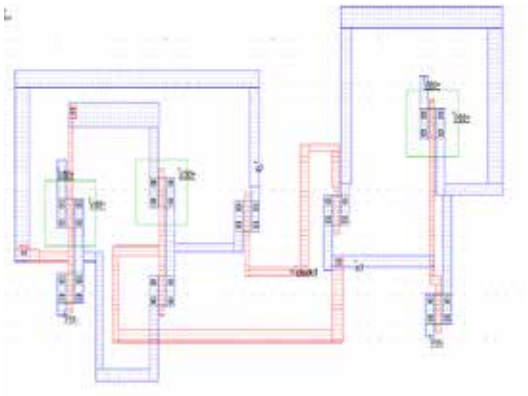


Fig.5:Proposed Layout Using Transmission Gate **Fig.6:Proposed Layout Using NMOS**

D flip flop can also be made using nmos ,so in second case of optimized design of 2 bit synchrnous up counter which is implemented using 8 transistor is shown in fig.6 and the output waveform is shown in fig.7.

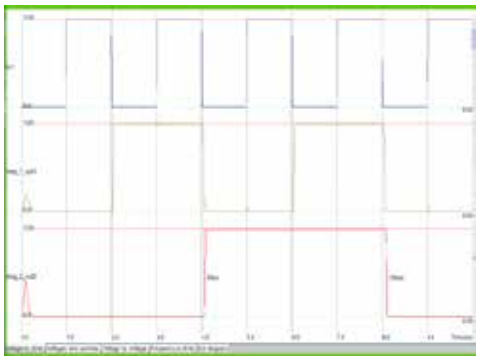


Fig.7:Proposed Layout Output Waveform

IV. RESULT ANALYSIS

As can be seen from the simulated schematic and layout that the auto generated layout is more complex in comparison to the self generated proposed layout. Table 2 shows the performance analysis all three counter on the basis on height, area and power required of each proposed layout and auto generated Layout of 2 bit synchronous up counter.

Table 2 Area and Power Analysis of Two Layout

	Auto generated Layout	Proposed Layout	
		Transmission gate	NMOS
Width	24.1 µm	14.29µm	11.5µm
Height	6.6µm	11.1µm	6.3µm
Area	159.1µm^2	158.7µm^2	76.1µm^2
Power	84.352µW	0.187mW	.153mW

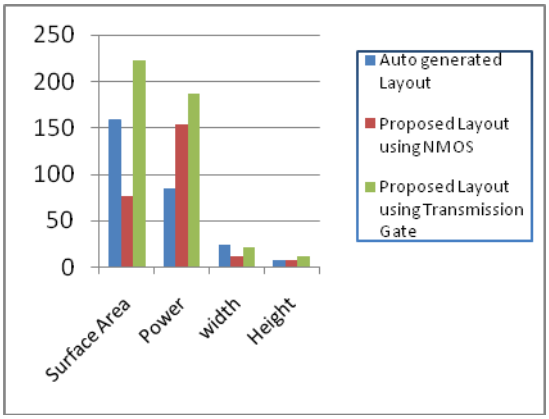


Fig.8: Layout Comparison for Area, Power and Height

The table 2 shows that the consumed power for auto generated layout is 84.352µW that is smaller than the power required for proposed layout, while the surface area requirement of proposed layout in which d flip flop is used as NMOS less in comparison with other two layout .It is also be noticed from all the three layouts that the number of transistor requirement is less in proposed layout which is made by NMOS transistor. Fig.8 shown above is the comparative analysis of auto generated layout and proposed layout and signify which layout perform better.

V. CONCLUSION

This paper includes the design of 2 bit synchronous up counter. Performance analysis of auto generated layout and proposed layout also be done in this paper.For the optimized area efficient proposed layout of synchronous up counter ,2 types of design has been used. one in which D flip flop is made by transmission gate and another one in which D flip flop is made by NMOS.From the result it is clear that optimized proposed layout of synchronous up counter is more area efficient than auto generated layout design .As optimized layout provide 52.16 % less area than the auto generated layout and 52.04% from the layout which used transmission gate as d flip flop. Number of transistor requirement is also less in proposed area efficientoptimized layout.

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LICENCE MANAGEMENT SYSTEM USING ANDROID BASED MOBILE BIOMETRICS

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ABSTRACT

Mobile based bio-metrics employing android technology provides an important front-line security in every domain. Based around a central biometric identification system (BIS), mobile based biometrics extend the functionality and capabilities of a static BIS by allowing users to capture fingerprints out in the field, and compare minutiae against remotely stored bio-metric databases. The idea of our project is to develop a client server android application, capturing the images of number plate of the driver's vehicle and the driver's fingerprints, upon which OCR and BOZORTH3 algorithms being performed respectively. For a match, the corresponding records being fetched from the database consisting of personal details, licence details, vehicle information. A track of history of numerous offenses would be kept at server side and updated continuously by the officials in the field. Also, in case of vehicles not complying with their registered users, an SMS would be sent being integrated with the application to instantly check for malicious vehicle thefts. Additionally, data mining using analytics is done on offenses info for determining any subtle statistical patterns of drivers and keeping a check on the road-side menaces.

Keywords: Bio-metrics, BOZORTH, licence, MINDTCT, Minutiae, OCR.

I. INTRODUCTION

Bio-metrics encompasses a range of for identity verification [17] using speciality-traits in them. Bio-metrics main focus is to exploit those distinctive and eccentric features using them for recognizing one sample from the other. Bio-metric technologies[4] are slowly evolving [16]to become one of the most far-reaching and paramount factors[5] in recognition and identifying processes .With the proliferating and swelling cases revealing the shaky and fragile security system, it is imminent that the time is drawing near for a better, safe, secure, well-guarded biometric identification systems especially fingerprints [14].Additionally, Android is becoming far more outreaching with its cutting-edge technology[20] and sophisticated features. It is evident that these systems are roaring in the market and will hold a key factor in security systems. Bio-metric based android solutions provide authenticity to data additionally to transactions and other covert channels. The applications of mobile biometrics employing android varies from as common as fast food centres and banks to as far-reaching [5]as in military and clandestine purposes [1]to bio-metric residence permits[12],[13]. Numerous domains are embracing these technologies. The most eloquent and compelling characteristics of fingerprint scanning are their resolution and their elegant act of handling the fingerprint images. The questions posed to the reader are thus:-

1. So why not employ this strategy for curbing the menacing problems encountered during road travels due to licenses, drunk driving and other related cases?

2. At a staggering estimated 7.5Billion$ industry worldwide in 2014, aren't vehicle thefts a menace not only to officials, but also to the common-men?

Many surveys have estimated that majority of all drunken driving, rash and other notorious activities takes place with drivers who do not have a valid driving licence. Unlicensed [3] and underage driving has also been on a rise [3]. Additionally, Vehicle thefts occur every 40sec added by insurance costs soaring at several billion$. In Mumbai alone, 18000 vehicles are stolen out of 150000 in 2014. Alas, even traffic officials dealing with cumbersome paperwork and receipts [6] leads to even greater misery. A client server android application curbing these menaces and offering a solution *for the officials, with the officials* is the whole objective in this paper. A very general block diagram is as shown in Fig 1.

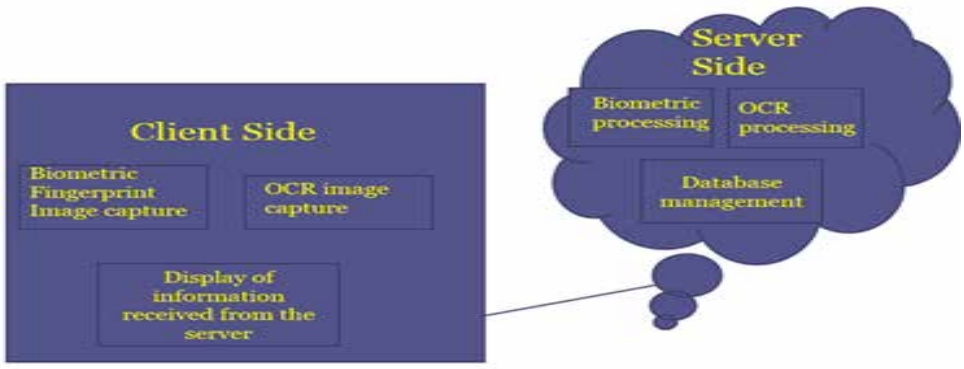

Fig. 1 Block Diagram of the Client and Server Side BIS.

II. OVERVIEW OF THE SYSTEM

The compelling characteristics providing an insight into the aspects of fingerprint biometrics are speciality-traits, accuracy and stability[2]. These form the main basis for further and detailed analysis. The steps involved in the whole process are:-

2.1 Wireless Access Using Socket Programming

Using IP address of the server, the login is made successful using socket programming. It requires an ad-hoc wireless network for fast fingerprint image transfer between the client and the server.

2.2 Peripheral Scanner

The peripheral device used is USB Fingerprint scanner: Nitgen Hamster DX for authentication, identification and verification functions[11]. The model used is HFDU-06[10] having technical specifications of 5V, 120 mA.

2.3 Procedure of Sensing

The classical and customary "ink and paper" method [11]was highly cumbersome. In the more popular live-scan method [11], the digitized image is gained by setting the thumb on the scanner. The process consists of acquiring the fingerprint image from the fingerprint scanner. Once the image is acquired, it is transferred to the Android Tablet used supporting OTG connectivity. Once the image is transferred to the tablet, it is then transferred to the server for further processing. The tablet should have two important features: one, it should possess a driving capability of equal or more than the scanner and two, it should possess the "OTG"(On the Go) connectivity.

2.4 Phases of Usage

The different phases [15] involving system are:-

2.4.1 Enrolment Phase

During this phase, the scanner scans the driver's fingerprint and converts it into a digital image. The subtle distinctive points (ridge endings and bifurcations) are then extracted using MINDTCT and based upon this information, they stored into a file(stored template) used for further processing using BOZORTH3 algorithm explained later.

2.4.2 Corroboration Phase

In this phase, once the user touches the same sensor, generating a new fingerprint image called a test template [11].This then generates numerous minutiae files, and the matching module compares it with the stored minutia template (single template only) in the enrolment database.

2.4.3 Discerning Phase

In this phase, if the test fingerprint when matched with the stored templates generates a matching score above an optimal one, it is then considered to be the expected result and further processing commences verification as shown in Fig.2.

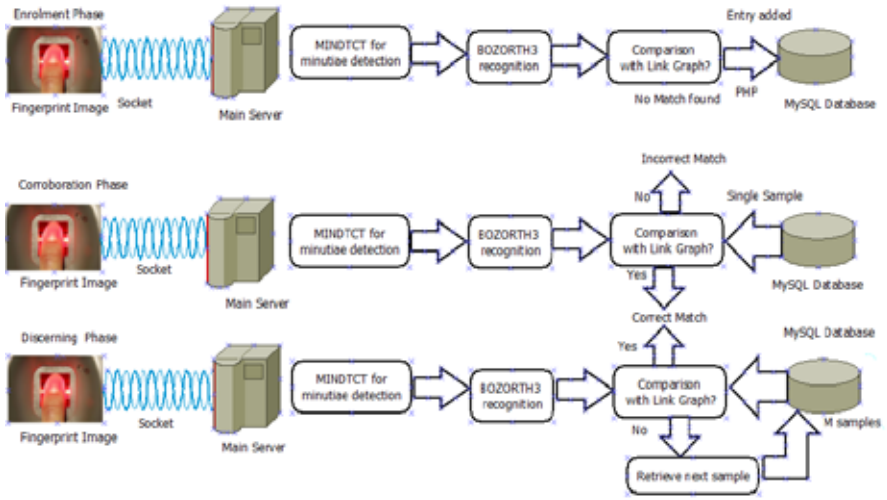

Fig. 2 Phases of Usages.

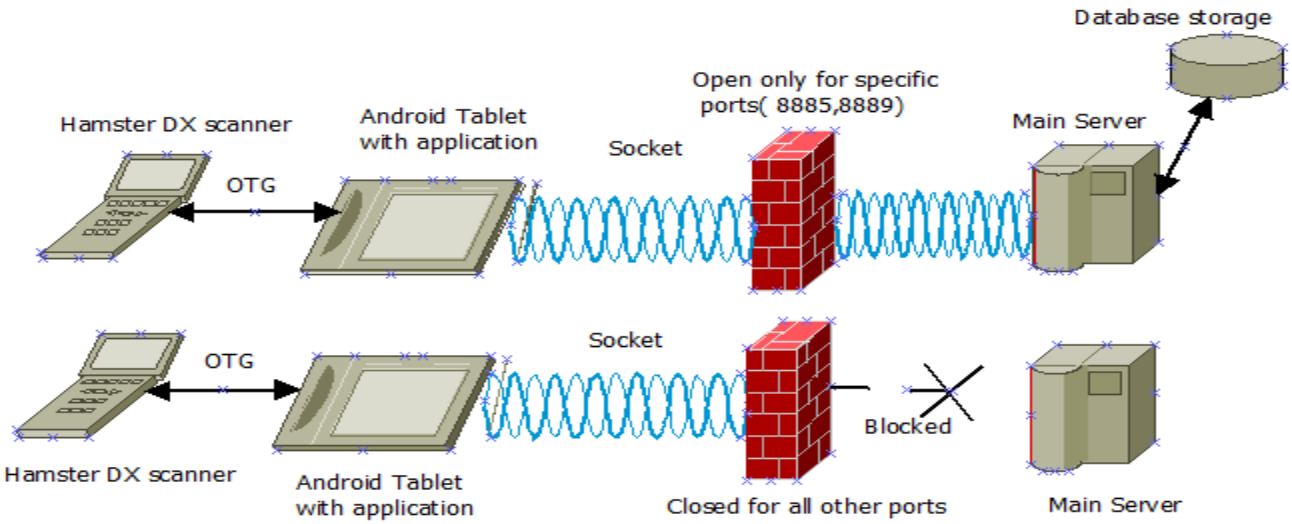

Fig.3 Process of Sensing Via the Tablet to the Remote Server

2.5 Fingerprint Processing Using Cygwin

Cygwin distribution provides numerous packages [19] of popular GNU tools and other headers, libraries for building and porting of applications. Following is the work of Cygwin for performing fingerprint processing:-

2.5.1 Mindtct

It was developed and still used by FBI's Universal Latent Workstation [14] which stands for "Minutiae Detection". For a given fingerprint image, [8]it determines the parameters necessary for further deduction which are location, orientation, quality and type. It uses these values for uniquely identifying the numerous fingerprints from the available samples found in the file folders in the main server. Minutiae are those specificities or the distinctive points which distinguish the sample points. Detection of these points thus forms one of the most important directive steps in the phase of fingerprint processing.

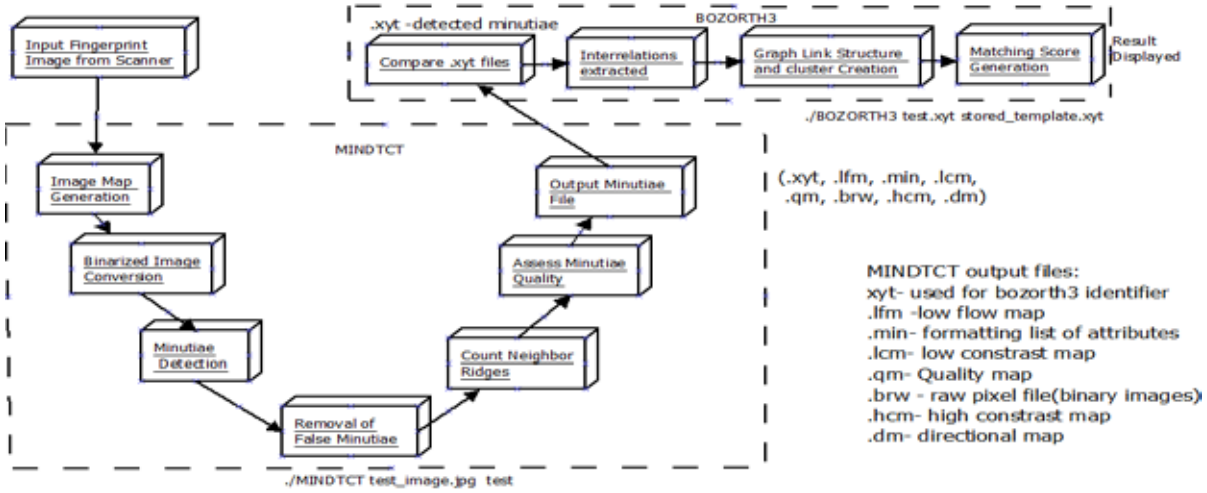

Fig.4 MINDTCT and BOZORTH3 operation

Command: ./MINDTCT [-b] <img_name> <oroot>S 1

As shown in (1); -b means image enhancement on low constrast images (optional). Image name means input name of the fingerprint image for processing. Lastly, "oroot" [21] signifies file name of the destination. Once the test image (in JPEG form only and if not, to be converted) is obtained in digitized form, it is subjected to various transformations [14] ,[18]collectively termed as MINDTCT involving:-

2.5.1.1 Image Map Transformation

This involves determining the parameters in the digitized images. These will form the initial basis for distinguishing different samples based on their subtleties.

2.5.1.2 Binary Image Conversion

All digitized images are converted to a Bi (2 level) images for further processing. Images having either high or low level can be subjected to extensive modifications.

2.5.1.3 Minutiae Detection

This phase deals with ridge endings and bifurcations. Each of the samples though similar to naked eyes have their own unique traits which are obtained in this phase.

2.5.1.4 Removal of False Minutiae

It is a very important stage to reduce FMR and others [20]. It involves removing islands, lakes, hooks and minutiae points too wide or too narrow (pores). It is similar to the noise removal in signal processing.

2.5.1.5 Count Neighbour Ridges

The resultant ridge-endings & curvatures are then counted to give a total for each of the samples.

2.5.1.6 Assess Minutiae Quality

This is determined by NFIQ discussed below describing a range of quality guideline numbers.

2.5.1.7 Output Minutiae File

These are the .extension files that are created. Out of these, .xyt containing the position(x, y coordinates), theta and orientation is further used for bozorth3 processing.

2.5.2 Nfiq

It determines the quality of the stored fingerprint images by using .qm (Quality Map) file. It gives output[18]as a series of numbers ranging from 1-5 where :1-Highest Quality 5-Lowest Quality as shown in (2).

Command: ./NFIQ <image_name> 2

2.5.3 Bozorth3

It is written by Alan. S. Bozorth at FBI [18]. The bozorth3 is on basis of minutiae for the matching algorithm and uses with regard to a matching score [14] for the different specific or subtle points and thus differentiates each and every sample by their location, quality, orientation and type. It is rotation and translation invariant [8]. It consists of two different tables for the fingerprint samples known as an Intra-fingerprint Specifics Differentiation Tables (ISDT), a Inter-fingerprint Similarity table (IST) for checking the matches and matching or suiting score(MS) using the IST. This algorithm can be described by the following steps which are:-

2.5.3.1 Isdt's

In this, we determine the relative measurements from one subtle point to all the other known specific (minutiae) points for both the test and stored template sample. By relative measurements, it both means distance and orientation between two minutiae points. The obtained results are stored in the ISDT's.

2.5.3.2 Ist

When the ISDT is created, a IST is created utilizing the parameters in ISDT for each of the two fingerprint samples. IST possesses those "consistent entries" which are "well-matched" entries between the two tables, each for the test and template. By consistent; it means that the matched measurements should be in justifiable forbearance. Basically, the IST holds the entries having very similar interrelations represented as single links in a graph- like structure.

2.5.3.3 Matching Score/Ms

Only and only if the matching score generated is high, will an entry be recorded in the database. The matching algorithm tries to amass all the sets of similar sampled table data entries via traversal into a large interrelated set of samples called as bunch. Thus greater the interrelations among the various bunches, greater the possibility of similarity and greater the MS.

Command: ./BOZORTH3 –A oufmt=sgp –g test.xyt template.xyt 3

The option –A outfmy-sgp displays the two minutiae parameter files to be compared and is optional as shown in (3).

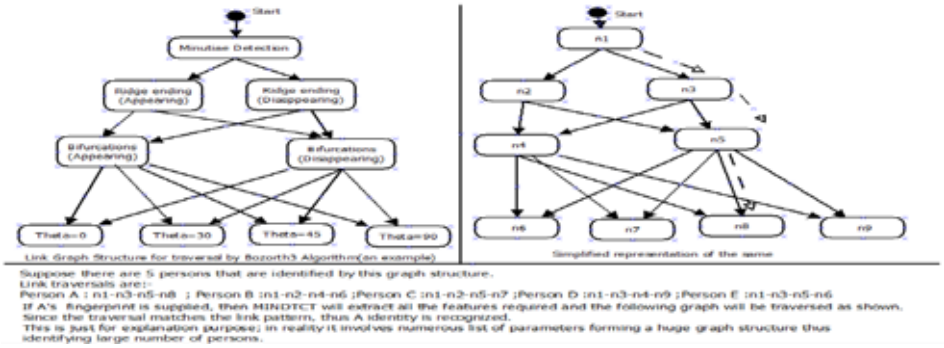

Fig. 5 Bozorth3 Description of Its Working

2.6 Optical Recognition Algorithm

A typical OCR system [9] consists of several components which are optical scanning, segmentation[7], pre-processing, feature extraction and post-processing as illustrated in Fig.6 shown below.

Fig.6 OCR Processing Description

2.7 Database Using MySQL and PHP on Xampp

Once the processing in Cygwin and OCR in Matlab is completed, for a particular match, the corresponding identifier is thrown which is captured and further used for retrieving the tuples in the database. There are 4 different databases namely: Personal_Info, Licence_Info, Vehicle_Info and Offenses.

Personal_Info: ID, PhoneNo, DOB, PhotoImage, Name

Licence_Info: LicenceNo, IssueDate, ExpiryDate, PlaceOfAuth

Vehicle_Info: NumberPlate, Colour, Type, DateOfReg.

Offenses: Name, typeOff, Location, Fine, Date, LicenceNo, Age.

These tables are updated continuously by the admin or some attributes selectively by the users through user interface developed. Due to fingerprint processing, Personal and licence details are retrieved. Due to OCR processing, Vehicle information is retrieved. Based upon the details, offenses are registered. A separate database is kept for number plates which are of 3 types:-

2.7.1 White List

These are the set of registered cars with the corresponding number plates and rightful owners.

2.7.2 Black List

These are the set of stolen cars with their number plates.

2.7.3 Grey List

These are the set of unregistered or unknown vehicle numbers.

2.8 SMS application

There arise two cases which are:-

2.8.1 Driver has reported the vehicle theft

In that case, the driver when reported instantly can be added to the black list. Additional details are also available in the list helping to nab thefts quickly.

2.8.2 Driver Has Not Reported or Unknown of the Theft

In that case, the driver is sent a SMS on his phone/phones to which instantly acknowledgement can be received and thus clarifications are received. Multiple phone numbers will be stored to facilitate the ongoing process. It will also benefit in better reliability in the system and more fault tolerance is achieved.

2.9 How numerous offenses are averted?

When powered with the system processing and android application on the device, this application provides a solution to the following problems:-

2.9.1 No Licence

If the driver caught at road without a licence faces a hefty fine otherwise, but with the application, it is averted.

2.9.2 Vehicle Thefts

A major hurdle is to determine whether a person has borrowed or stolen. It is determined by sending SMS to the specified owner of the vehicle and getting proper notification.

2.9.3 Others

Includes underage driving, unregistered vehicle, no helmet, no seatbelt, mobile driving, rash driving, no park violation, no horn violation, zebra crossing violation, signal break, roadside urination, wrong-side overtake ,no light after sunset, triple seat.

2.10 Data Analytics on Offenses Info

Huge clusters of data provide extensive insights. Offenses having various attributes can be easily mined for generating:-

1) Habitual driving patterns of drivers.
2) Number of offenses and their severity.
3) No. of road mishaps, accretion/decrease in problems and exactly where, what, how, whom?

2.11 Advantages

They are as follows:-

1. The official has all the devices required. No requirement of paper work at all.

2. Vehicle thefts can be prevented by a much reduced rate than the current system.

3. Data analytics on the Offenses Info will help in forming patterns, taking stringent actions and using it as a*"Modus Operandi"*.

III. PROPOSED SYSTEM IN A NUTSHELL

This application provides the official to make new entries of users to the database with the offenses and the number of times they are caught breaking the traffic rules. This basically helps to keep a track on the history of traffic crimes committed by any individuals, which serves the purpose of R.T.O officials.

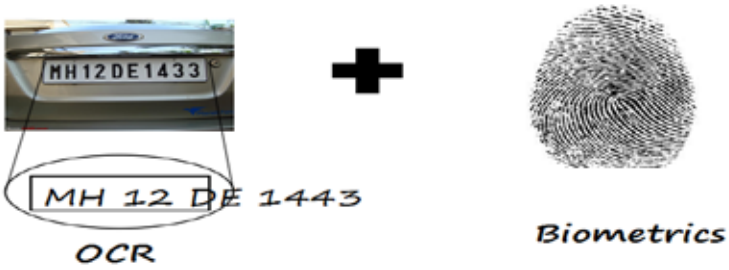

Fig.7 Proposed System Working

The important and most foremost is that there should be relatively no or minimal delay involved. More and more officials should be involved to nab the miscreants at various strategic locations in the various corners of the city. Also, the system is slightly costlier but to counter the outnumbering vehicle thefts would be incomparable indeed. It is essential that the number of vehicle thefts need to be curbed and this system offers a more approachable and crisp solution.

IV. DESIGN ASPECTS

4.1 Class Diagram

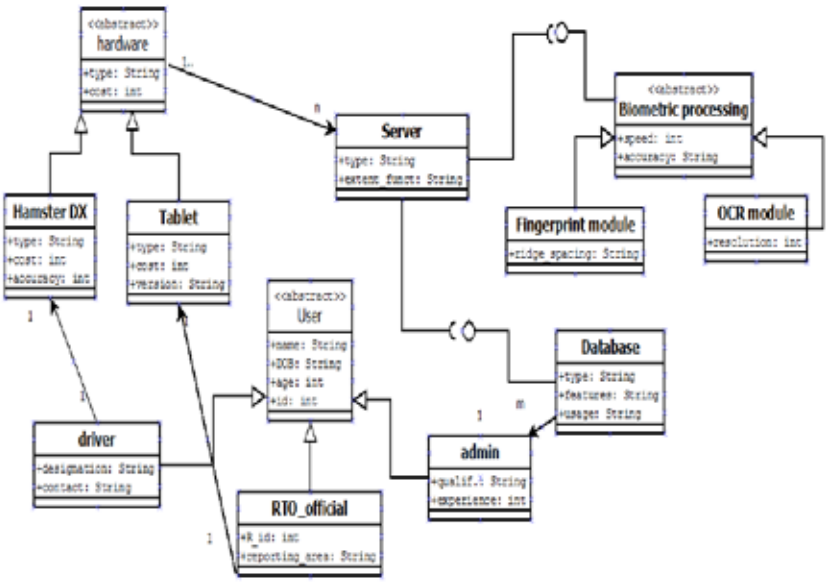

Fig.8 Class Diagram of the system

The class diagram consists of the different classes which are namely the Server, the databases, scanner, the OCR modules and different users of the system. The class diagram denotes the components, connectors and configuration of the system with the client-server Architectural style.

4.2 Flowchart

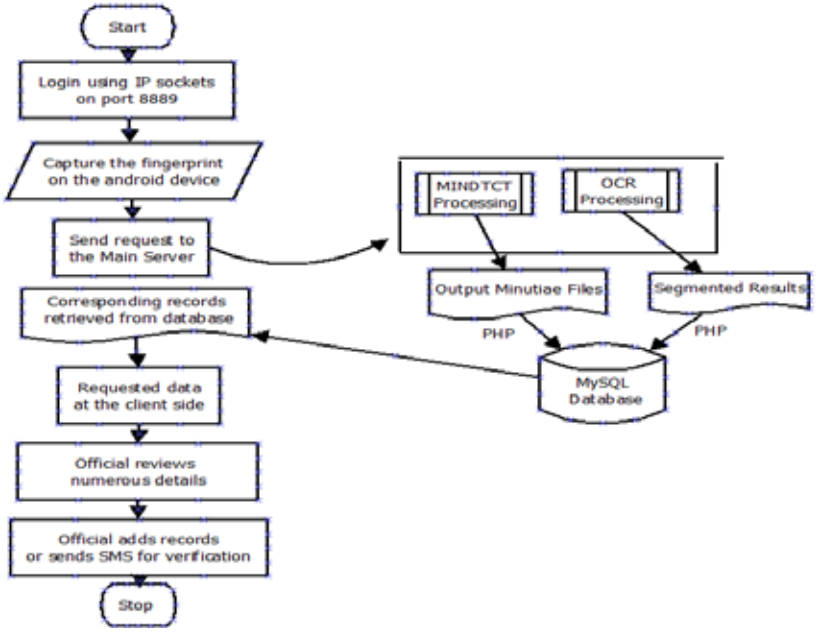

Fig.9 Flowchart of the System

The flowchart of the system consists of the process of the biometric identification system (BIS) involving the peripheral device, the fingerprint recognition module and OCR modules.

4.3 Use Case Diagram

Fig.10 Use Case Diagram

Use case diagram consists of User or driver, both malicious and benign, official, DB specialist and Admin. These are the entities that are interacting with the system. The various use cases implemented are by the individual actors in the system.

V. IMPLEMENTATION ASPECTS

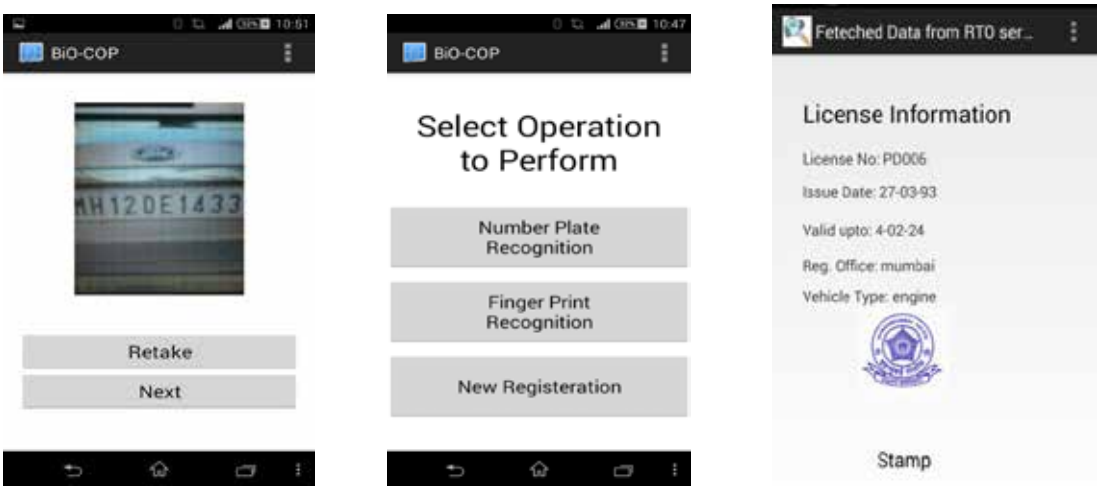

Fig.11 A) Activate Camera For Number Plate Capture. B) Select any of The 3 Options Mentioned. C) Display of Licence Info From The Server

Number-plate Recognition consists of activating the camera and performing the OCR. Fingerprint Recognition consists of obtaining the biometric via a peripheral device and using Bozorth3 algorithm on it. Lastly, a new Registration is added to the main database server for any new inclusions to the already available information. The type of offence is also specified in the new entry as shown in Fig.11.

As shown in Fig.12; it shows some snapshots of the app which would be used by the traffic policeman.

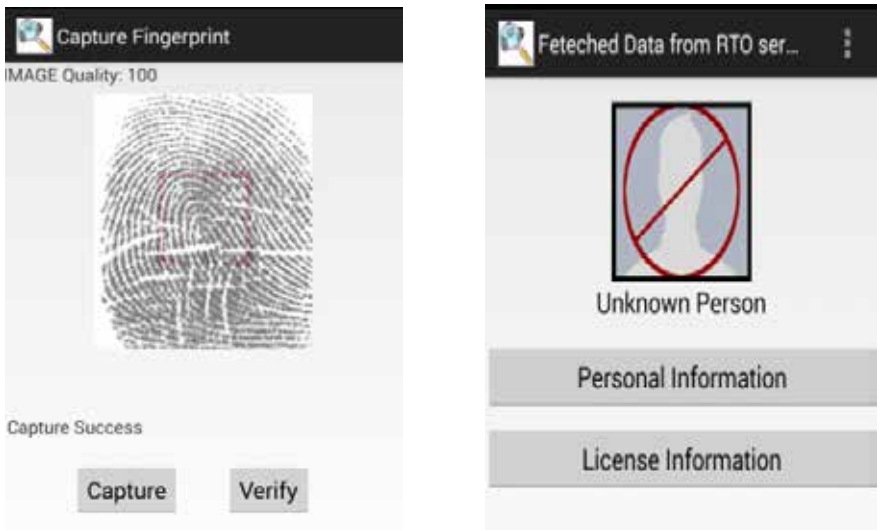

Fig.12 A) Fingerprint Capture; Here Square Box Focuses on Capturing Core Points. B) Not Registered

VI. CONCLUSION

The era of fingerprints continues to be a booming field with its ever growing applications in several domains especially banking and commercial uses. But licence management is still devoid of the advent of mobile biometrics based android app. Unlike the existing system of carrying documents, which can get misplaced, the genuineness of the documents can be verified at any instant, thus this proposed system eliminates the demerits and provides an instantaneous and lucid solution.. This is also supported by Optical Character Recognition

which helps the application to extract details about any vehicle by preventing or reducing any vehicle thefts, offenses, road mishaps and greater misery to what already exists.

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