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DESIGN OF A HIGH SPEED MULTIPLIER BY USING ANCIENT VEDIC MATHEMATICS APPROACH FOR DIGITAL ARITHMETIC

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ABSTRACT

In this paper, an area of efficient multiplier architecture is presented. The architecture is based on Ancient algorithms of the Vedas, propounded in the Vedic Mathematics. The multiplication algorithm used here is called Urdhva Tiryakbhyam Sutra. The multiplier based on the ancient technique is compared with the modern multiplier to highlight the speed and power superiority of the Vedic Multipliers. The author's purpose generalized algorithm for multiplication is proposed through of the Urdhva Tiryakbhyam Sutra from Vedic Mathematics, operating in radix - 2 number system environment suitable for digital platforms. Statistical analysis has been carried out based on the number of recursions profile as a function of the smaller multiplicand. The proposed algorithm is efficient for smaller multiplicand as well, unlike most of the asymptotically fast algorithms. Further, a basic block schematic of Hardware Implementation of our algorithm is suggested to exploit parallelism and speed up the implementation of the algorithm in a multiprocessor environment.

Keywords - Multiplication, algorithm, Vedic mathematics, Urdhva Tiryakbhyam Sutra,digital arithmetic, reduced-bit, Time Complexity.

I. INTRODUCTION

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products [2]. Vedic multiplier is faster than array multiplier and Booth multiplier. As the number of bits increases from 8x8 bits to 16x16 bits, the timing delay is greatly reduced for Vedic multiplier as compared to other multipliers. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Array multiplier, Booth Multiplier is some of the standard approaches used in implementation of binary multiplier which are suitable for VLSI implementation. Delay in Vedic multiplier for 16 x 16 bit number is 14 ns while the delay in Booth and Array multiplier are 37 ns and 43 ns respectively. Thus

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this multiplier shows the highest speed among conventional multipliers. It has this advantage than others to prefer a best multiplier [3].

II. BOOTH MULTIPLIER

The Booth recording multiplier is a multiplier which scans three bits at a time to reduce the number of partial products .These three bits are the two bit from the present pair and a third bit from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the array to control the operations performed by the adder cells. Booth algorithm gives a procedure for multiplying binary integers in signed 2's complement representation on. It operates on the fact that strings of 0's in the multiplier require no addition but just shifting and a string of 1's in the multiplier from bit weight 2^k to weight 2^m can be treated as 2^{K+1}-2^m. Fig 1

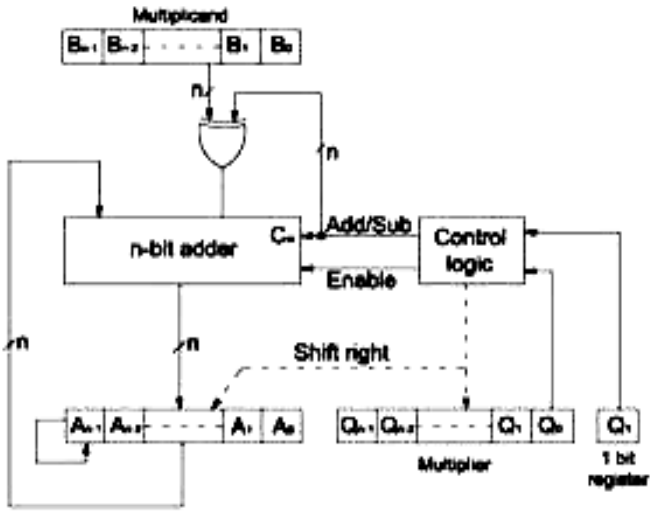

Fig.1 Hardware Implementation Of Signed Binary Multiplication For Booth's Algorithm

shows the hardware implementation for Booth's algorithm. It consists of an n-bit adder, control logic and four registers A, B, Q and Q_{-1}. Multiplier and Multiplicand are loaded into register Q and register B respectively Register A and Q_{-1} are initially set to 0. The n-bit adder performs addition, inputs of adders comes from multiplicand and content of register A. In case of addition, Add/Sub line is 0, therefore, C_{in} = 0 and multiplicand is directly applied as a second input to the n-bit adder. In case of subtraction, Add/sub line is 1, therefore C_{in} = 1 and multiplicand is complemented and then applied to the n-bit adder. As a result, the 2's complement of the multiplicand is added to the contents of register A. The control logic Scans bits Q_0 and Q_{-1} one at a time and generates the control signals to perform the corresponding function. If the two bits are same (1 1 or 0 0), then all the bits of A, Q and Q_{-1} registers are shifted to right I-bit without addition or subtraction (Add/Subtract Enable = 0). If the two bits differ, then the multiplicand is added to or subtracted from the A register, depending on the status of bits. After addition or subtraction right shift occurs such that the left most bit of A (A_{n-1}) is not only

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shifted into A_{n-2}, but also remains in A_{n-1}. This is required to preserve the sign of the number in A and Q.The flow chart of Booth's algorithm for signed multiplication is shown in Fig 2.

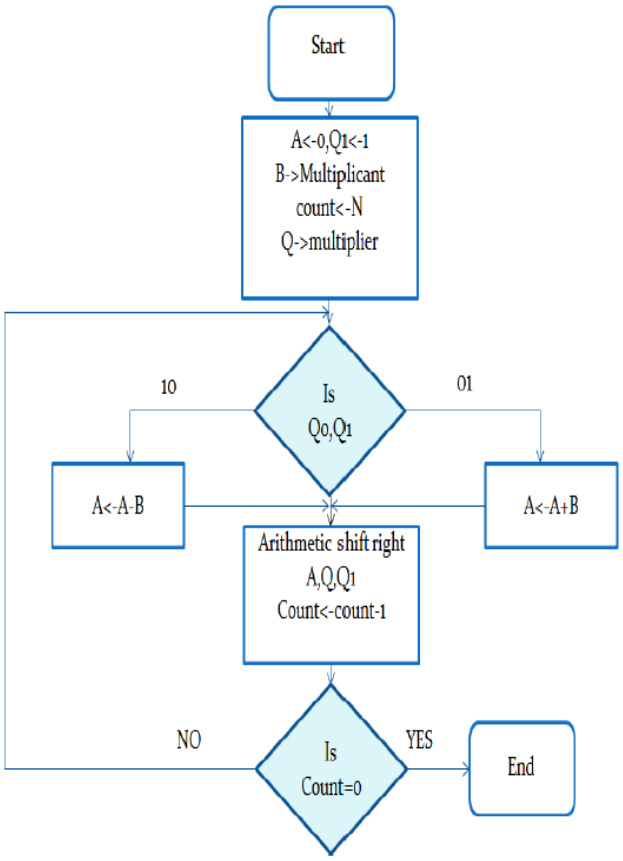

Fig.2 Flow Chart Of Booth's Algorithm For Signed Multiplication

III. VEDIC MULTIPLICATION TECHNIQUE

What we call VEDIC MATHEMATICS is a mathematical elaboration of **'Sixteen Simple Mathematical formulae from the Vedas'** as brought out by Sri Bharati Krishna Tirthaji. The use of Vedic mathematics is to reduces the typical calculations in conventional mathematics to very simple one. Because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

Urdhva Tiryakbhyam Sutra

The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital

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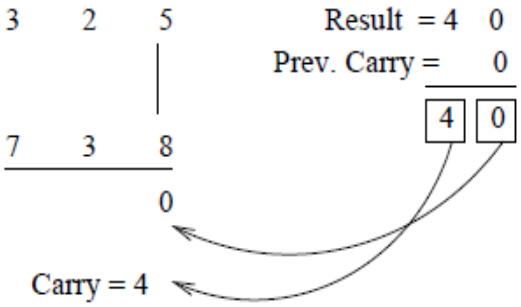
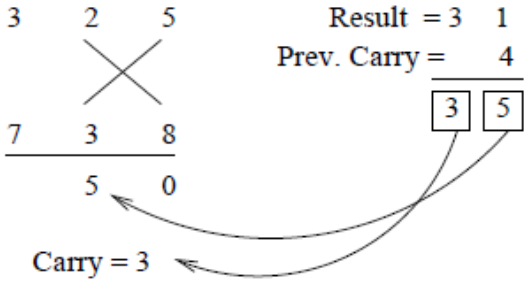
hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and Crosswise*".

To illustrate this scheme, let us consider the multiplication of two decimal numbers 325 x 738 by Urdhva-Tiryakbhyam method. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

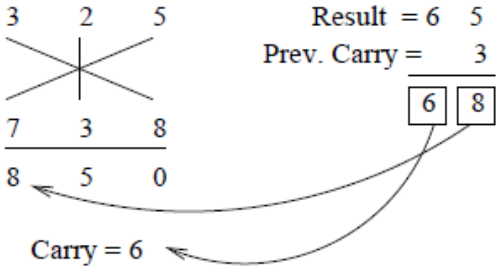
STEP 1



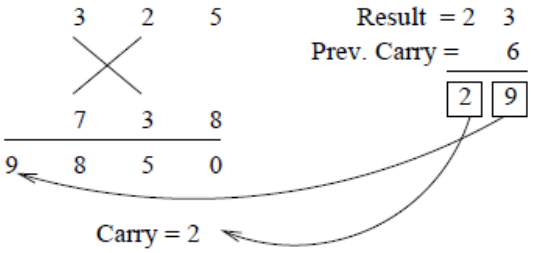
STEP 2



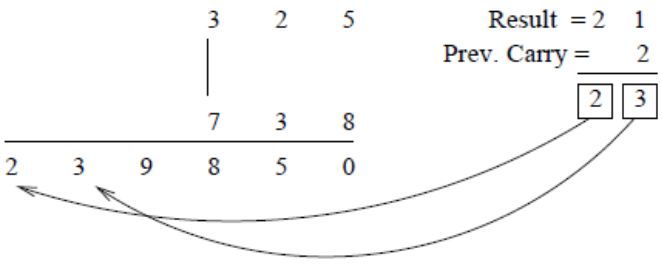
STEP 3



STEP 4



STEP 5



325 X 738 = 239850

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An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig. 3. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

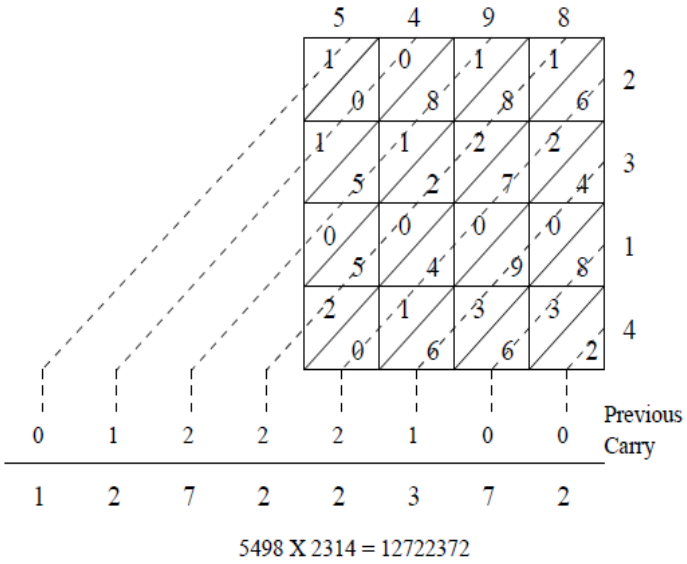

Fig. 3. Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

IV. THE PROPOSED VEDIC MULTIPLIER ARCHITECTURE

The hardware architecture of 4x4, 8x8 and 16x16 bits Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

A. *Vedic Multiplier for 4x4 bit Module*

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To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers $a_3a_2a_1a_0$ and $b3b2b1b0$. As the result of this multiplication would be more than 4 bits, we express it as $---r_3r_2r_1r_0$. Line diagram for multiplication of two 4-bit numbers is shown in Fig. 4 which is nothing but the mapping of the Fig. 3 in binary system. For the sake of simplicity, each bit is represented by a circle. Least significant bit r_0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier. The process is followed according to the steps shown in Fig. 4. As in the last case, the digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result (r_n) and a carry (say c_n). This carry is added in the next step and hence the process goes on. If more than one lines are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all the other bits act as carry. For example, if in some intermediate step, we get 110, then 0 will act as result bit and 11 as the carry (referred to as c_n in this text). It should be clearly noted that c_n may be a multi-bit number. Thus we get the following expressions:

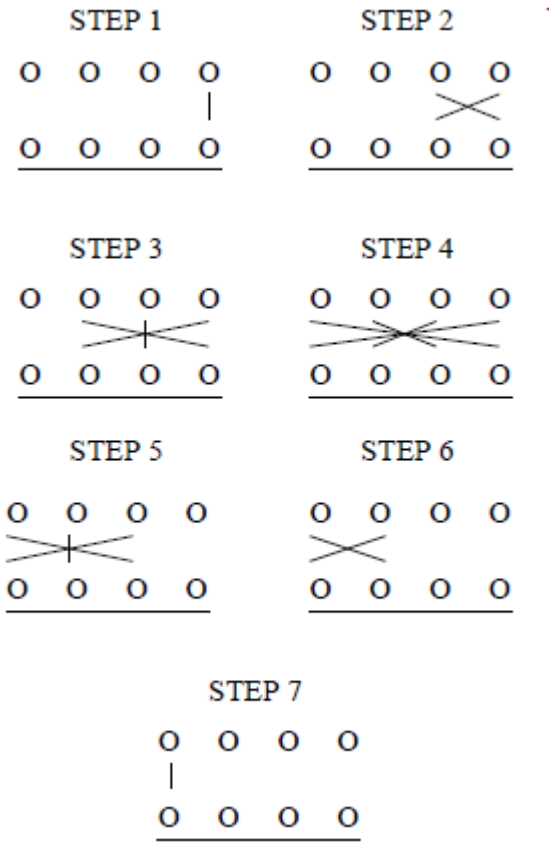

Fig. 4. Line diagram for multiplication of two 4-bit numbers.

$r_0 = a_0b_0;$ (1)

$c_1r_1 = a_1b_0 + a_0b_1;$ (2)

$c_2r_2 = c_1 + a_2b_0 + a_1b_1 + a_0b_2;$ (3)

$c_3r_3 = c_2 + a_3b_0 + a_2b_1 + a_1b_2 + a_0b_3;$ (4)

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$c_4r_4 = c_3 + a_3b_1 + a_2b_2 + a_1b_3;$ (5)

$c_5r_5 = c_4 + a_3b_2 + a_2b_3;$ (6)

$c_6r_6 = c_5 + a_3b_3$ (7)

With $c_6r_6r_5r_4r_3r_2r_1r_0$ being the final product. Hence this is the general mathematical formula applicable to all cases of

multiplication. The hardware realization of a 4-bit multiplier using this Sutra is shown in Fig. 5.

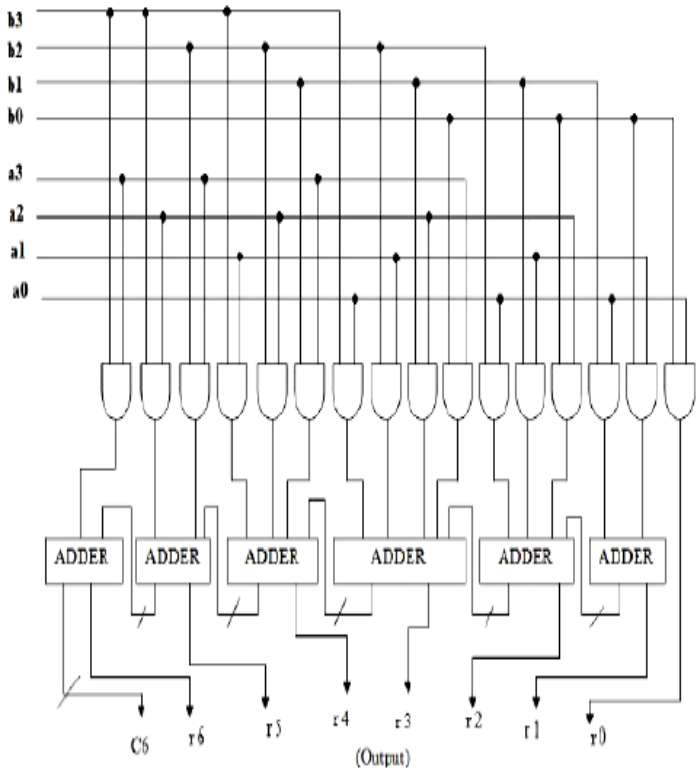

Fig. 5. Hardware architecture of the Urdhva tiryakbhyam 4x4 multiplier.

B. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 8 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. Let's analyze 8x8 multiplications, say A= A7 A6 A5 A4A3 A2 A1 A0 and B= B7 B6 B5B4 B3 B2 B1B0. The output line for the multiplication result will be of 16 bits as – S15 S14 S13S12 S11 S10 S9 S8 S7 S6S5S4 S3 S2 S1 S0. Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

P = A x

B = (AH-AL) x (BH-BL) = AH x BH + (AH x BL + AL x BH) + AL x BL

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Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 6.

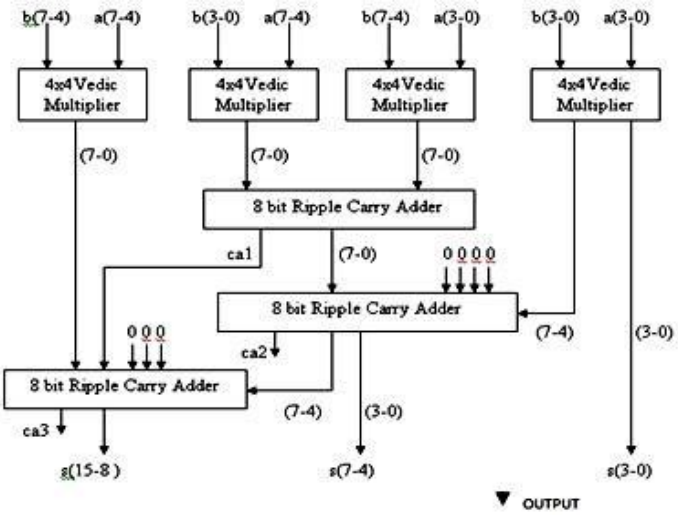

Fig. 6. Hardware architecture of the Urdhva tiryakbhyam 8x8 multiplier.

C. *Vedic Multiplier for 8x8 bit Module*

The design of 16×16 block is a similar arrangement of 8×8 blocks in an optimized manner .The first step in the design of 16×16 block will be grouping the 8 bit (byte) of each 16 bit input. These lower and upper bytes pairs of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8×8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are added in a 16-bit carry look ahead adder optimally to generate final product bits. The schematic of a 16×16 block designed using 8×8 blocks. The partial products represent the Urdhva vertical and cross product [6] terms. Then using or and half adder assembly to find the final product. Power dissipation [7] of this multiplier is 0.18 mW and propagation delay is 6.216 nsec

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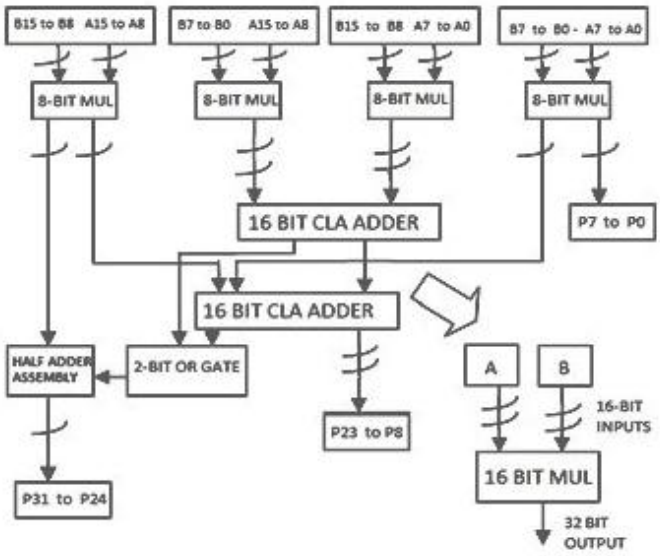

Fig. 7. Hardware architecture of the Urdhva tiryakbhyam 16x16 multiplier.

V. IMPLEMENTATION ON XILINX SOFTWARE

In this work,16x16 bit Vedic multiplier is designed in verilog (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done in XilinxISE13.2i - Project Navigator and ISim simulator integrated in the Xilinx package.

The performance of circuit is evaluated on the Xilinx device family Spartan3, package vq100 and speed grade -4.The RTL schematic of 16x16 bit Vedic multiplier. For 16x16 bit Vedic multiplier input, the multiplier x="1111000011110000" (decimal number system)

And

Multiplicand y="0000111100001111" (decimal number system)

And we get 16-bit output

p=00001110001011000010111000010000 "" (decimal number system).

VI. HARDWARE IMPLEMENTATION

After the programming is done in the XILINX software the hardware part comes into account. To see easily the output of multiplication we have executed the output on FPGA (Field Programmable Gate Array) kit. The kit is having many LED's which we are using for input and output purpose. One port is attached to the kit and the other port is attached to the CPU. After the program is downloaded we will see different combinations of 16X16 bit multiplication. The use of this FPGA kit is that the user will see the output easily.

VII. RESULTS

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The result of the 16X16 Vedic multiplier is given in the figure's below in which 16 bit number is in binary and decimal form. Also the RTL schematic of Vedic and Booth multiplier is given.

VIII. COMPARISON OF DEVICE UTILIZATION BETWEEN BOOTH'S AND VEDIC MULTIPLIER

We have compared Booth's and Vedic multiplier on the basis of device utilization which is as given below.

Table 1: Comparison of device utilization theory of 4x4 multiplier

Parameters	**Booth's multiplier**	**Vedic multiplier**
Combination path delay	14.226 ns	5.160 ns
No. of slices	25 out of 3584	15 out of 3584
No. of 4 input LUTs	45 out of 7168	40 out of 7168
No. of bonded IOBs	13 out of 141	20 out of 141

Table 2: Comparison of device utilization theory of 8x8 multiplier

Parameters	**Booth's multiplier**	**Vedic multiplier**
Combination path delay	52.667 ns	20.254 ns
No. of slices	181 out of 3584 (5%)	84 out of 3584 (2%)
No. of 4 input LUTs	325 out of 7168 (4.5 %)	140 out of 7168 (2%)
No. of bonded IOBs	24 out of 141 (17%)	32 out of 141 (22%)

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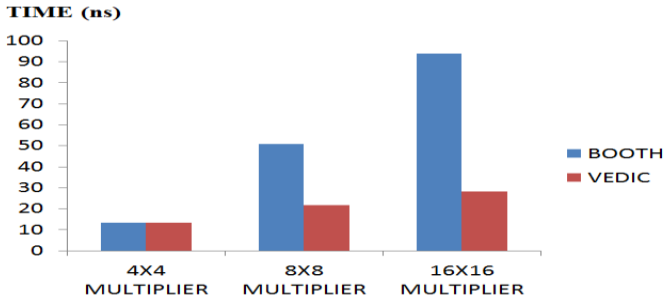
Table 3: Comparison of device utilization theory of 16x16 multiplier

Parameters	Booth's multiplier	Vedic multiplier
Combination path delay	95.85 ns	27.145 ns
No. of slices	705 out of 3584 (20%)	345 out of 3584 (9%)
No. of 4 input LUTs	1280 out of 7168 (17%)	622 out of 7168 (8%)
No. of bonded IOBs	60 out of 141 (42%)	64 out of 141 (45%)

Comparison of Combination Path Delay between Booth's and Vedic Multiplier



IX. CONCLUSION

In this paper we have developed the suitable architecture for multiplication using Vedic multiplier. This multiplier is suitable for multiplication of large number of bits. We compared Vedic multiplier over Booths multiplier and successfully show that Vedic multiplier is more convenient than Booths multiplier. The simulation results clearly shows that the Vedic multiplier is having minimum path delay as compared to the Booth's multiplier also hardware complexity of Vedic algorithm is less than the Booth's algorithm.

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