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AN OPTIMIZATION OF A COMMUNICATION SYSTEM USING PULSE TRIGGERING METHOD

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ABSTRACT

A power optimization of a system is proposed in this paper with pulse triggering method. Now a day's power consumption of systems are strictly restricted with the system specifications. An optimization techniques are reduce the power consumption by modifying logic of the system .In most of digital logics the dynamic power loss plays a vital role. We can save more power by reducing this dynamic power loss. The pulse triggering method solves dynamic power loss without degrading the system performance. Encoder and decoder logic blocks are designed using pulse triggering logic by using pulse triggered flip flops. This pulse triggering method solves conflictions between area and power domains. In this paper we used two frequencies 20MHz and 200MHz. For these frequencies the total hierarchy 75.3% , logic power is53.33% , and signal power is 80% reduced with this method. Veerilog HDL has been used for implement various blocks, simulation has done with modelsim 6.5e and RTL has been done using Xilinx 10.1.

Key words: *power optimization, pulse triggering method, clock gating, disparity*.

I. INTRODUCTION

The VLSI industry growing very rapidly with the advantages of reducing power, speed and area without modifying the given system specifications.The main task in VLSI is to reduce the power consumptions as much as possible. power can be reduced by many methods, clock gating is one of the method to reduce the the power consumption.

Clock gating method reduce the power consumption by reducing the unwanted transitions in the applied clock signal without changing system specifications. In this paper we are used pulse triggering method to save the power.

The communication system consists of encoder and decoder blocks along with parallel to serial and serial to parallel converter with respective.

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II. LOW POWER METHOD

Low power optimization method can be achieves at many levels in vlsi

Design level	Optimization method
Operating system level	Portioning, power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining,redundancy,data encoding
Logic level	Logic styles, transistor size and energy recovery
Technology level	Threshold reduction, multi threshold device

III. POWER DISSIPATION

In logic circuits power dissipation can be classified into

i. static power dissipation.

biodynamic power dissipation.

mostly static power dissipation almost zero for cmos logics. So dynamic power plays crucial role in power consumption mechanism. Dynamic power loss expressed as

$P_{Dyn}= \quad C_L .VDD^2. F_{CLK}.$

Where CL is load capacitance, FCLK is max clock frequency From above expression it is clear that dynamic power directly related to clock frequency if clock frequency increases dynamic power also increase in accordance with clock frequency.

IV. SYSTEM DESIGN

Many of data transmission circuits are using 8b/10b encoder/decoder circuit for making accurate data transmission. The main purpose to use this 8b/10b encoder/decoder is able to making reliable transitions for clock recovery easily.

Features of 8b/10b encoder and decoder:

- 8b to 10b encoder and 10b to 8b decoder.
- Previous octet disparity input and current disparity output.
- Output to indicate when invalid ASCII character is requested to be encoded.
- Output to indicate when invalid data/control character is received.
- Running disparity checking.
- Conform to 8b/10b specified in IEEE 802.3z and ANSI X3.230-1994.

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The 8b/10b coding theme was at first planned by albert X. Widmer and Peter A. Franaszek of IBM Corporation in 1983. This cryptography theme is employed for high-speed serial information transmission. The encoder on the transmitter aspect maps the 8-bit parallel information input to 10-bit output. This 10-bit output is then loaded in and shifted out through a high-speed Serializer (Parallel-in Serial-out 10-bit Shift Register). The serial information stream are going to be transmitted through the transmission media to the receiver. The high-speed Deserializer (Serial-in Parallel-out 10-bit Shift Register) on the receiver aspect converts the received serial information stream from serial to parallel. The decoder can then remap the 10-bit information back to the initial 8-bit original information.

4.1 Block Diagrams And Implementation Guidelines

The encoder and decoder logic circuits are showed in fig1 and fig2. From those figures it is clear that the clock latency of encoder is 2 and clock latency of decoder is 3.these latency provides a reliable data transmission and also which increases the throughput of the system. The data inputs will be sampled at positive edge(or negative edge) when the set up/hold time of clock satisfied as seen in fig3.

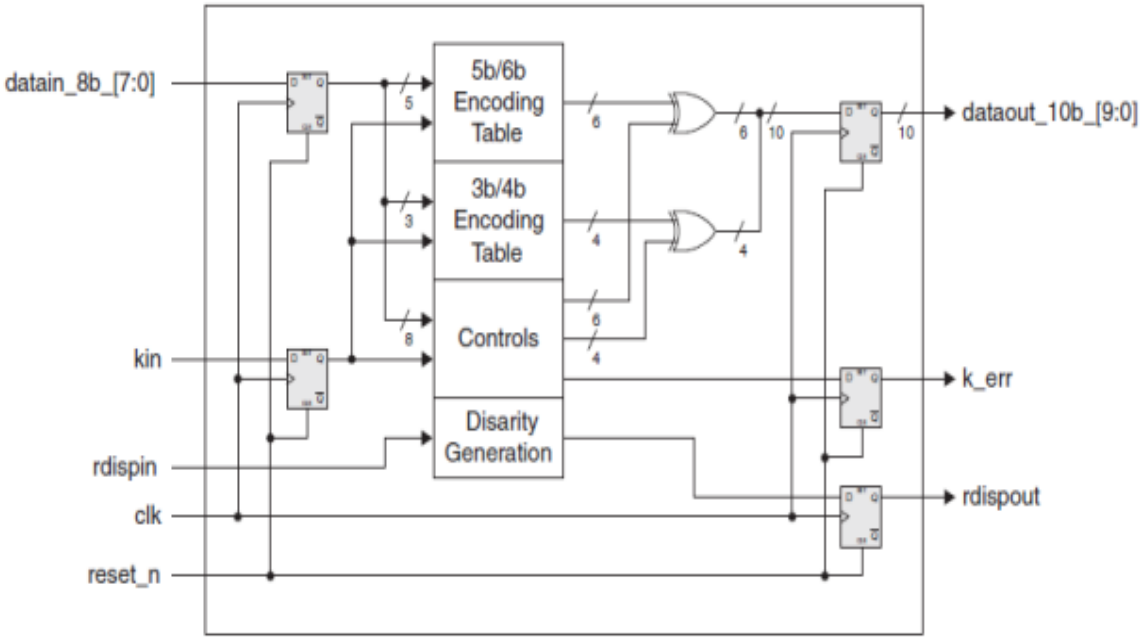

Fig1: Transmitter block

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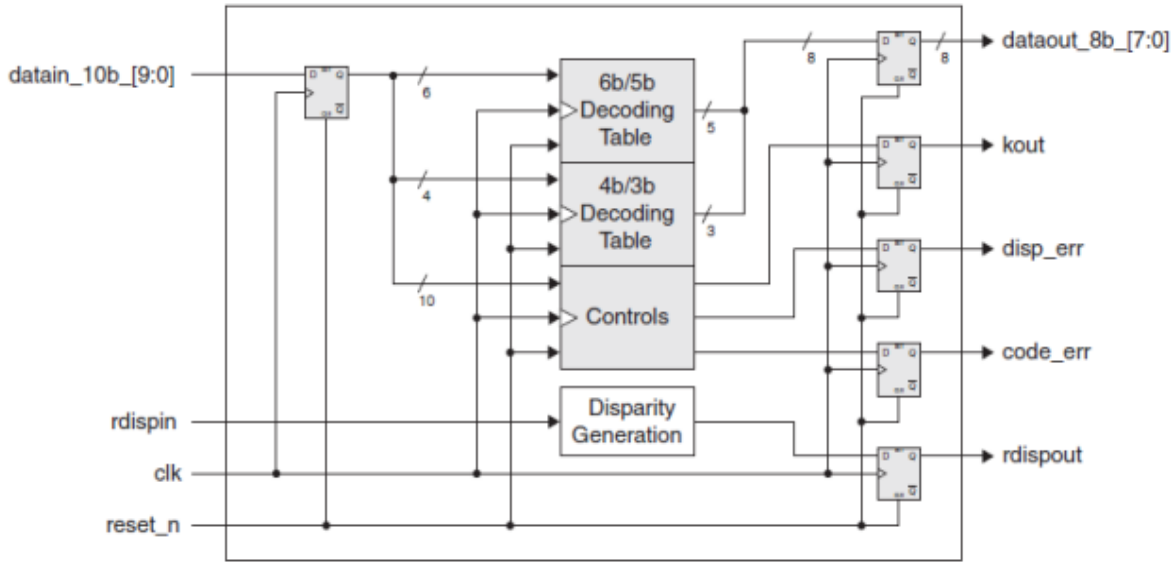

Fig2: Receiver block

V. CLOCK GATING TECHNIQUE

clock gating method is one of the power optimizing method, in this method the un used clock transitions are eliminated and produce a global clock signal without changing the performance of the system.

By reducing the clock transitions in the logic the dynamic power consumptions are reduced. The clock gating can be achieved with many logics like

And gating logic

OR gating logic

Mux based logic

Latch based logic

F/F based logic and more.

Clock gating is a prominent procedure utilized as a part of numerous synchronous circuits for diminishing element power dissemination.

The addition of clock is to the gates able to rational spares power and also able to prune the clock tree. Pruning the clock tree to the modules of the hardware make it handicaps so that the flip flop failures don't need to change the state which means reduce the un necessary transitions(states).

The clock gating block diagram is showed at fig4.

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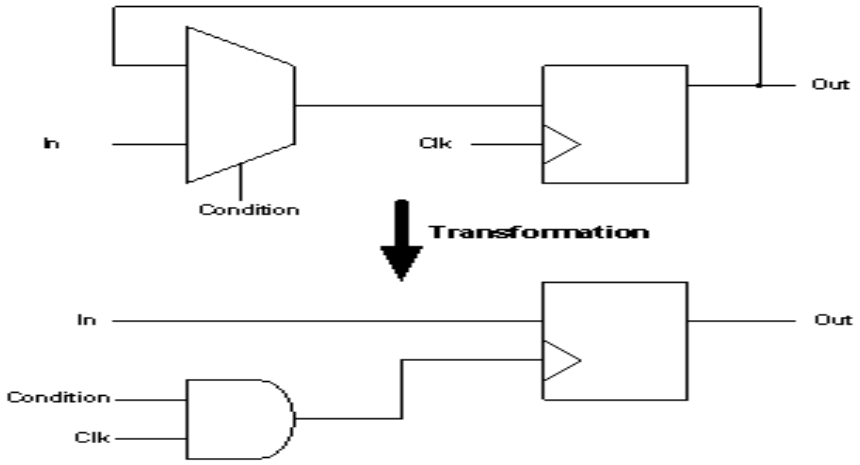

Fig4:clock gating(AND logic)

VI. PULSED CLOCKS

The conventional delayed pulsed clock circuits can be used to save the AND gates in the delayed pulsed clock generator in Fig. 5. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits

to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 4 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

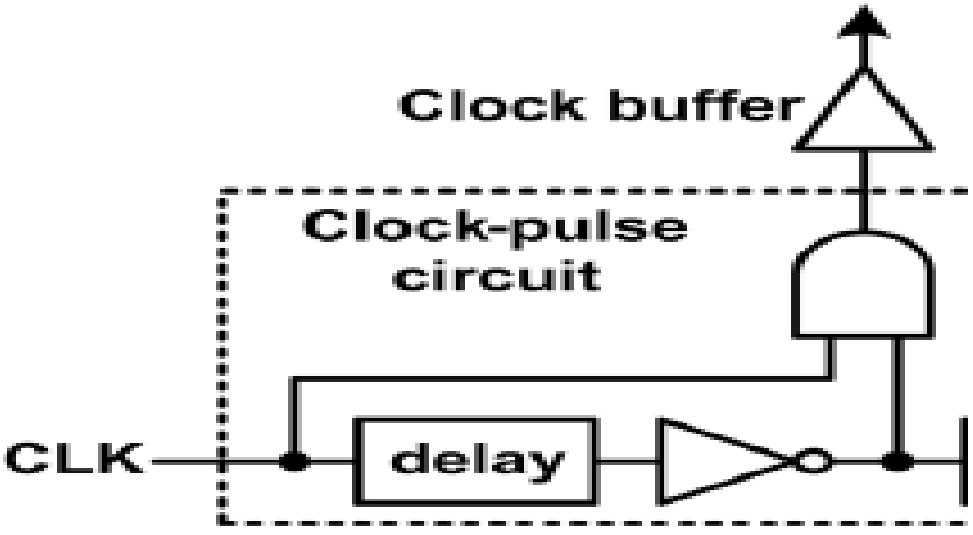

Fig:5 pulsed clock

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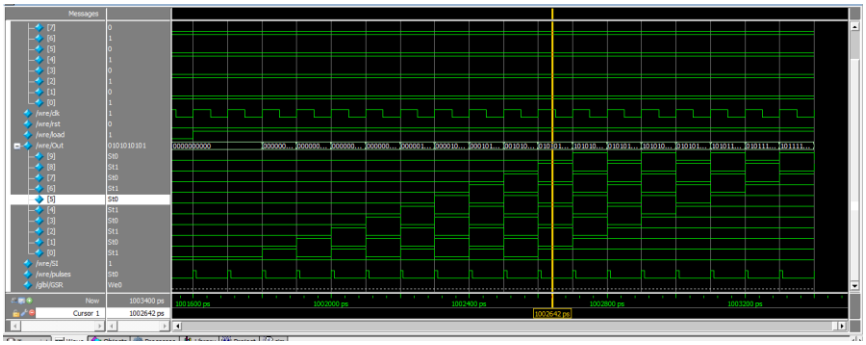
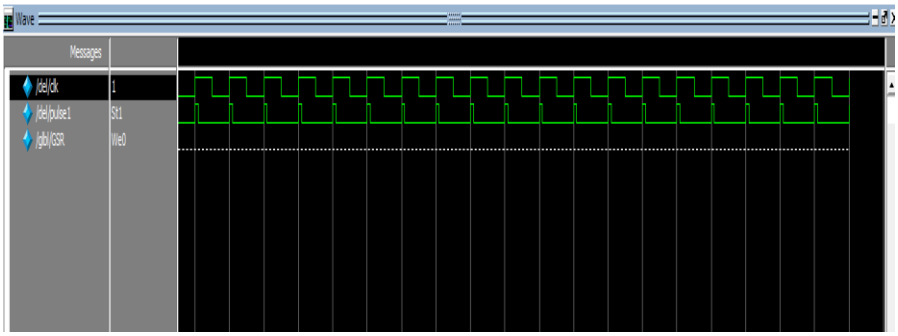
VII. SIMULATION RESULTS

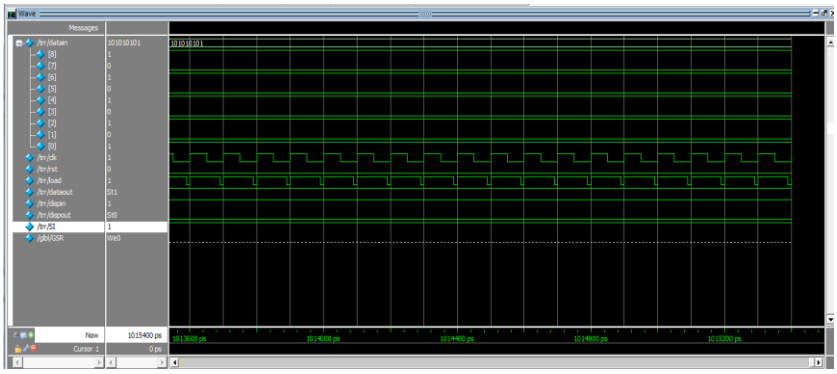
To implement this communication system and their modules a verilog HDL is used. The simulation results for 8b/10b encoder /decoder, shift register (SIPO,PISO) ,clock pulse generator are showed below.



Waveform for shift register



Waveform for pulsed clocks



Waveform for encoded

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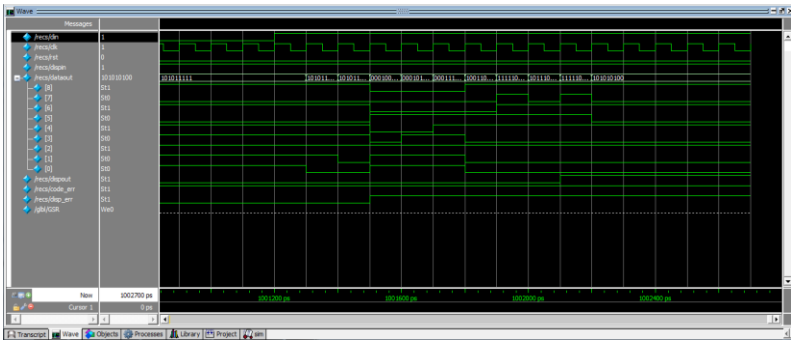
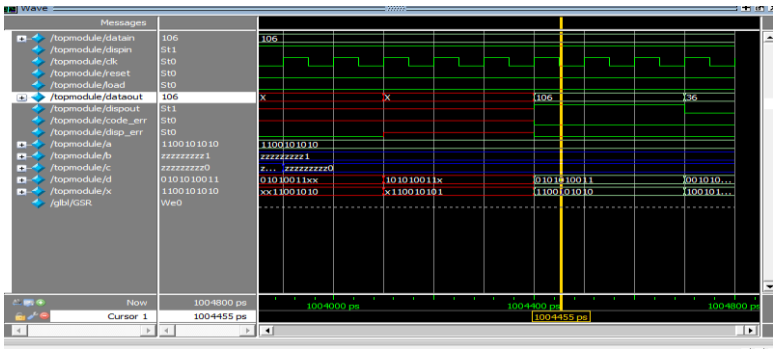


Waveform for decoded



Final design waveform

7.1 Power analysis

Types of design blocks	Clock gating Power analysis	Pulsed clock power analysis
encoded	241mW	241mW
decoded	249mW	249mW
Communication systems	25mW	mW

7.2 Delay analysis

Types	**Delay**
Clock gating based communication system	13.632ns
Pulse generator based communication systems	9.41ns

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VIII. CONCLUSION

Communication system with clock gating technique and pulsed clock technique by using Xilinx ISE suite 10.1 Xpower Analyzer. The power consumed by the communication system with gated clock and pulsed clock illustrated in Table 1. In this table we compare the different power and found that using pulsed clock technique we can reduce the power consumption to an extent without degrading the performance of the system.

REFERENCES

[1] A.X.Widmer, P.A.Franaszek, "A DC-Balanced Partitioned-Block, 8B/10B Transmission Code" IBM J.RES. DEVELOP Vol.27, No.5, and September 1983.

[2] Jagrit Kathuria, M. Ayoubkhan, Arti Noor, MIT International Journal of Electronics and Communication Engineering, "A Review Of clock Gating Technique", MIT Publications, ISSN 2230-7672, Vol 1, No.2, Aug 2011.

[3] Gajendra Singh Solanki, Rekha Agarwal, Sandhya Sharma, "Power Optimization of High Speed Pipelined 8B/10B encoder", International Journal of Innovative Technology & Exploring Engineering, Vol.3, No.7, December 2013

[4] Mohammad Maadi, "An 8b/10b Encoding Serializer/Deserializer (SerDes) Circuit For High Speed Communication Application Using a DC Balanced, Partitioned Block, 8B/10B Transmission Code", International Journal of Electronics & Electrical Engineering, Vol.24, No.2, April 2014.

[5] Kanika Sahni, Kiran Rawat and Sujata Pandey, "Power Optimization of 8b/10b Encoder Decoder Used For High Speed Communication" IEEE Conference, ICIIS, ABV IIITM Gwalior, Dec 2014, in press.

[6] Kanika Sahni, Kiran Rawat and Sujata Pandey, "A Low Power Approach for Implementation of 8B/10B Encoder and 10B/8B Decoder Used for High Speed Communication" IEEE Conference ET2ECN, NIT Surat, Dec 2014, in press.

[7]. Power Optimization of Communication System Using Clock Gating Technique