7th International Conference on Recent Innovations in Science, Engineering and Management
The Institutions of Engineers, Delhi State Center (India)
16th September 2016, www.conferenceworld.in
RISEM - 16
ISBN : 978-93-86171-07-8

PERFORMANCE ANALYSIS OF ANALOG BIST USING BODY BIASING TECHNIQUES

M.Ashok kumar[1], M.Greeshma[2]

[1]M.Tech student, [2]Assistant proffessor M.Tech

[1,2] C.R.Reddy College of engineering, eluru, west godavari district, Andhra Pradesh, (India)

ABSTRACT

A device core logic testing of analog signals with minimal area overhead for measuring on chip voltages in digital circuits can be adopted by BIST(built in self test) in a distributed architecture. Here for measuring this analog voltage, the sub sampled signal pair is fed to delay measurement to measure the skew between this pair. The routing of analog signals over long paths can be minimized by using clock gating. A clock is routed serially to the nodes of analog test voltage with consists of delay cells, flip-flops. However the test voltage to a scheme between The variable body biasing reducing the static power consumption. The Simulation is done by cadence virtuoso tool at 0.18um technology to reduce power dissipation

I. INTRODUCTION

In analog circuits BIAS VARIATION is a common problem and it's getting worse as the technology scales. In here the variation of process is increasing, and reduces the power supply. Increased popularity of mixed signal IC designs in the deep submicron process, to precisely measure analog voltages for testing & debugging process. When measuring on-chip voltages such situations arise in BIST applications, while measuring voltages at the terminals of sleep transistors for power monitor applications and in measuring low bandwidth signals in sensor systems. These analog voltages could be potentially located all over the chip. For displaying analog signal waveforms using the technique of subsamlping. For viewing waveforms in laboratory this method is well suited. For automated testing it cannot be used directly Techniques of analog routing, wherein voltages and/or currents to be measured in some internal circuitry are literally “scanned” out to test pins, have been proposed [5], but here analog circuits are used to route analog voltages/currents, which can themselves lead to signal distortion during propagation. It is hence desirable to have testing circuitry that is simpler than those being tested. Analog routing with digital interface has also been proposed [6], where an analog voltage is digitized and the bits are scanned out through a single pin. Similarly, one can also scan in digital bits and excite circuits with analog voltages using a digital-to-analog converter (DAC). But with reducing power supply voltages in the deep submicrometer technology nodes, leading to reduction in the available voltage headroom, designing conventional ADC architectures for such applications is becoming increasingly difficult. However, in the case of time-based architectures, time resolution has improved since the transition time of digital signals has reduced

RISEM - 16
ISBN : 978-93-86171-07-8

with technology scaling [7]. The all-digital nature of time-based approaches offers itself for scaling and suits the stringent area and power specifications.

Day by day the advancement in technology leads to increase in the number of transistor count on any digital logic design .This increase in transistor count have an sever impact on power consumption because adding more and more transistor will give rise in the heat dissipated in the device [1]. Now a days the era is revolving around portability, is offered by low power consuming system ,Since most of the portable devices are battery driven the power consumption of these devices must be low so the battery life improves, performance improve, reliability improve s and reduces heat removable costs. Because of these reasons the optimization for lower power dissipation and faster device performance is of prime concern in any design. The ideal design is one which consumes minimum power, requires minimum area but has the highest throughput. However, these parameters (area, speed and power) are often in disagreement and a suitable solution for this is to maintain a tradeoff between these parameters. At every level of digital design flow there is a possibility in optimization of power even though benefits are good at the algorithmic and architectural design level. In Modern day microprocessors design, maximum speed and low power with minimum area are main design constraints to meet performance requirement with technology. An Arithmetic and logic unit (DFF) is a digital electronic circuit that performs arithmetic and bitwise logical operations on integer binary numbers. DFF is the heart and crucial building block of all computationally intensive units such as central processing unit (CPU), Floating point unit (FPU) and Graphical processing unit (GPU), almost always falls in the data path during the execution of an instruction decoded by instruction decoder. To meet these requirements, a power efficient, high performance DFF need to be designed. Hence the power consumption of the DFF should be kept at a minimum.

II. RELATED WORKS

Each sampling head consists of a pair of identical delay cells (V2D) and a pair of flip-flops (DFF), as shown in Fig. 1(b). A clock signal is routed serially to all the sampling heads, which is fed to both the delay cells in the sampling head. The delay of one element of the pair is controlled by the analog voltage VAi , and that of the other by a reference voltage *V*ref. Thus, a voltage difference between the node voltage and reference shows up as a delay difference in the clocks at the output of the delay cell pair. This pair of clocks is sampled by a slightly slower sampling clock, giving rise to a pair of beat frequency signals. We call them the subsampled signals, and the skew between them is "amplified" by this process of "subsampling" As can be seen from Fig. 1, both the input clock (clk) and sampling clock (samp clk) are "picked up" from a single point for each sampling head. Hence, crosstalk and coupling noise that may affect the clocks do not contribute to additional noise in the sampling head circuitry. Also, the output subsampled signal pair of the sampling head are low-frequency signals and the skew between them is already amplified by the "subsampling" process, which makes the subsampled signal pair also immune to crosstalk and coupling noise. Another possible approach for the same setting, proposed in [15], although reduces the number of flip-flops used, has the limitation that nodes that do not contribute to signal information may end up adding to the noise since the subsampled signals are daisy-chained through all the sampling heads. This technique of subsampling provides bandwidth/resolution tradeoff, i.e.,

RISEM - 16
ISBN : 978-93-86171-07-8

measurements requiring coarser resolutions can be done faster whereas finer resolution measurements need more time.

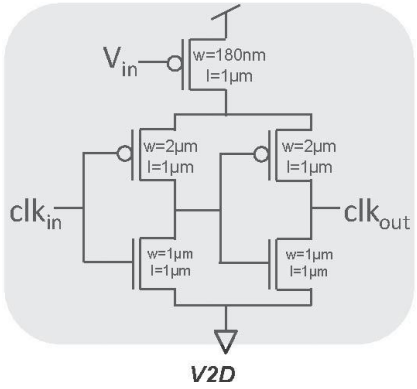

Fig:1 V2D Circuit.

III. VARIABLE BODY BIASING

The proposed structures are combination of forced stack and sleep with variable body bias technique. The sleep transistor technique retains the logic state of circuit while forced stack maintains the minimum delay penalty. Thus this reduces the leakage power while saving the logic state. There are two modes of operation, active mode and sleep mode. The SSVBB has a structure merging forced sleepy stack with variable body biasing technique. The sleepy stack divides the existing transistors into two halves while maintaining the input capacitances. Then the sleep transistors are added in parallel to stacked pull up and pull down transistors. During active mode, s=0 and s'=1 are asserted, thus all sleep transistors are turned on thus reducing circuit delay. The performance is improved as the body to source of the PMOS is ON, which lowers the Vth of PMOS transistor again. Due to body effect, Vth decreases thus increases the performance. As the sleep transistors are always on there is faster switching time than the forced stack. During sleep mode, s=1 and s'=0 are asserted, so both of the sleep transistor are turned off, thus maintaining the logic state of the circuit. As a result of body effect, Vth increases, which decrease the performance.

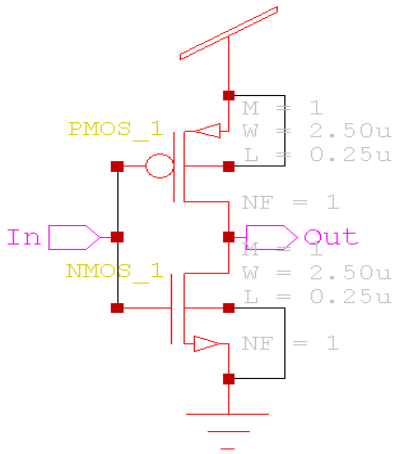

Fig2: Body Biasing Techniques

RISEM - 16
ISBN : 978-93-86171-07-8

IV. RESULTS AND SIMULATION

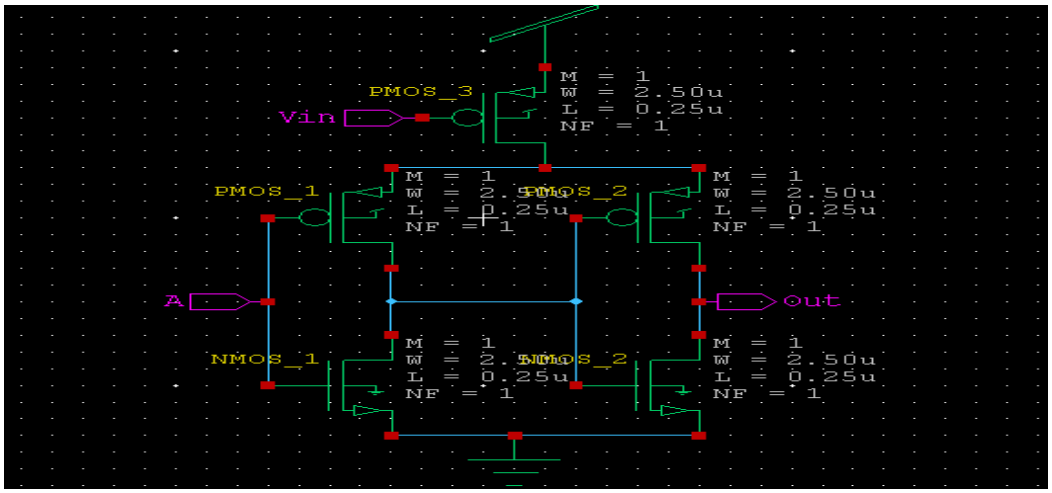

Fig3: V2D Circuit

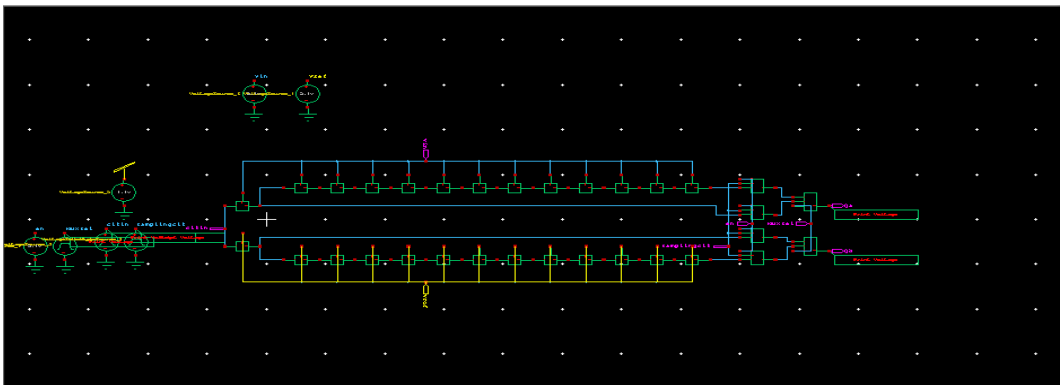

Fig4: BIST Full Setup

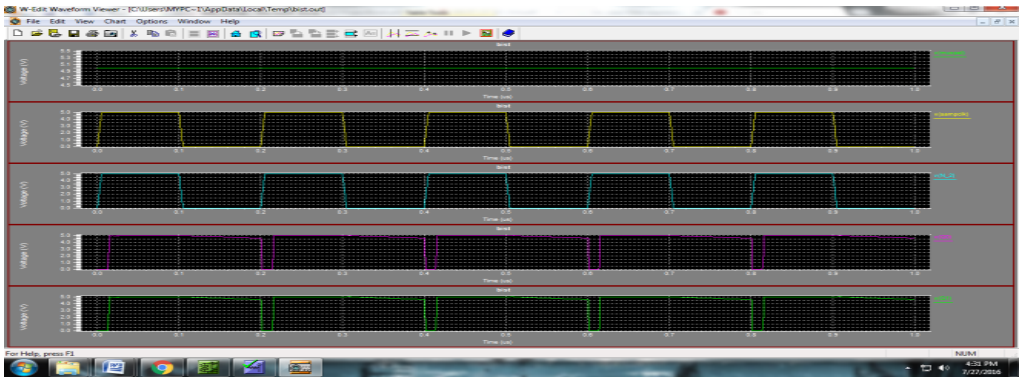

Fig5: Waveform For Analog BIST

V. POWER ANALYSIS

Techniques	Power consumption	Delay
Without Body Biasing	2.173690e-002 watts	5.4413e-008
With Body biasing	1.845307e-005 watts	5.3939e-008

VI. CONCLUSION

Implementation of a BIST scheme to observe the common mode voltage of analog circuitry in a test chip of a power-scalable receiver fabricated in TSMC018 nm is described in this chapter. The design of the voltage-to-delay cells and control circuitry are described along with simulation results from Tanner EDA environment. The voltage-to-delay cell described here is better than the one used earlier, as is clear from the simulation results.

REFERENCES

[1] Anju S. Pillai, Isha T. B, Factors causing power consumption in an Embedded processor", International Journal of Application and Innovation in Engineering and Management (IJ1IEM), 2(7), July 2013.

[2] KanikaKaur and Arti Noor (2011, May). Strategies and Methodologies for low power VLSI designs: A review. International Journal of Advances in Engineering & Technology. [Online]. ISSN: 2231-1963. pp. 159-164. Available: http://www.ijaet.org/media/18 Strategies-Methodologies-For-Low-Power-VlsiDesigns-A-Review-Copyright-IJAET.pdf.

[3] AnkitMitra, Design and implementation of low power 16 bit ALU with c lock gating, International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), 2(6), June 2013. [4] J. Shinde and S. S. Salankar, Clock gating-A power optimizing technique for VLSI circuits, in Proc. Annual IEEE India Conference (INDICON), pp. 1–4, 2011.

[4] R. Ho, B. Amrutur, K. Mai, B. Wilburn, T. Mori, and M. Horowitz, "Applications of on-chip samplers for test and measurement of integratedcircuits," in Symp. VLSI Circuits Dig. Tech. Papers, 1998, pp. 138–139.

[5] C.-L. Wey and S. Krishnan, "Built-in self-test (BIST) structure for analog circuit fault diagnosis," IEEE Trans. Instrum. Meas., vol. 39, no. 3, pp. 517–521, Jun. 1990.

[6] L. S. Milor, "A tutorial introduction to research on analog and mixedsignal circuit testing," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 45, no. 10, pp. 1389–1407, Oct. 1998.

[7] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de Obaldia, and P. T. Balsara, "Alldigital TX frequency

synthesizer and discrete-time receiver for bluetooth radio in 130-nm CMOS," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[8] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8 μW 100kS/s SAR ADC with time domain comparator," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2008, pp. 246–610.

[9] S.-K. Lee, S.-J. Park, H.-J. Park, and J.-Y. Sim, "A 21 fJ/conversionstep 100 kS/s 10-bit ADC with a low-noise time-domain comparator for low-power sensor interface," IEEE J. Solid-State Circuits, vol. 46, no. 3, pp. 651–659, Mar. 2011.

[10] G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari, "Delay-line-based analogto- digital converters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 6, pp. 464–470, Jun. 2009.

[11] T. Watanabe, T. Mizuno, and Y. Makino, "An all-digital analog-to-digital converter with 12μV/LSB using moving-average filtering," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 38, no. 1, pp. 120–125, Apr. 2004.

[12] J. Bergs, "Design of a VCO based ADC in a 180 nm CMOS process for use in positron emission tomography," M.S. thesis, Dept. Space Sci., Luleå Univ. Technol., Stockholm, Sweden, 2010.

[13] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time σδ ADC with a 5-bit, 950-MS/s VCO-based quantizer," IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[14] J. Xiao, A. V. Peterchev, J. Zhang, and S. R. Sanders, "A 4-μa quiescentcurrent dual-mode digitally controlled buck converter IC for cellular phone applications," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[15] R. Vasudevamurthy, P. K. Das, and B. Amrutur, "A mostly-digital analog scan-out chain for low bandwidth voltage measurement for analog IP test," in IEEE Int. Symp. Circuits Syst. Dig. Papers, May 2011, pp. 2035–2038.

[16] P. K. Das, B. Amrutur, J. Sridhar, and V. Visvanathan, "On-chip clock network skew measurement using sub-sampling," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2008, pp. 401–404.

[17] H. Pekau, A. Yousif, and J. W. Haslett, "A CMOS integrated linear voltage-to-pulse-delay-time converter for time based analog-to-digital converters," in IEEE Int. Symp. Circuits Syst. Dig. Tech. Papers, May 2006, pp. 2373–2376.

[18] D. Fick, N. Liu, Z. Foo, M. Fojtik, J. S. Seo, D. Sylvester, and D. Blaauw, "In situ delay-slack monitor for high-performance processors using an all-digital self-calibrating 5ps resolution time-to-digital converter," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2010, pp. 188–189.

[19] T. Hashida and M. Nagata, "An on-chip waveform capturer and application to diagnosis of power delivery in SoC integration," IEEE J. Solid- State Circuits, vol. 46, no. 4, pp. 789–796, Apr. 2011.

[20] [20] B. Amrutur, P. K. Das, and R. Vasudevamurthy, "0.84 ps resolution clock skew measurement via subsampling," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 12, pp. 2267–2275, Dec. 2011.

[21] [21] R. J. Baker, CMOS Mixed-Signal Circuit Design. Piscataway, NJ, USA, IEEE Press, 2002.