POWER QUALITY ENHANCEMENT BY WIND POWER BASED SHUNT ACTIVE FILTER

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ABSTRACT

This paper present research work about renewable energy based shunt active filter to harmonics reduction at the receiving end for the purpose of power quality improvement. Energy source requirement for connected shunt active filter is fulfil by wind power using induction generator. The output of wind farm converts into DC by rectification. This wind farm based shunt active filter is equipped with pulse width modulation technique for inverter to achieve voltage level and frequency as desire by main power system. Simulation gives study for normal working under balance loading condition. This load introduces harmonics in main supply of power system and responsible for higher total harmonics distortion value shows injection of harmonics in main supply of power system. Which reduce by wind farm based shunt active filter thus total harmonics distortion value at receiving end will reduce which is clear indication for reduction in harmonics at the receiving end.

Keywords: Induction Generator, Pulse Width Modulation, Shunt active Power filter, Total Harmonics Distortion

I. INTRODUCTION

Under normal working condition of power system must provide good quality of electrical power to the user associated with it. One can also say the same in terms of lower harmonics content and better power level availability for the user. Harmonics mainly causes by different types of nonlinear loads connected to power system. These are mainly constructing by inductor, capacitor or other energy storage elements. These elements have energy storage capability so it store energy at every half cycle according to polarity of voltage or direction of current offer by source. This stored energy gets discharge in next half cycle due to application of voltage of opposite polarity. Apart from this phenomena inductor and capacitor are also shows some electrical inertia, it will not change its energy states as instantly change in the source apply occur (Karthik Kannan, 2008). Above mention two reason will disturb original wave shape of the power supply thus in other word one can say that it is inducement of harmonics in power supply. Harmonics of high magnitude will causes overheating of phase and neutral conductor, increment in skin effect in transmission system as well as in windings of the motor, causes less efficient performance of the connected systems or other mechanical motion devices for industrial or commercial propose. Transformers are also show lower performance parameters in terms of eddy current loss and load loss (Chengke Zhou, 2002). Harmonics of lower magnitude will affect electronics loads. Hence harmonics in supply will affect the overall performance of connected loads located at different other positions in power system to serve end user in different ways. Application of normal filtering or use of reactor will causes reduction in power availability level at user end although these two passive harmonics reduction technique provide well reduction in harmonics. This reduction in power availability level due to harmonics reduction, will

again affect performance of connected load in terms of active power availability mainly when active power serving for development of mechanical power at connected load.

IEEE standard 519 was introduce in 1981 and get update in 1992. The abstract of this standard are strictly recommending these days for industry and commercial purpose power supply. Power quality mainly deals with deviation in voltage, current and frequency those results in failure customer equipment. Good power quality means user is receiving better wave shape of power at all the time i.e. as close as possible to sinusoidal wave with power level availability according to desire with continuity (H. Fujita, 1991). The active power filter are filter of new generation contain power sources, use to improve the wave shape of power supply in order to reduce harmonics contain in supply by proper filtering and capable to inject power in main power supply. Thus over all power at the reviving end will have less harmonics but power level availability at reviving end will maintain nearly constant (S. Charls and G. Bhuvaneswari , 2010). Another side renewable energy sector is one of the most popular sectors for researchers during these days but does not have enough capability to replace classical power generation technique as effectively and serve as base load plant due some limitation in practical applications till now. Under these circumstances the application of renewable energy sources as power sources for active power filter is a wonderful effort and use to improve harmonics contain as well as maintain power level availability at the receiving or user end to offer better power quality to the user.

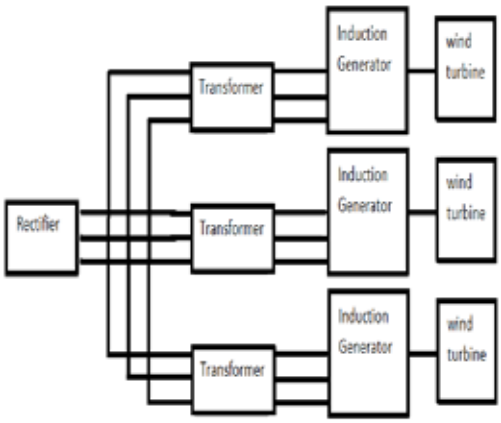

Fig.1: Block Diagram of Induction Generator Based Wind Power Plant with Rectifier

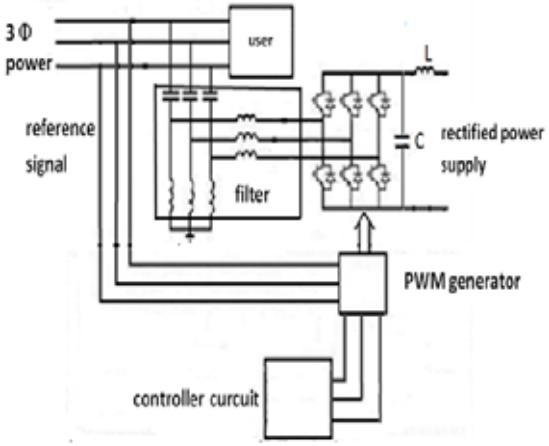

Fig.2: Basic Block Diagram for Shunt Active Filter Connected With Main Supply System

Figure1shows basic block diagram for induction generator based wind power plant use to generate 3 phase electrical power this block is build by parallel connection of three block each have series connection of wind turbine, pitch controller, induction generator. Wind power based induction generator generates AC power this electrical energy converts into DC by simple rectification action. Converted DC has ripples so implementation of inductor and capacitor become essential thus user get ripple free DC supply at input terminal of controlled inverter circuit.

II. MODELLING AND SIMULATION

Wind turbine based shunt active filter was designed and simulated successfully using MATLAB (SIMULINK). SIMULATION is performed with the following parameters in table 1.

Table 1: Simulation Parameters

Sn.	Parameters	Values
1.	Wind Speed	9 m/s
2.	Pitch Angle (Maximum)	43^0
3.	Pitch Angle controller gain (K_p, K_i)	6, 28
4.	Capacitor Ratting for induction generator	400 Kvar
5.	Frequency	60 Hz
6.	Power generation by single wind turbine based induction generator	1.5 MW
7.	Smoothing Reactor after rectification	10 mH
8.	Smoothing Capacitor after rectification	200 mF
9.	Inductor in LC filter for 1^{st} and 2^{nd} stage	2 mH
10.	Capacitor in LC Filter for 1^{st} and 2^{nd} stage	50 mF
11.	Connected Induction motor as load	150 MVA
12.	Mechanical Power Develop by Induction motor	85 MW

Fig. 3 shows simulation of connected wind turbines by which total active power generation by each wind turbine is 3 MW which actually combination of 2 MW and 1 MW wind turbine in parallel use to improve the power quality at the load end. These wind turbines are connecting in parallel with each other. Thus total active power generate by this combination of wind power will be 9 MW. Output of wind turbine connects with input terminal of shunt active filter. Connected load at receiving end have total value of 85 MW as shown in figure 2. Main power grid is connecting in parallel with shunt active filter at load at receiving end. An induction motor of ratting 150 MVA is also connects with main grid supply to obtain non linearity and induce harmonics in the power supply. This power is again transmit through the transmission line. Received power at load end is much affected by the harmonics which eliminate by shunt active filter thus power quality will also improve.

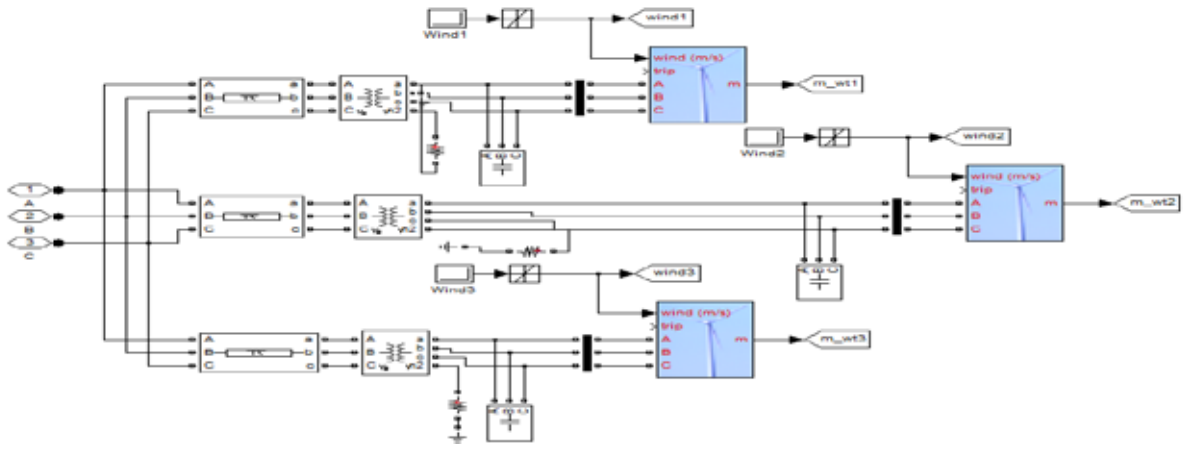

Fig.3: Simulation of Wind Turbines to Generate 9 MW Power

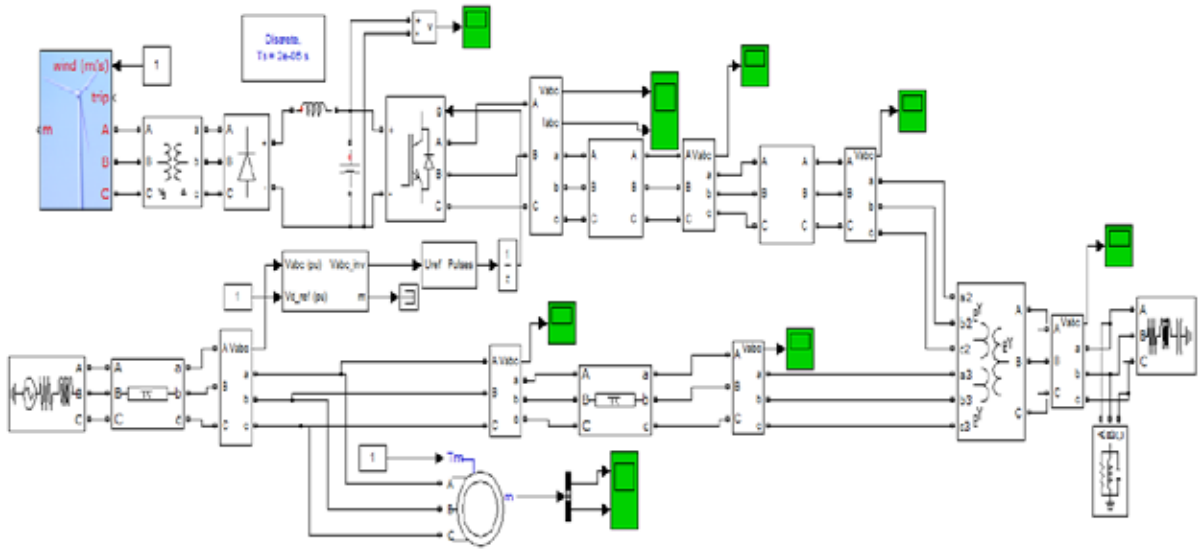

Fig.4: Simulation of Shunt Active Filter with Power System for Harmonics s

III. RESULT AND DISCUSSION

FFT analysis will provides information about the harmonics content at two different positions of the connected simulation for system, connected voltmeter also at similar positions will give magnitude of voltage at these particular positions in per unit. The study of content of harmonics has been carried out for 2 cycles with fundamental frequency of 60 Hz. The harmonics content in the waveform is shown in terms of THD. Higher THD percentage gives information about higher distortion in wave shape in comparison with original wave shape which is pure sinusoidal in this study.

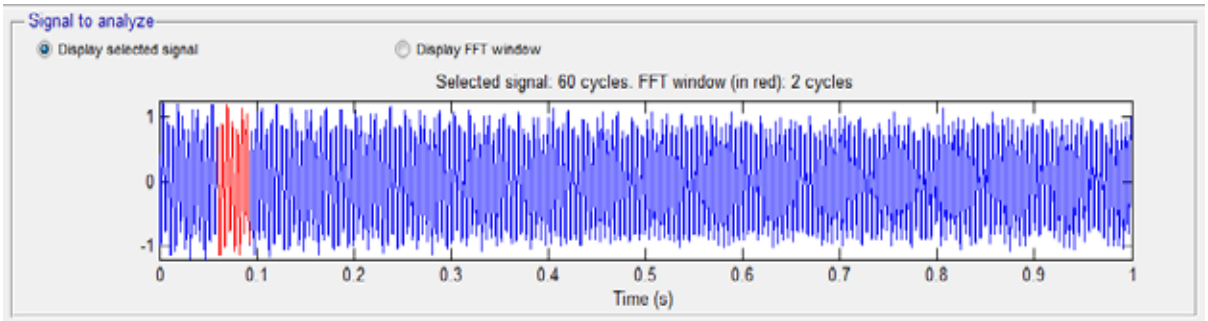

Fig.5: Selected Signal for FFT Analysis after Nonlinear Load in Main Supply

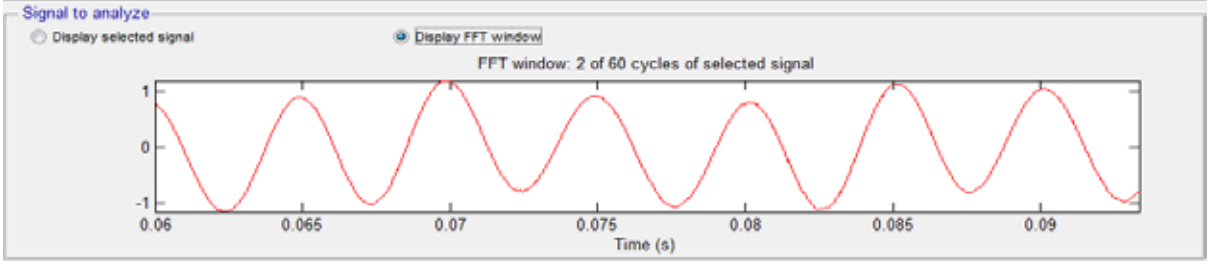

Fig.6: FFT Window for 2 Cycles of Selected Signals for Analysis by Scope Data 1

figure 5 and figure 6 shows the signal for FFT analysis of scope Data 01 which is connected at main supply system at position after nonlinear load. figure 5 shows overall cycles available for time period of 1 sec. Figure 6 shows only 2 cycles for which FFT analysis has been carry out.

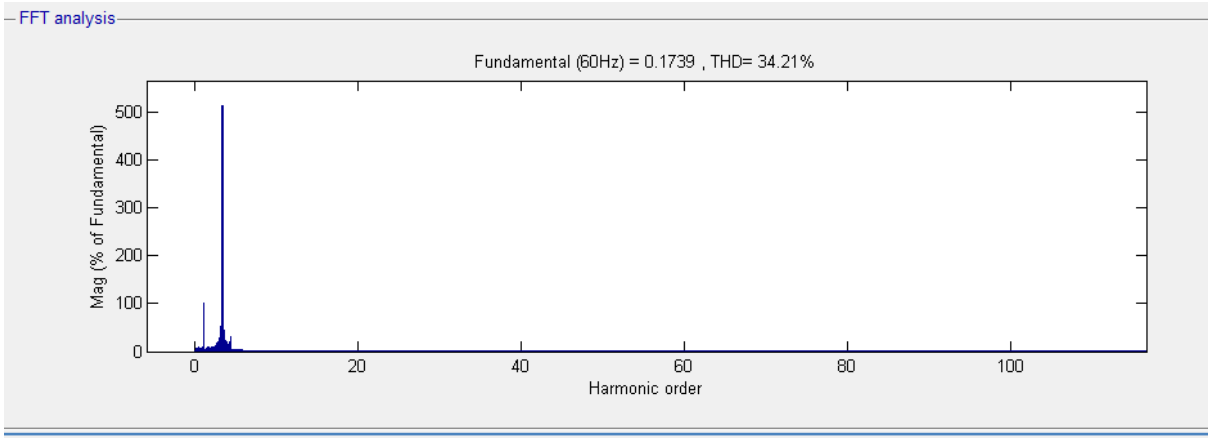

Fig.7: THD Analysis for Selected Signal for Scope Data 1

Figure 7 shows FFT analysis for above mention scope data 01. The total harmonic distortion value is 34.21%. These values of THD show that supply signal has harmonics content of 34.21% with voltage level of 0.956 p.u. at the connecting point. Figure 8 and figure 9 shows the signal for FFT analysis of scope Data 02 which is connected at main supply system at position after connection of shunt active filter. Figure 8 shows overall cycles use for time period of 1 sec. Figure 9 shows only 2 cycles for which FFT analysis has been carry out.

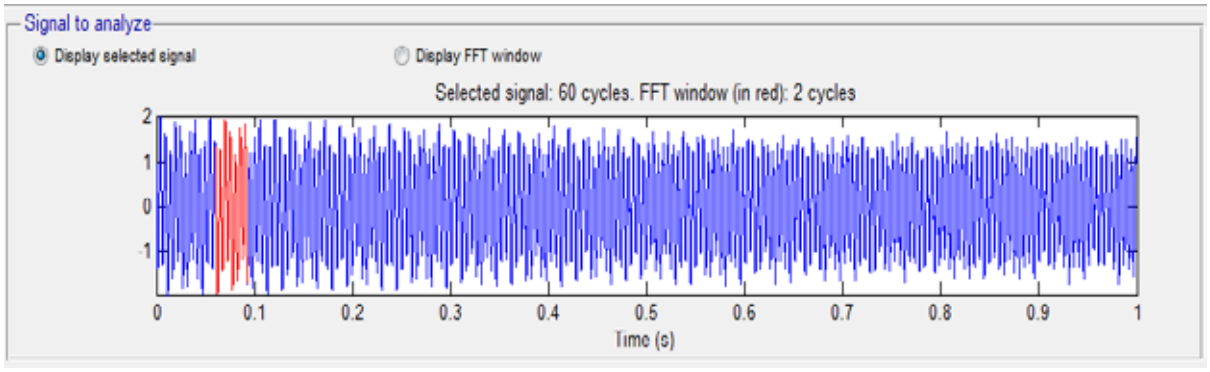

Fig.8: Selected Signal for FFT Analysis after Shunt Active Filter in Main Supply

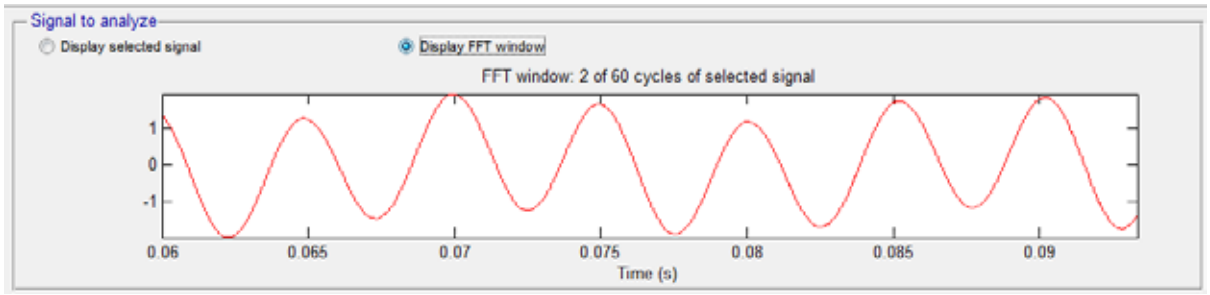

Fig.9: FFT Window for 2 Cycles of Selected Signals for Analysis by Scope Data 2

Figure 10 shows FFT analysis for above mention scope data 02. The total harmonic distortion value is 25.05%. This value of THD shows that supply signal has harmonics content of 25.05% with voltage level of 0.972 p.u. at the connecting point.

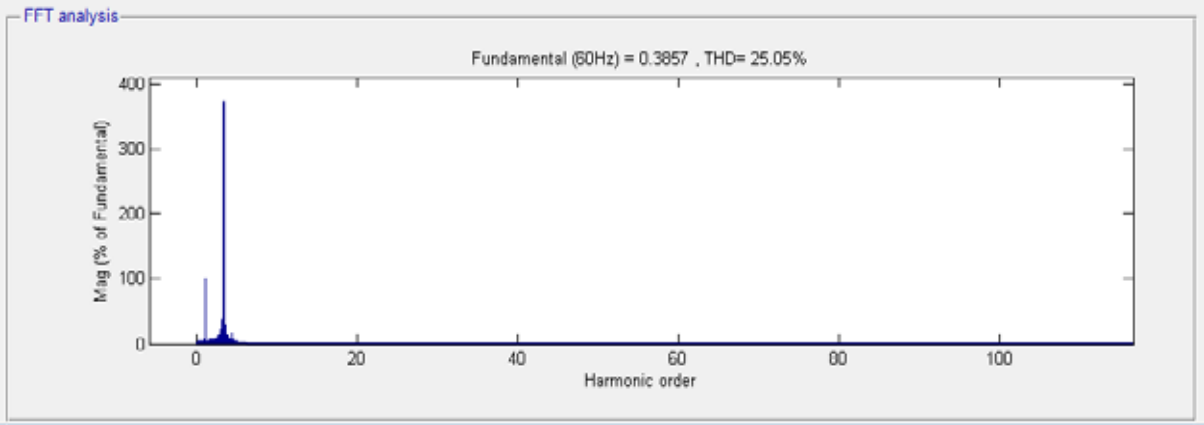

Fig.10: THD Analysis for Selected Signal for Scope Data 2

Thus the above mention result shows that implementation of shunt active filter will gives improvement in THD value about 9.16 in percentage; along with reduction in harmonics the voltage level at the user terminal will also be improved by value of 0.016 p.u., show lower voltage regulation by connection of shunt active filter.

IV. CONCLUSION

The above mentioned results show that implementation of shunt active filter is able to improve harmonics content at user, THD values of 34.21% and 25.05% at nonlinear load end and at connecting point of filter shows improvement in harmonics content at the user terminal. Apart from this voltage regulation is also get improve by shunt active filter which have values of 0.956 p.u. and 0.972 p.u. at above mentioned two positions respectively. Use of wind turbine for power generation in shunt active filter, increases the contribution of renewable energy sector in the main stream of power utilization with improved power quality in terms of wave shape and power availability level.

NOMENCLATURE

P	Active Power (MW)
L	Inductor (H)
C	Capacitor (F)
THD	Total Harmonics Distortion (%)

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COST-EFFECTIVE ROUTE DISCOVERY (CERD) FOR MOBILE AD HOC NETWORKS

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ABSTRACT

A mobile ad hoc network is an infrastructure less network, where nodes are free to move independently in any direction. The nodes have limited battery power; hence we require energy efficient route discovery technique to enhance their lifetime and network performance. In this paper, an energy-efficient route discovery technique CERD has been proposed that greatly reduces the number of route-requests flooded into the network and also gives priority to the route-request packets sent from the routers that has communicated with the destination very recently, in single or multi-hop paths. This not only enhances the lifetime of nodes but also decreases the delay in tracking the destination.

Keywords: Ad Hoc Network, Energy Efficiency, Flooding, Node Lifetime, Route Discovery.

I. INTRODUCTION

An ad hoc network is a group of wireless mobile devices or nodes that communicate with each other in a collaborative way over multi-hop wireless links without any stationary infrastructure or centralized management. These networks are deployed mainly in battlefields and disaster situations such as earthquake, floods etc. Many routing protocols have been proposed for ad hoc networks. They can be mainly categorized as proactive and reactive routing protocols. Among proactive routing protocols, destination-sequenced distance vector (DSDV) [1], wireless routing protocol (WRP) [2], global state routing (GSR) [3] and cluster-based gateway switch routing (CGSR) [4] are well known. In all proactive routing protocols the nodes proactively store route information to every other node in the network. In general, the proactive routing protocols suffer from extremely huge storage overhead because they store information both about active and non-active routes. This inculcates the unnecessary complexity of discovering routes to the destinations with which a node rarely communicates. Reactive or on-demand routing protocols are designed to reduce this overhead. In reactive routing protocols, when a source node needs to communicate with a destination, it floods route-request packets through out the network to discover a suitable route to the destination. Dynamic source routing (DSR) [5], ad hoc on-demand distance vector routing (AODV) [7], adaptive communication aware routing (ACR) [8], flow-oriented routing protocol (FORP) [9] and associativity-based routing (ABR) [10] are well-known among the reactive routing protocols. AODV builds routes using a route-request, route-reply query cycle. When a source node desires to send packets to a destination for which it does not already have a

route, it broadcasts a route-request (RREQ) packet across the network. Nodes receiving this packet update their information for the source node and set up pointers backward to the source node in their routing tables. A node receiving the route-request (RREQ) packet sends a route-reply (RREP) if it is either the destination or has a recently established route to the destination with. Dynamic source routing (DSR) is similar to AODV in that it forms a route on-demand when a source node requests one. It uses source routing instead of relaying on the routing table at each device. Determining source routes require accumulating the address of each router in the route-request message. In FAIR [11], the source node transmits RREQ packets that arrive at the destination through multiple paths. Depending upon the locations, residual energy, velocity etc. various characteristics of the routers, the destination node evaluates performance of the paths by considering their stability and agility. Then communication from source to destination begins through one of the best paths. FORP and ABR are link stability based routing protocols that also rely on the flooding of RREQ packets for route discovery. So, if the number of RREQ packets can be reduced then much lesser number of routers will be involved in the route discovery process in the CERD versions of the above-mentioned routing protocols compared to their ordinary versions. As a result, network throughput or data packet delivery ratio enhances with decrease in energy consumption in nodes.

In order to resolve the issue of reduction of RREQ flooding into the network, as much as possible, our present article proposes a cost-efficient route discovery (CERD) technique for communication in ad hoc networks where the RREQ packets are forwarded only to those downlink neighbours for which it is possible to send the RREQ packet to the destination, depending upon the most recent location of the destination as known to the underlying router or source of the communication. The latest is the known location of the destination the smaller is the number of flooded route-requests. Our proposed technique can be applied with any reactive routing protocol to enhance the performance of the protocol.

II.OVERVIEW

Each node maintains a cache of nodes with which it has communicated recently. The information stored in cache about each such recently communication destinations, are identification number of the destination, its maximum velocity, geographical location in terms of latitude and longitude at the time of communication and timestamp of the communication. These are supplied by the destination node embedded within its route-reply message. Ordinary flooding of RREQ packets floods them to all downlink neighbours of a node. On the contrary, CERD imposes a constraint that a node (source/ router) will forward a RREQ packet only to those downlink neighbours for which it is possible to successfully send the route-request to the destination node within the lifetime of those RREQ packets, given a pre-specified location of the destination. Hence, CERD greatly reduces the number of flooded RREQ packets preserving the battery power of network nodes. The improvement is very much noticeable because in ad hoc networks generally the nodes communicate with a fixed set of nodes. For example, a school boy generally communicates with a fixed set of teachers, class-friend and family members; a business person generally communicates with a fixed set of clients and colleagues etc. So, very often a recent location of the destination node is known to the source or routers. The benefit is highest if a recent location of the destination is known to the source.

It is minimum in the situation where a recent location of the destination is known only to an uplink neighbour of the destination and to none of its predecessors.

III.COST-EFFICIENT ROUTE DISCOVERY (CERD) TECHNIQUE

The technique of CERD is illustrated in this section based on the following assumptions:-

i) n_s is the source and n_d is the destination node

ii) n_s initiates route discovery at time ts which arrives at a router n_i at time t

iii) The maximum lifetime of a RREQ packet is t.

iv) A router n_i knows the location of the destination at time t1 where t1 < t

v) Location of any node n_i in the network at time t¢is denoted by an ordered pair (x_i(t¢), y_i(t¢))

vi) Maximum velocity of any node n_i is given by v_{max}(i)

vii) Approximate velocity of the wireless signal is given by v_s

A downlink neighbour n_j of n_i receives the RREQ forwarded by n_i destined to n_d, only if it is possible for n_j to send that RREQ to n_d within the entire lifetime of the RREQ packet.

Definition: **Destination Embedding Circle (DEC)**

The circle that embeds all possible positions of the destination n_d during the entire lifetime of the RREQ generated by n_s at time ts, is termed as the destination embedding circle (DEC) as observed by n_i. Its center is (x_d(t1), y_d(t1)) and radius is {v_{max}(d) ´ ((t-t1)+t-(t-ts))} i.e. { v_{max}(d) ´ (t-(t1-ts))}.

n_i will send RREQ packet to n_j if any wireless signal transmitted by n_j at time t can reach the nearest point on the DEC as observed by n_i at time t1, within the time interval (t-(t1-ts)). The distance that can be traveled by the wireless signal within the time interval (t-(t1-ts)) is given by (v_s ´ (t-(t1-ts))). This distance should not be lesser than the distance of n_j from the nearest point on the DEC as observed by n_i at time t1, for receiving the RREQ from n_i. In figure 1, let (h, k) be that particular point on the DEC of n_i, which is closest to n_j. The points (x_j(t), y_j(t)) , (x_d(t), y_d(t)) and (h,k) are collinear. From this condition of collinearity, I obtain the equation (1) and equation (4) is obtained based on the situation that (h,k) is a point on the DEC of n_i. So, its distance from the center of the DEC is equal to radius of the DEC. The situation can be depicted from figure 1.

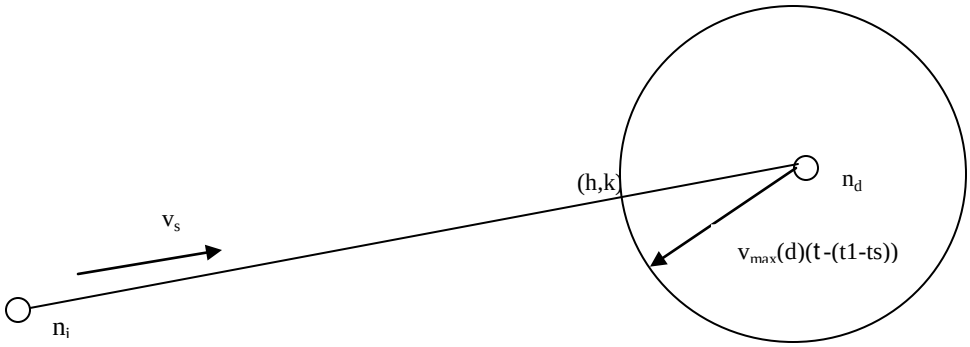

Figure 1: Demonstration of DEC

$$(h - x_j(t)) / (x_j(t) - x_d(t)) = (k - y_j(t)) / (y_j(t) - y_d(t)) \quad (1)$$

Therefore, $h = x_j(t) + (k - y_j(t))\,(x_j(t) - x_d(t)) / (y_j(t) - y_d(t))$ (2)

so, $h = c1\ k + c2$ (3)

where $c1 = (x_j(t) - x_d(t)) / (y_j(t) - y_d(t))$ and $c2 = x_j(t) - c1\ y_j(t))$

$$(h - x_d(t))^2 + (k - y_d(t))^2 = v^2_{max}(d)\,(t-(t1-ts))^2 \quad (4)$$

For simplicity, lets replace $v^2_{max}(d)\,(t-(t1-ts))^2$ by a constant c3. Putting $h = c1\ k + c2$ in (5) I get,

$$(c1\ k + c2 - x_d(t))^2 + (k - y_d(t))^2 = c3 \quad (5)$$

This is a quadratic equation. Solving this equation, following two values (lets denote them as k_1 and k_2)

of k are obtained.

$$k\_1 = [y_d(t)-c1(c2-x_d(t)) + \sqrt{\{c1(c2-x_d(t)) - y_d(t)\}^2-(1+c1^2)\{(c2-x_d(t))^2+y^2_d(t)\}}] / (1+c1^2) \quad (6)$$

$$k\_2 = [y_d(t)-c1(c2-x_d(t)) - \sqrt{\{c1(c2-x_d(t)) - y_d(t)\}^2-(1+c1^2)\{(c2-x_d(t))^2+y^2_d(t)\}}] / (1+c1^2) \quad (7)$$

Corresponding values of h are denoted as h_1 and h_2 where

$h\_1 = c1\ k\_1 + c2$ and $h\_2 = c1\ k\_2 + c2$

Let dist1 and dist2 indicate the distance of the points (h_1, k_1) and (h_2, k_2), respectively, from the center of the DEC in figure 1. Then,

$dist1 = \sqrt{\{(h\_1 - x_d(t))^2 + (k\_1 - y_d(t))^2\}}$ and $dist2 = \sqrt{\{(h\_2 - x_d(t))^2 + (k\_2 - y_d(t))^2\}}$

Assume that mindist denotes the smaller among dist1 and dist2 (i.e. mindist = dist1 if dist1 < dist2, else mindist = dist2).

If $mindist > (v_s \times (t-(t1-ts)))$ then n_i does not forward the RREQ to n_j.

IV . SIMULATION RESULTS

Simulation of the mobile network has been carried out using ns-2 [12] simulator on 800 MHz Pentium IV processor, 40 GB hard disk capacity and Red Hat Linux version 6.2 operating system. Graphs appear in figures 2 to 7 showing emphatic improvements in favor of cost effective route discovery. Number of nodes has been taken as 20, 50, 100, 300 and 500 in different independent simulation studies. Speed of a node is chosen as 5m/s, 10 m/s, 25 m/s, 35 m/s and 50 m/s in different simulation runs. Transmission range varied between 10m and 50m. Used network area is 500m ´ 500m. Used traffic type is constant bit rate. Mobility models used in various runs are random waypoint, random walk and Gaussian. Performance of the protocols AODV, ABR and FAIR are compared with their CERD embedded versions CERD-AODV, CERD-ABR and CERD-FAIR respectively. In order to maintain uniformity of the implementation platform, I have used ns-2 simulator for all the above-mentioned communication protocols. The simulation matrices are data packet delivery ratio (total no. of data packets delivered´ 100/total no. of data packets transmitted), message overhead (total number of message packets transmitted including data and control packets) and per node delay in seconds in tracking destination (total delay in tracking the destination in different communication sessions / total number of nodes). Simulation time was 1000 sec. for each run.

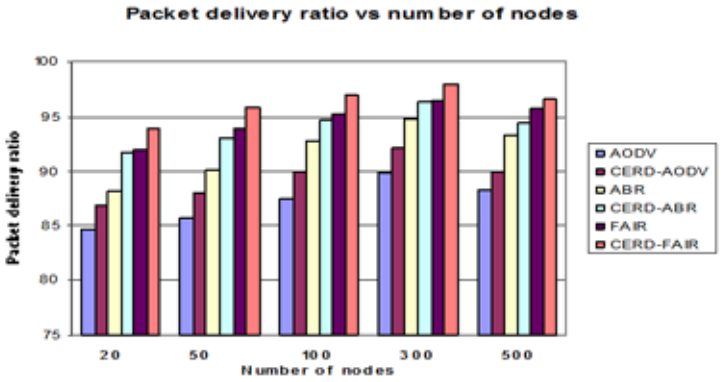

Figure 2: Data packet delivery ratio vs number of nodes

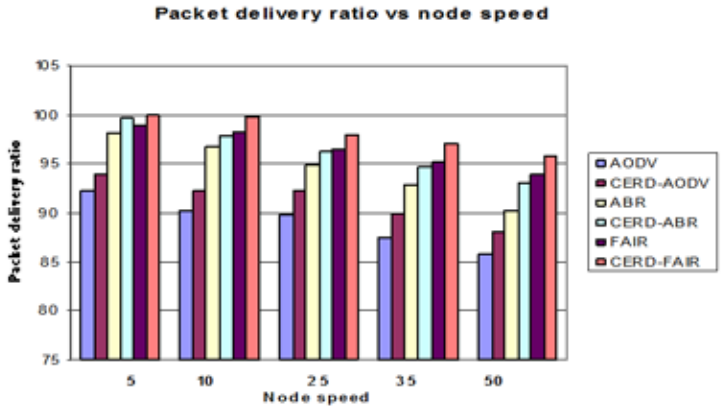

Figure 3: Data packet delivery ratio vs node speed

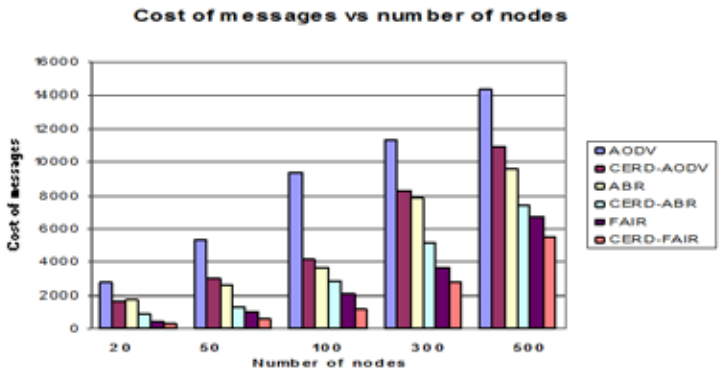

Figure 4: Cost of messages vs number of nodes

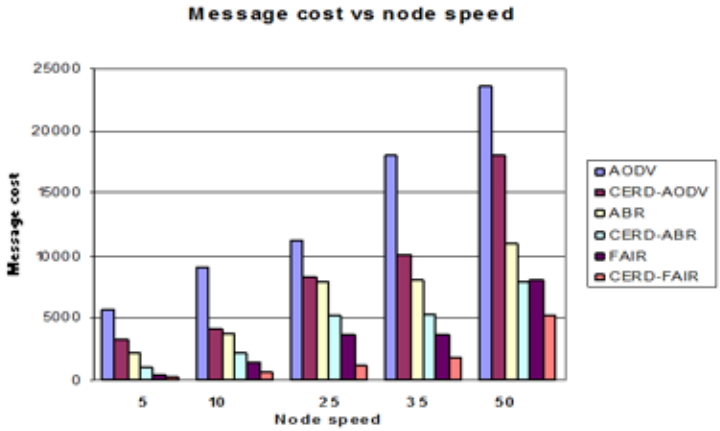

Figure 5: Cost of messages vs node speed

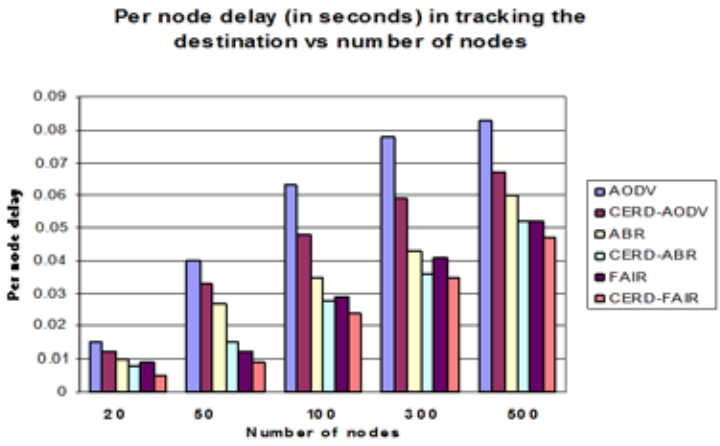

Figure 6: Per node delay vs number of nodes

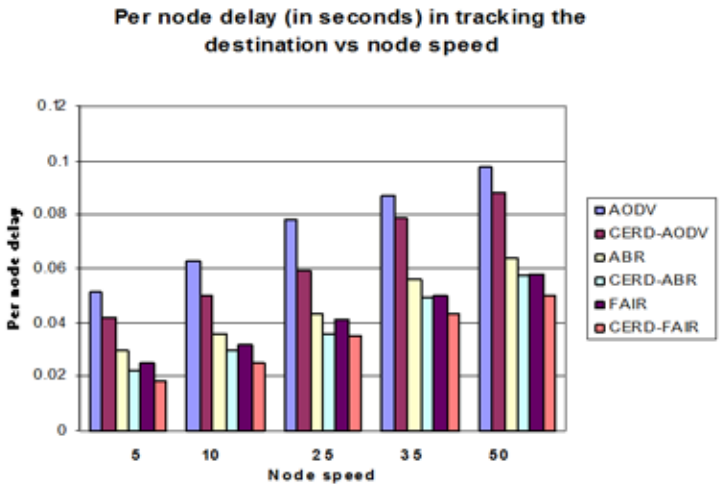

Figure 7: Per node delay vs node speed

Figure 2 shows that the initially the data packet delivery ratio improves for all the protocols with increase in number of nodes and then it starts reducing. The reason is that the network connectivity improves with increase in number of nodes, until the network gets saturated or overloaded with nodes. When the overloading occurs, cost of messages become very huge and the packets hinder one another from reaching their destinations by colliding. Figure 4 shows that for all the protocols cost of messages increase with increase in number of nodes. This is quite self-explanatory. From figure 6 it may be seen that as the number of nodes increase, the delay in tracking the destination also increases. The reason is that more number of communications is initiated with increased number of nodes and due to better network connectivity more destinations can be tracked now which are far apart. Also the phenomenon of more packet collision increases the delay in tracking destinations. Figures 3, 5 and 7 are concerned with the influence of node speed on these metrics. As the node speed increases, many new links form and older ones break increasing the network congestion and message collision. Colliding messages are unable to reach their respective destinations; hence they need to be retransmitted. This causes additional delay in the process and injects some more messages. As a result, packet delivery ratio decreases with increased cost and delay.

CERD reduces the injection of route-request packets to a great extent since an intermediate node that has recently communicated with the destination, broadcasts the route-request only to those downlink neighbors from which it is possible to drive the RREQ to the actual destination within the lifetime of RREQ packet generated by the source of the communication session. This increases the node lifetime and reduces the packet collision. As a rate, data packet delivery ratio of CERD embedded versions of the above-mentioned protocols also increase compared to the ordinary versions of those. The improvements are evident from figures 2, 3, 4 and 5. As far as delay in tracking the destination is concerned, CERD embedded versions show significant improvement. The reason is that RREQ packets in CERD embedded versions face much less hindrances due to lesser amount of packet collisions compared to the ordinary versions of those protocols. Therefore, those RREQ packets are driven to their respective destinations much sooner in protocols with CERD facility.

Please note that the improvement produced by CERD-AODV over ordinary AODV is more than those produced by

CERD-ABR over ordinary ABR and CERD-FAIR over ordinary FAIR. The reason is that in AODV, among all discovered routes from source to destination, the one with minimum hop count is elected for communication, without considering stability of the links (stability is expressed mainly in terms of relative velocities between the two nodes forming a link). On the other hand, in ABR, the route with maximum number of stable links is elected as optimal. FAIR is even more conscious on link stability as well as agility. Hence, the phenomenon of link breakage is more frequent in AODV than ABR as well as FAIR. In order to repair the broken link, more RREQ messages are injected into the neighborhood of the broken link in case of ABR and FAIR whereas in AODV a new route discovery session is initiated altogether which requires generation of a huge number of RREQ packets once again. Actually, link breakage in all protocols increases message overhead decreasing the network throughput with different intensity determined by the logic of the protocol itself. Note that, the phenomenon like route discovery and link repair are less devastating in ABR and FAIR than in AODV. So, performance enhancement of CERD-AODV over AODV is more than that produced by CERD-ABR over ABR and CERD-FAIR over FAIR.

V.CONCLUSION

The concept of energy-efficient route discovery presented in this paper greatly reduce message overhead of the network. As a result, data packet delivery ratio increases along with the lifetime of network nodes. Maximum benefit can be obtained if the source node knows about a recent location of the destination which is very much possible from the point of view of ad hoc networks.

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FESA: FUZZY CONTROLLED ENERGY EFFICIENT SELECTIVE ALLOCATION AND REALLOCATION OF TASKS AMONG MOBILE ROBOTS

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ABSTRACT

Energy aware operation is one of the visionary goals in the area of robotics because operability of robots is greatly dependent upon their residual energy. Practically, the tasks allocated to robots carry different priority and often an upper limit of timestamp is imposed within which the task needs to be completed. If a robot is unable to complete one particular task given to it the task is reallocated to some other robot. The collection of robots is controlled by a Central Monitoring Unit (CMU). Selection of the new robot is performed by a fuzzy controller called Task Reallocator (TRAC). It accepts the parameters like residual energy of robots, possibility that the task will be successfully completed by the new robot within stipulated time, distance of the new robot (where the task is reallocated) from distance of the old one (where the task was going on) etc. The proposed methodology increases the probability of completing globally assigned tasks and saves huge amount of energy as far as the collection of robots is concerned.

Keywords: Energy efficiency, Fuzzy Controller, Priority, Selection, Task.

I. INTRODUCTION

The present article focuses on the efficient distribution of tasks among a collection of mobile robots, which are centrally controlled by a Central Monitoring Unit (CMU). All robots can directly send signals to CMU and receive signals from it. The situation can be detected from figure 1 where R, R1, R2 and R3 are the robots. CMU keeps track of the residual energy of robots, tasks that are allocated to them and the present status of execution of those tasks along with the constraints associated with them. A decision process is initiated in order to accept/ reject tasks for further processing as well as to continue/ re-allocate a task in progress. On a global point of view, a task allocation procedure is initiated after arrival of a new job or cancellation of an ongoing task subjected to the availability of able robots.

Studies on energy-aware operation and task allocation among mobile robots are in progress in a number of research groups. F. Dressler and G. Fuchs [1] proposed an energy-aware task allocation among mobile robots where only the residual energy of robots are considered. Issues of coordination among mobile robots are presented in [2] and [3] whereas cooperation issues are discussed in [4]. One of the most commonly used task allocation strategies in robotics are threshold based systems. These systems are based on observations of task or role allocation processes in social insects, whereby tasks, often implicitly, send out a signal, and the insects/robots react to this signal if it surpasses an internal threshold. Due to differences in this threshold among individuals, task allocation emerges in proportion to the task's signal intensity [7]. In [6], a variation of this mechanism is presented whereby all robots have the same threshold and the differentiation comes from the

variability in the local observation of the signal intensity by the individuals. In [8] an ant-like task allocation model was proposed that is based on local threshold value for energy efficiency.

The rest of the paper is organized as follows. Section 2 illustrates the basic system model. Heuristics that drive TRAC are discussed in section 3. Design of TRAC is performed in section 4. Section 5 emphasizes the effectiveness of our proposed scheme through extensive simulation results. Section 6 analyzes the complexity of our proposed scheme FESA and section 7 concludes the paper.

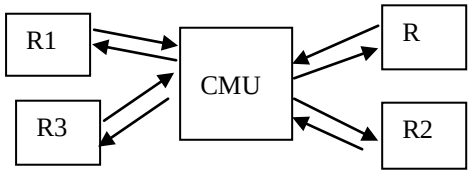

Fig.1 Signal transmission and reception between CMU and robots R, R1, R2 and R3

1.1 System Model of FESA

The system of FESA consists of a collection of robots and a CMU that allocates and reallocates the tasks to robots as the tasks arrive into the system. The system is non-preemptive. Once a task is allocated to a robot, say R1, it is allowed to continue its task till the upper limit of time duration associated with the task elapses or some unnatural incident makes R1 unable to operate any further. For example, fire may break out into the system and destroy R1. It may be noted that, at any point of time a task may be allocated to exactly one robot. When a new task arrives into the system it is initially allocated to any idle robot possessing sufficient amount of energy to complete the task. If no such robot is found, then the task is allocated to one of the robots having maximum residual energy. The intention is to complete a task as much as possible. On the other hand, during reallocation, CMU consults the TRAC embedded in it to find the best possible robot to carry out the pending task. A task is reallocated if sufficient time is there to complete the task i.e. upper limit of timestamp within which the task needs to be completed, is not crossed, at least one operational idle robot is there and no task with higher priority is waiting at that time for being allocated or reallocated to robots. CMU maintains three different tables termed as ROBOT_TABLE, TASK_TABLE and HISTORY_TABLE. CMU also stores the maximum possible distance between any two robots through a path traversable in the present geographical scenario. Attributes of the mentioned tables are shown below:

ROBOT_TABLE
Robot_id
Enrg_tot
Enrg_thres

HISTORY_TABLE
Robot_id
Task_id
Task_portion
Session_id
Assign_timestamp
Release_timestamp

TASK_TABLE
Task_id
Priority
Completion_timestamp
Ptr_robotarray
Enrg_task

Enrg_rem_task
Status

A tuple (p,q,r) in the ROBOT_TABLE indicates that p is identification number of one robot, q is its total energy and r is its energy threshold. According to the characteristic curve of the batteries used in mobile robots, voltage drop shows a linear decline until some critical value [1, 2]. After that point the voltage drop speeds up quickly with very small remaining time left for execution [1]. Energy of the robot corresponding to the critical voltage is termed as energy threshold of the robot.

A tuple (p, ts, tp, sid, atm, rtm) in the HISTORY_TABLE signifies that the robot p completed tp portion of the task ts within time interval (rtm-atm) in session sid. atm is the timestamp at which the task was assigned and rtm is the time at which the task finished. Similarly, a tuple (ts, pr, ct, rbr, et, etrem, st) in TASK_TABLE denotes that the task with identification number ts has priority pr and it needs to be completed within timestamp ct. rbr is pointer to a list. Each entry of the list contains identification numbers of the robots to which the task was assigned earlier, portion of the task that was assigned along with the corresponding timestamp, the timestamp when the robot unsuccessfully stopped execution of that portion of the task and portion of the task remaining to be executed. et is the minimum energy required to accomplish the whole task whereas etrem is the minimum energy required to accomplish the remaining portion of the task. All possible values of st are 0 and 1. It is set to 0 if the task is being executed and set to 1 if it cannot be completed (possible reasons are unavailability of robots, completion time constraints etc.).

During reallocation, portion of a task may be reallocated. For example, let 50% of a task has been carried out by a robot R1 after which it suddenly stopped operating. Then the rest 50% of the same work can be allocated to some other robot R2 although it is not possible in our proposed scheme to allocate 30% of the remaining task to R2 and the rest to R3, simultaneously. At any point of time, one particular task cannot run in more than one robot, even partly.

1.2 Heuristics of TRAC

The fuzzy controller TRAC, which is responsible for task reallocation, performs according to the following heuristics:

i) If a robot R is equipped with high residual battery power so that the residual energy above its energy threshold is greater than the energy required to accomplish the remaining portion of task A, then R is in an advantageous position to execute that portion of the task.

ii) According to the HISTORY_TABLE of CMU, if a robot R has successfully accomplished the task A earlier within the mentioned stipulated time duration, then R has a good chance of being assigned the same task A in future.

iii) If the minimum geographical distance through a traversable region within the given scenario, of the old robot R1 (where a task A was going on earlier) from the new robot R (where A is going to be reallocated) is small, then it will be beneficial for the new robot R to resume the task, specially when the task is of the type exploration and supervision of unknown surroundings.

iv) If a robot R has got a bad failure history i.e. failed to complete a number of tasks on so many occasions, then it is better to avoid R during reallocation of tasks.

The observations expressed above are in the form of if-then rules which are the basic unit of fuzzy function

approximation. Advantages of fuzzy logic are that it is flexible, conceptually easy to understand and based on natural language. Moreover, it is tolerant of imprecise data and can model non-linear functions of arbitrary complexity. All these encouraged us to design the scheme of FESA using fuzzy logic.

II. DESIGN OF TRAC

2.1 Formulation of parameters

The input parameters of TRAC are energy_efficiency, history_of_support, distance_quotient and failure_quotient. These are formulated below based on the assumption that the current timestamp is t and TRAC is considering to reallocate a portion r (A,t) of task A in robot R. R1 is the old robot where the task A was being carried out.

Energy_efficiency

The energy_efficiency $a_R(t)$ of a robot R at time t is given by,

$$a_R(t)=1-e_A/(E_R(t)-Ethres_R) \quad (1)$$

e_A specifies the minimum energy required to complete portion of the task A to be reallocated. $E_R(t)$ is the residual energy of robot R at time t and $Ethres_R$ signifies the threshold energy of the same robot. It is quite evident from (1) that $a_R(t)$ lies between -¥ and 1. Positive fractional values of $a_R(t)$ puts R in a good position to carry out the task r (A,t).

History_of_support

Let H(R,A) denote the set of occasions or sessions during which the robot R successfully completed execution of the portion of task A that was given to it abiding by the time constraint associated with the task. Also assume that HF(R,A) denote the set of occasions or sessions during which the robot R could not successfully complete execution of the portion of task A that was given to it. Then, history_of_support $h_{R,A}(t)$ of robot R at time t with respect to task A is given by,

$$h_{R,A}(t) = \begin{cases} (h¢_{R,A}(t) / T\_C(A)) & \text{if } (h¢_{R,A}(t) / T\_C(A)) \geq 1 \\ (h¢_{R,A}(t) / T\_C(A))^{\exp Z(R,A)} & \text{otherwise} \end{cases} \quad (2)$$

$$h¢_{R,A}(t) = [\{t+\{\tilde{O}_{w \hat{I} H(R,A)} (b_{R,w}/q_w(A))\}^{1/|H(R,A)|}\}´ r(A,t)] \quad (3)$$

$$Z(R,A) = H(R,A) / \{H(R,A)+HF(R,A)\}$$

According to the history of behavior of robot R, in session w, $q_w(A)$ portion of the task A has been completed by robot R in time duration $b_{R,w}$. T_C(A) is the timestamp within which the task A must be fully completed. If $h_{R,A}(t)$ is less than 1 then R has a good chance to be assigned the task r (A,t). $h_{R,A}(t)$ should acquire a low value if number of successes of robot R with respect to task A is high and number of failures of R with respect to task A is low, i.e. if H(R,A) is high and HF(R,A). This is correctly modeled through Z(R,A).

Distance_quotient

Let $dist_{R,R1}(t)$ be the least geographical distance between the robots R1 and R at time t through a path which is traversable in the present scenario. Also assume that dist_max is the maximum possible distance between any two robots through a path traversable in the present scenario. Then, the distance_quotient $dq_{R,R1}(t)$ of robot R w.r.t. robot R1 at time t is given by,

$$dq_{R,R1}(t) = dist_{R,R1}(t) / dist\_max \quad (4)$$

Distance_quotient lies between 0 and 1. Values close to 0 indicate that R won't have to make huge extra efforts to resume the pending task A of R1.

Failure_quotient

Let $b_R(t)$ be the number of tasks allocated to robot R within time t, irrespective of whether they were allocated fully or partly. Among them, on $b¢_R(t)$ number of occasions the tasks had to be reallocated from R. Hence, the failure quotient $fq_R(t)$ of robot R at time t based on the history of it's behavior, is,

$$fq_R(t) = b¢_R(t) / b_R(t) \quad (5)$$

Actually failure quotient of a robot indicates its general attitude towards the tasks assigned to it by the CMU. If it is high then it denotes that R is only eager to relinquish its tasks. Please note that fq also ranges between 0 and 1.

2.2 Rule Bases of TRAC

As far as the range division of a is concerned, the range from -¥ to 0 is not advantageous for the system and it is denoted as a1. The ranges from 0-0.33, 0.33-0.66, 0.66-1 are indicated as a2, a3 and a4 respectively. For range division of h, the ranges from 0-0.33, 0.33-0.66, 0.66-1 are indicated as a1, a2 and a3 respectively. The range from 1-¥ is not acceptable and it is denoted as a4. For the subsequent two parameters dq and fq the range division is uniform between 0 and 1, i.e. 0-0.25 is a1, 0.25-0.50 is a2, 0.50-0.75 is a3 and 0.75-1 as a4. Please note that the subscripts have been omitted here for simplicity.

Table 1 shows the fuzzy composition of energy efficiency and history_of_support generating a temporary output t1. History_of_support plays a significant role in determining whether a pending task will be reallocated to one particular robot only if energy of the robot is sufficiently high to accomplish that task. t1 is combined with failure quotient in table 2 generating another temporary output t2. t1 dominates in table 2 because it is a combination of two parameters which are equally or more important than fq. Similarly, t2 is combined with dq in table 3 generating the ultimate output reloc. Here also t2 dominates for the reasons described earlier in case of table 2.

Table.1. Fuzzy Combination of a and h Generating t1

a® h¯	a1	a2	a3	a4
a1	a1	a2	a3	a4
a2	a1	a2	a3	a4

a3	a1	a2	a2	a3
a4	a1	a1	a1	a2

Table.2. Fuzzy Combination of t1 and fq Generating t2

t1® fq¯	a1	a2	a3	a4
a1	a1	a2	a3	a4
a2	a1	a2	a3	a4
a3	a1	a2	a3	a3
a4	a1	a1	a2	a3

Table.3. Fuzzy Combination of t2 and dq Generating reloc

t2® dq¯	a1	a2	a3	a4
a1	a1	a2	a3	a4
a2	a1	a2	a3	a4
a3	a1	a2	a3	a4
a4	a1	a2	a2	a3

Among the various value ranges of reloc of different robots, any one possessing the highest value range will be selected for reallocation of a certain job.

III. SIMULATION RESULTS

For simulation, I have used the Webots 3D physics-based robotics simulator [9] to create the virtual world which the robots mapped and navigated as part of the experiments. Webots has high fidelity and models realistic sensor and motion errors. In the simulation experiments I used RV-400 [10] robots. In various runs, the number of robots was 3, 6, 9, 11 and 14 while the number of tasks was 5, 9, 12, 15 and 20. The tasks are to explore portions of a room of different sizes. The simulation was carried out for approximately 3000 seconds. The results reported graphically in this section correspond to the average of all the simulation runs.

Performance of the present scheme has been compared with other state-of-the-art techniques that address the similar issue i.e. energy-aware operation and task allocation (EOTA [1]) and ant-like task allocation (ATA [8]) models. Performance matrices are consumed energy per robot, percentage of successfully completed tasks, delay for completion of each task and required percentage of reallocation. The results reveal that our proposed scheme *Fuzzy-controlled Energy-efficient Selective Allocation* (FESA) outperforms its competitors in every respect. The results are graphically shown in figures 2, 3, 4 and 5.

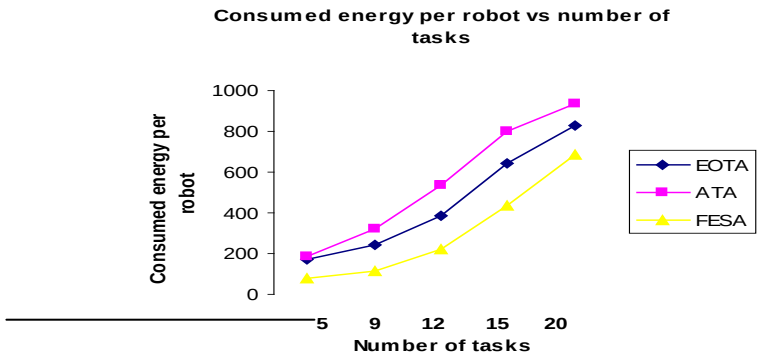

Figure 2: Graphical illustration of consumed energy in Joule per robot vs number of tasks

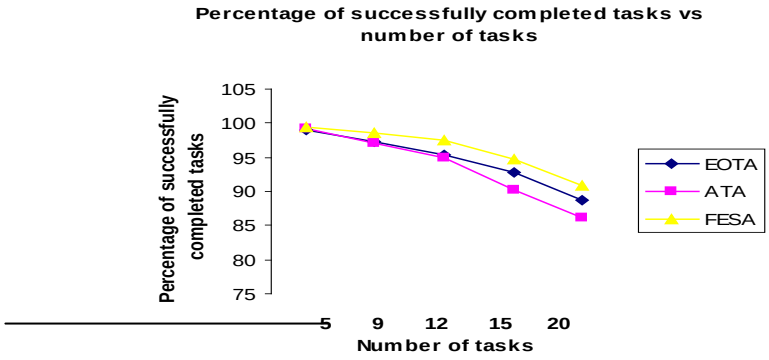

Figure 3: Graphical illustration of percentage of successfully completed tasks vs number of tasks

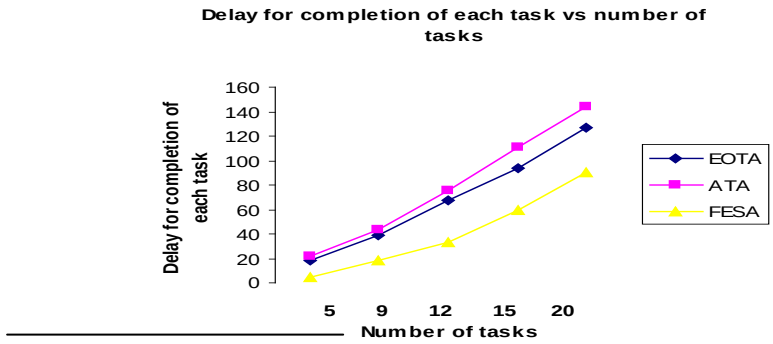

Figure 4: Graphical illustration of delay for completion of each task in seconds vs number of tasks

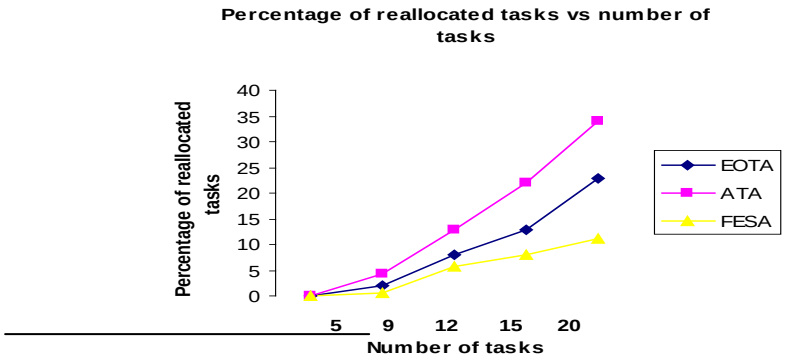

Figure 5: Graphical illustration of percentage of reallocated tasks vs number of tasks

If a robot is bound to execute some task when its residual energy is less than energy threshold, then its rate of energy consumption abruptly increases. Our proposed scheme FESA always tries to allocate or reallocate tasks to those robots that have sufficient battery power to execute the tasks. Moreover, during reallocation, FESA tries to find new robots which are geographically close to the old one so that the new robot chosen by TRAC can efficiently take over the charge of the old one without much effort. This is particularly useful for the tasks like exploring a room. All these contribute to the reduction of energy consumption in favor of our proposed scheme FESA. However, it is quite trivial that the amount of energy consumption for each robot will increase for all the task allocation schemes as the number of tasks increase. This is illustrated in figure 2.

By analyzing the attitude of robots towards a specific task and to all other tasks from the task table in CMU, preferences are given to the robots which have successfully completed the same task or its portion, whatever was assigned to it, within specific time limit. Also the robots that have shown a positive response to the tasks assigned to them in general, obtain more weight than others. Reallocating tasks to these robots improve the chance of successful completion of a task. Hence, percentage of successfully completed tasks increase along with the decrease in the percentage of reallocated tasks. These are evident from figures 3 and 5. As the number of tasks become huge, percentage of successfully completed tasks decrease (and percentage of reallocated tasks increase) for all the task allocation schemes have been compared here. The reason is possible unavailability of robots with sufficient energy or priority collision among the tasks or shortage of time in certain cases.

As the required number of task reallocation in FESA is much lesser than those in EOTA and ATA, the delay in completion of each task in FESA is lesser than its competitors. It may be noticed from figure 4 that the delay increases with increase in number of tasks for all the schemes compared here. This is due to increased number of job reallocation as a result of huge energy consumption, unavailability of suitable robots etc.

IV. COMPLEXITY OF FESA

In this session, I have computed both the time and space complexity of FESA.

4.1 Worst Case Time Complexity

Let, at any point of time, total N number of robots are there in the system busy with K number of tasks. So, the number of free robots is (N-K). Among those K tasks, one particular task needs to be reallocated and during that time no other task with higher priority is waiting to be allocated and reallocated. Also assume that at most HT number of entries may appear in the history table and at most FT number of entries may be there in ptr_robotarray corresponding to each task in the TASK table. The maximum size of task table is ST.

TRAC has to evaluate the reallocation efficiency of (N-K) number of available robots. So, the time complexity TC of FESA is as follows:

TC = (N-K) ¦ (6)

Where ¦ is the complexity to evaluate reallocation efficiency of each robot.

To compute the residual energy to complete reallocated portion of the task, at most (ST+FT) number of records in ptr_robotarray corresponding to the desired task id needs to be scanned. For determining $E_R(t)$ and $Ethres_R$ entire ROBOT table should be scanned in worse case. So, the complexity involved in this case is N. For determining the parameter history_of_support, at most HT entries in HISTORY table, FT entries in ptr_robotarray in TASK table and the entire task table (for determining the value of T_C(A)) should be read in worst case, resulting into the complexity (HT+FT+ST). Complexity of computing distance_quotient is O(1) and the same for computing failure quotient is (ST´ FT) because at most FT records will have to be scanned for all the tasks in the task table to find out the attitude of a robot towards the tasks given to it, in general, not corresponding to one particular task. So, the overall complexity for determination of parameters of TRAC, is (ST+FT+N+HT+FT+ST+ST´ FT) i.e. (N+HT+2FT+2ST+ST´ FT). As far as the rule base tables are concerned, access to exactly one cell of each table is required resulting into total 3 table accesses. Hence, the overall complexity ¦ for evaluating the reallocation efficiency of one robot is (N+HT+2FT+2ST+ST´ FT+3). So, TC is O(N(N-K)).

4.2 Worst Case Space Complexity

Space complexity is due to the storage of ROBOT table, HISTORY and TASK table with their respective contributions being N, HT and (ST´ FT) and three rule base tables each having 25 entries. Hence, the overall space complexity is (N+HT+ ST´ FT+75) i.e. O(N).

V. CONCLUSION

The proposed method FESA is a fuzzy controlled task allocation-reallocation mechanism that analyzes the reallocation efficiency of a robot based on the history of its behavior, its residual energy along with its energy threshold with respect to the minimum energy required to complete the portion of the task to be reallocated, distance of the new robot from the old one and general tendency of the new robot towards the tasks assigned to it. Extensive simulation has been conducted and results are very promising from the perspective of energy optimization as well as optimization of task execution. In future, I have planned to extend the work by incorporating some real life experiments with different kinds of robots and tasks.

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FPGA IMPLEMENTATION OF LOW POWER RCHITECTURE FOR ADAPTIVE NOISE CANCELLATION

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ABSTRACT

This paper presents the VLSI implementationof Adaptive noise cancellation based on LMS algorithm. The main goal of this paper is to reducing the noise signal and also to verify the functionality and performance of the noise cancellation using audio input. At the beginning the adaptive parameters are obtained by simulating Noise cancellation on MATLAB. Simulink model of adaptive noise canceller was developed and the noise is suppressed to a much larger extent in recovering the original signal. The given elements of input and output signals, desired signal, step size factor and coefficient so adaptive filter was processed by FPGA .After that, the functionality of the FPGA based system structure for Adaptive noise cancellation on Least Mean Square algorithm was simulated, implemented and synthesized on Spartan-6 FPGA XC6SCX45T-2CSG324 board. Area and timing reports are given for particular target device. The power dissipation of 0.084W is obtained and the proposed system for different clock frequencies is estimated using Xilinx ISE 12.1 tool.

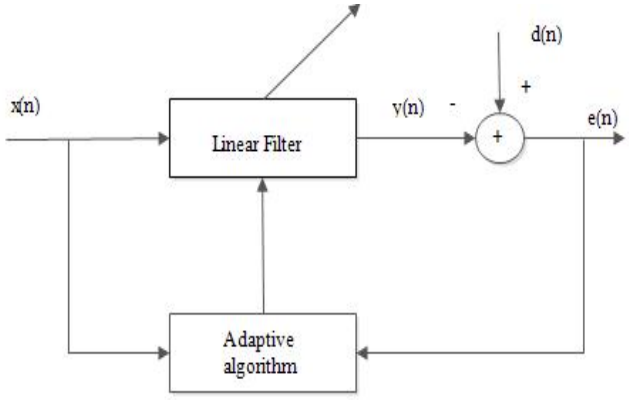
Key Words– LMS Algorithm , Adaptive Filter, Error Estimation, MATLAB/SIMULINK, Spartan - 6 FPGA XC6SCX45T-2CSG324 XILINX ISE 12.1.

I.INTRODUCTION

Speech is a very basic way for humans to convey information. It has a bandwidth of only 4 kHz; it can convey information with the emotion of a human voice. Certain properties of the speech signal are, it is a one dimensional signal, with time as its independent variable, it is random source in nature, and also it is non-stationary, and the frequency spectrum is not constant in time. Although human beings have an audible frequency range of 20 Hz to20 kHz, the human speech has significant frequency components only up to 4 kHz .The most common. problem in speech processing is the effect ofinterference noise in the signals[8]. This noise masks the speech signal, reduces its intelligibility and also in noisy environment speech communication is greatly affected by the presence of background acoustic noise. The presence of background noise in speech significantly reduces the intelligibility of speech. Noise reduction algorithms are used to suppress such background noise and improve the perceptual quality and intelligibility of speech. Removing various types of noise is difficult due to the random nature of the noise and the inherent complexities of the speech. The performance of noise cancellation technique using adaptive filters depend on the quality and intelligibility of the Processed speech signal. The improvement in the speech signal to noise ratio is the target of this technique.[11]

II.ADAPTIVE FILTER

Adaptive filter automatically adjusts the parameters of the system to achieve optimal performance according to some criteria. Adaptive filters are having wide range of applications such as noise cancellation, System identification, channel equalization and beam forming etc. The block diagram of adaptive filter is shown in Fig.1.Adaptive filters are generally designed as finite impulse response (FIR) filters due to the fact that these filters can provide a linear phase response and always stable.



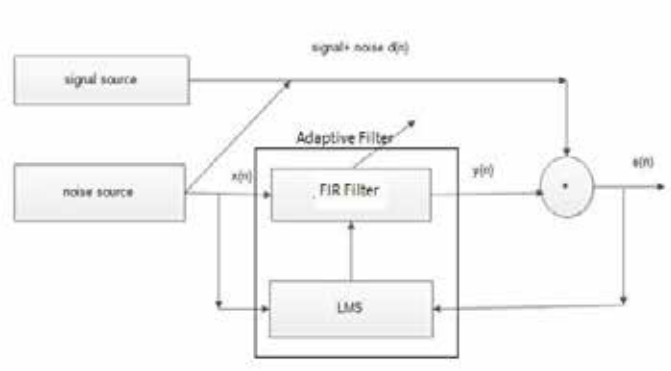


Fig.1: Block diagram of Adaptive filter **Fig.2 :Block diagram of Adaptive noise cancellation**

Least Mean Square algorithm (LMS) is used to implement adaptive noise canceller because of its simplicity and low complexity. Performance of adaptive filters using LMS algorithm is better in relation with the number of iterations required for convergence when compared with other algorithms. The design tools should be chosen carefully as the signal processing applications enforce substantial limits on area, power dissipation, speed and cost. Digital signal processors (DSPs), Field programmable gate arrays (FPGAs) and application specific integrated circuits are the most widely used tools for the design of such application. The DSP used for every complex math-intensive tasks but can't process great sampling rate applications due to its architecture. ASIC faces lack of flexibility and need extensive design cycle. The limitations of DSP and ASIC are overcome by single FPGA [4]. Therefore FPGA has become the best choice for the signal processing system designs due to their greater flexibility and greater bandwidth, resulting from their parallel architecture[5].

This paper is structured as follows : Section III gives brief overview of LMS algorithm and weaknesses of current techniques .Section IV presents the proposed system of noise cancellation. Section V shows the hardware implementation and software simulation results and section VI is conclusion of the paper. This paper investigates the applicability of FPGA system for adaptive noise cancellation[6] ineffective and in expensive way.

III.LMS ALGORITHM

The least mean squares (LMS) algorithms adjust the filter coefficients to minimize the cost function Compared to recursive least squares (RLS) algorithms, the LMS algorithms do not involve any matrix operations. Therefore, the LMS algorithms have fewer computational resources and memory than the RLS algorithms. The

implementation of the LMS algorithm is less complicated than the RLS algorithm.[5] However, the Eigen value spread of the input correlation matrix, or the correlation matrix of the input signal, might affect the convergence speed of the resulting adaptive filter. Least mean squares (LMS) algorithm are a class of adaptive filter used to mimic a desired filter by finding the filter coefficients that relate to producing the least mean squares of the error signal (difference between the desired and the actual signal).The least mean squares (LMS) algorithms adjust the filter coefficients to minimize the cost function. And it require fewer computational resources and memory. The implementation of the LMS algorithms also is lesscomplicated. The output of the filter y (n) is given by Equation (1),

$$y(n) = w^T(n)x(n) \quad (1)$$

Where w (n) is weight vector and the error signal is given by Equation (2),

$$e(n)=d(n)-y(n) \quad (2)$$

Substituting (1) in (2) yields

$$e(n)=d(n)-w^T(n)x(n) \quad (3)$$

According to the mean square error criterion Optimum filter parameters Wopt should make £=E{e^2(n)}, as minimum.

The mean square error can be expressed as in Equation (4),

$$£=E\{d^2(n)\}-2w^Trxd+w^TRxxw \quad (4)$$

Where rxd =E{x(n)d(n)}, is cross-correlation vector and Rxx = E{x(n)X^T (n)}, is autocorrelation matrix. It can be seen that the mean square error is a quadratic function of Wopt, and the matrix Rxx is positive definite or positive semi definite, so it must have a min value. Due to this gradient of W is zero, so the minimum when wopt meet Δ£=0 and when Rxx get a unique solution wopt=Rxxrxd, is considered.In LMS algorithm the gradient of the instantaneous squared error can be used instead of the gradient of the mean square error. To update the weights for each iteration of theAdaptive filter a step size parameter μ is introduced to control speed of convergence of the algorithm.

$$w(n+1) =w(n) + 2\mu e(n)x(n) \quad (5)$$

The step size parameter affects the stability, convergence speed and steady state error, so to reduce steady state error Small step size is used but it decreases the speed of the convergence of the algorithm. For better speed of convergence the step size value is increased but this affects the filter stability.

IV. ADAPTIVE NOISE CANCELLATION

Adaptive noise cancellation algorithms utilize two signal. One signal is used to measure the speech + noise signal while the other is used to measure the noise signal alone. The technique adaptively adjusts a set of filter coefficients so as to remove the noise from the noisy signal. This technique, however it requires that the noise component in the corrupted signal and the noise in the reference channel have high coherence. With large separations the coherence of the noise is limited and this limits the effectiveness of this technique.

Figure.2 shows the adaptive noise cancellation setup. In this application, the corrupted signal passes through a filter that tends to suppress the noise while leaving the signal unchanged. This process is an adaptive

process, which means it cannot require a priori knowledge of signal or noise characteristics.[12] .An adaptive filter automatically adjusts it shown impulse response through an LMS algorithm. The key objective of this paper is to provide an idea for FPGA Implementation of LMS algorithm for Adaptive Noise Canceller. Xilinx Spartan6 FPGA is used for synthesis [11].The advantage of the process is its adaptivity and real time application.

V. RESULTS AND DISCUSSION

5.1 MATLAB simulation

The design implement the FIR filter with 5 taps. The coefficients for the filter are extracted using Remez command in MATLAB. The speech signal having the frequency of 16 Hz is used as the input. A bird's eye view of the speech signal is used as the input for the system. The speech signal is desired using samples and the sample values are used as the inputs for the system.Gaussian noise generator is used as the error signal. So in the LMS filter block input signal, desired signal, adaptive, step size and reset input ports. And output , error are used as the output ports. In noise cancellation, the Gaussian noise is given to the input signal and Gaussian noise + speech signal is given to the desired signal. Then output signal from LMS filter is given to the input of the Adapt port ,step size is maintained at 0.002.Then the output is connected to the audio device. Figure.3 shows The Simulink implementation of the noise cancellation system.

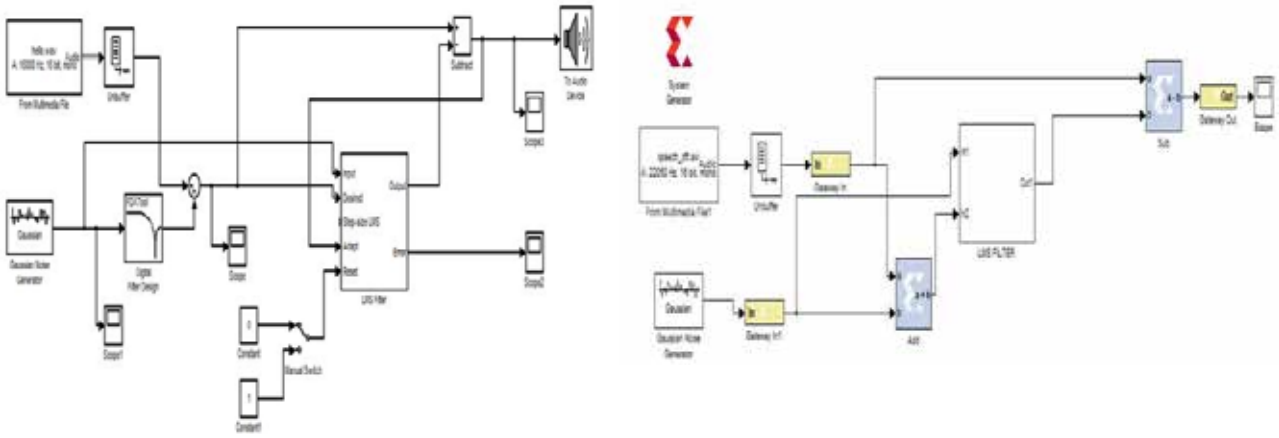


Fig.3: Simulink model of adaptive noise cancellationFig.8 :Xilinx model of simulink implemention of ANC

5.2 MATLAB simulation results

Environmental noise polluted sinusoidal signal is extracted. Noise signal is modelled as Gaussian noise. The two signals are added and are used as the inputs for of LMS adaptive filter. The other input to the noise cancellationsystem is Gaussian noise signal. The qualities of outputs are examined to interpret the characteristics of the noise cancellation system. Evaluation of the proposed noise cancellation system is done through simulation outputs for the various steps sizes. If the step size parameter is kept high the response is fast but is less accurate and vice versa.The difference of desired Signal and Input Signal is the error Signal which is obtained from error Signal output port of LMS block. The Signal from this port is the Filtered Signal from

which Noise has been adaptively removed out.[7]

The error signal value decreases as the iteration proceeds and emulating the desired signal more effectively cancelling the noise. MATLAB simulations are carried out with different steps size to optimize the step size for better convergence of the algorithm. Adaptive parameters are obtained through MATLAB simulations are used as the inputs for the hardware to be implemented on FPGA. The Figure.4 and 5 shows the input Gaussian noise signal and desired signal respectively.Figure.6, and Figure.7 shows the adaptive noise canceller Simulink Model scope output. Figure.4 represents noisy signal entering into the system. Figure.5shows the noisy and speech signal entering into the system. Figure .6 shows the signal obtained after Adaptive filtering. By varying the step size parameter of LMS for noise cancellation is observed. Higher the step size, fast the convergence rate.

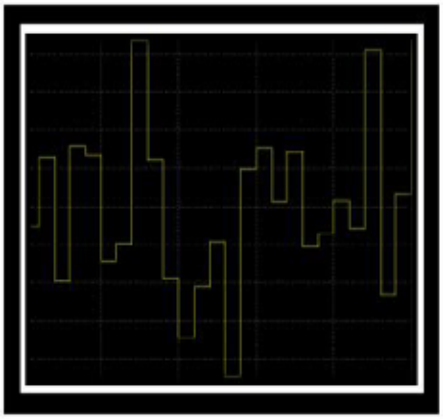


Fig.4: input Gaussian signal

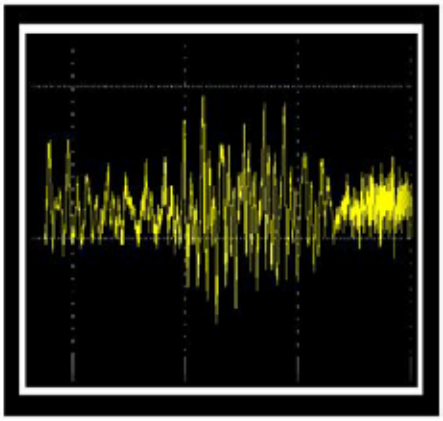


Fig.5: desired signal

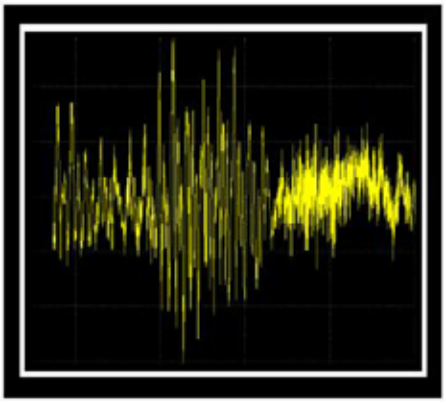


Fig.6: original speech signal

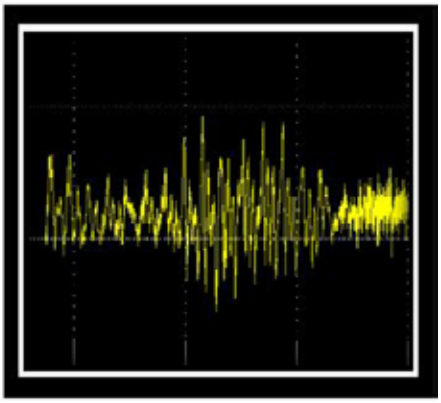


Fig.7: Error signal

5.3 FPGA implementation using Xilinx

The Simulink implementation of the noise cancellation system is shown in Figure.8. It consists of 3 blocks: Input signal, desired signal and Adaptive filter. Here x(n) is the analog input signal which is applied to the one of the input of adaptive filter. Which convert analog to digital form ,the output of the digital filter block is d(n).[3]

The Xilinx 12.1 development environment was used for implementation of MATLAB design. The design has been transferred to VHDL code and it's the hardware simulation done with the Xilinx ISE simulator and also

implemented on Spartan-6 FPGA XC6slx45t-2csg324 board.Apply x(n) the input random signal with 1024 samples and d(n) to the Adaptive FIR filter . The adaptive filter starts compare d(n) with x(n) and produces the output e(n). The Adaptive FIR Filter updates the coefficients using LMS algorithm based on the error signal generated using input speech signal and estimated output of adaptive filter.

5.4 .Xilinx results

The input signal of Gaussian noise is sampled and that is fed to the one of the input of Xilinx Model[3]. The desired signal of Gaussian noise and speech signal is also sampled and that is given to the another input of Xilinx model. In this Xilinx model have to discuss about the minimum period required for system, combinational path delay, maximum frequency required for the system and power dissipation of the system.The test bench is developed in order to test the modelled design. This developed test bench will automatically force the inputs, which are taken from the reference, and will make the operations of algorithm to perform. Timing reports include total time delay for output to appear after giving input.

At speed grade of -12, design operates at maximum frequency of 135.66MHz.Theminimum period require is 7.376ns and combinational delay is 3.723ns.The power dissipation of the proposed architecture for different clock frequencies is estimated by Xilinx Power tool 0.084watts. The proposed design implemented on Spartan 6 based FPGA can work at maximum operating frequency. The total power consumption of the proposed design based on XC6SCX45T-2CSG324FPGA device has been calculated.The simulation results showed in below Figure.9.The values of x (n) are stored in a delay register and registers are required for each weight coefficient. Each unit contains a slice of the shift registers, an adder and a multiplier. It also consist an output register, but this is optional. Table.1 shows the Xilinx device utilization summary.TABLE.II represents the performs comparison of Vakulabharanam Ramakrishna & Tipparti Anil Kumar(2013) where in the base design and previous works viz., Sujith Chatrad & Asha (2013), Jebin Roy & Ramya (2014) designs. In previous work ,the power dissipation of the noise cancellation system is high and combinational path delay also high.

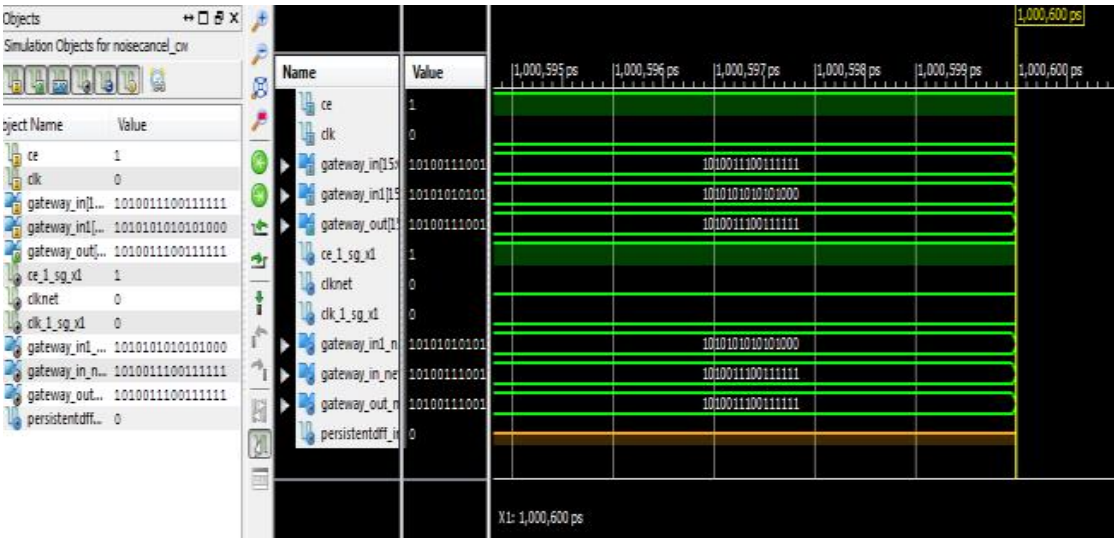
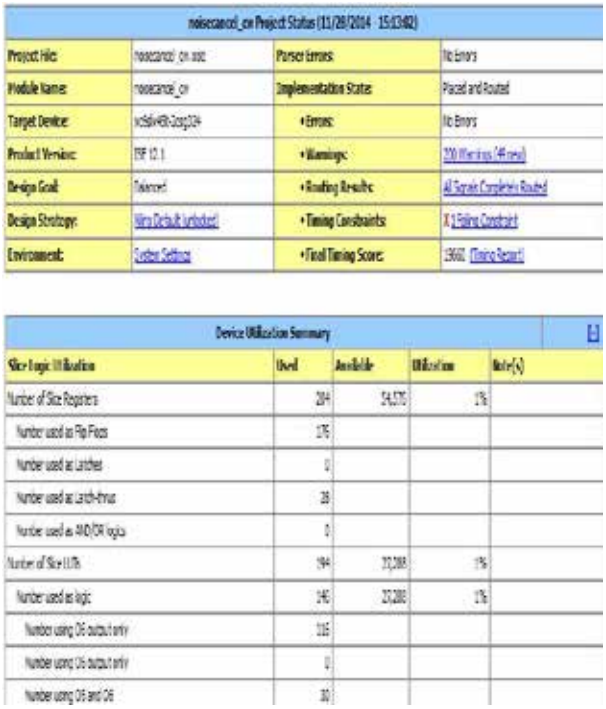


Fig.9: Output waveform of proposed ANC

The proposed method reduces the Area ,power dissipation and Combinational path delay.The design operates at maximum frequency of 135.66MHz.The minimum period require is 7.376ns and combinational delay is

3.723ns.The power dissipation of the proposed architecture for different clock frequencies is estimated by Xilinx Power tool 0.084watts. The proposed design implemented on Spartan 6 based FPGA can work at maximum operating frequency. The total power consumption of the proposed design based on XC6SCX45T-2CSG324 FPGA device has been calculated.

TABLE.I Device utilization summary of ANCTABLE.II represents the comparison of previous work and proposed work of the noise cancellation system.



noisecancel_cm Project Status (11/28/2014 - 15:03:02)			
Project File:	noisecancel_cm.xise	Parser Errors:	No Errors
Module Name:	noisecancel_cm	Implementation State:	Placed and Routed
Target Device:	xc6slx45t-2csg324	• Errors:	No Errors
Product Version:	ISE 12.1	• Warnings:	200 Warnings (46 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Signals Completely Routed
Environment:	System Settings	• Final Timing Score:	13662 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	284	54,576	1%	
Number used as Flip Flops	276			
Number used as Latches	0			
Number used as Latch-thrus	28			
Number used as AND/OR logics	0			
Number of Slice LUTs	194	27,288	1%	
Number used as logic	146	27,288	1%	
Number using O6 output only	116			
Number using O5 output only	0			
Number using O6 and O5	30			

Design	Power dissipation (Watts)	Delay(ns)	Max. Operating frequency (MHz)
Sujith Chatrad & Asha (2013)	0.156	3.738	137
Jebin Roy & Ramya (2014)	0.1789	3.76	105
Base paper - Vakulabharanam Ramakrishna & Tipparti Anil Kumar(2013)	0.084	3.723	135.66

VI.CONCLUSION

The method of Adaptive noise cancellation System provide a signal free from noise. The adaptation of filter coefficients is effected using LMS algorithm technique. The LMS algorithm is suggested to reduce the number of coefficients for low computational complexity. Through implementation and survey it has been found out that using pipelined architecture as computational unit makes implementation of adaptive filters easier. Numbers of registers and delays were adjusted the coefficient value to achieve speed of operation, while minimizing approximation error. The implementation results of adaptive noise cancellation system in Spartan 6 FPGA board revealed better area and power reduction compared to power approaches with the power consumption of 0.084 watts. In addition with the proposed approach there is a high possibility for pipelining to achieve higher throughput facilitating real time implementations.

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VakulabharanamRamakrishna&TippartiAnil Kumar, (2013)"Low Power VLSIImplementation AdaptiveNoise
Canceller based onLeastMean Square Algorithm",IEEE Transactions on Circuits and Systems - Ii: V No.60.

IMPLEMENTATION OF INTELLIGENT CONTROLLER FOR A NON-LINEAR PROCESS

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ABSTRACT

This paper presents the real-time implementation of a neural network based controller for a non-linear process. The control structure is demonstrated on a conical tank system (CTS).The control of liquid level in a conical tank is non-linear due to variation in the area of cross-section of the tank system. So designing a controller for conical tank presents a challenging problem.PID controller is the classical control algorithm in the field of process control. Major limitation of PID is that it shows poor performance with non-linear and interacting processes. This can be overcome by soft-computing techniques like neural network, fuzzy logic, etc. From the results it is observed that neural network based controller shows faster settling time and minimum overshoot.

Keywords: Artificial Neural Networks, Internal Model Control (IMC), Non-linear process, PID controller.

I INTRODUCTION

In real-world applications, most of the industrial processes are non-linear in nature. The control of such non-linear process is a difficult task. There are different types of controllers applied to process to maintain the desired level. The optimum setting for PID tuning is proposed by [1]. The design of PID controllers for unstable FOPTD model was described by [2]. Although PID controllers have advantages on linear systems, these controllers are not suitable for systems with time-delay, high-ordered, nonlinear systems. This gained the researchers attention towards intelligent control schemes. A two-level, optimization based method for deriving tuning parameters for PID was proposed by Mhaskar [3]. It is demonstrated on a non-linear Continuous Stirred-Tank Reactor (CSTR) which has the response similar to the non-linear controller. Artificial Neural Networks (ANN), in recent years has become an attractive tool to construct complex non-linear process models [5]. Chen [8] described an improved conventional PID control structure using linearization through neural network for a non-linear process. It has several advantages. One of which is the linear control scheme applied to the non-linear control design has less computation compared to non-linear counterpart based on non-linear neural network model. Shu [7] proposed a PID Neural Network for time-delay systems which resulted in short convergence time and quick learning speed and can be applied to practical processes. IMC based Neural Network to adjust the control parameters for roll motions of the container ship were described by Fust Alarcin [6]. A robust neural network based intelligent

controller for a Continuous stirred-Tank Heater (CSTH) was developed by Gaurav [4]. The result shows that the proposed ANN controller well tracks the set-point variations and also rejects the unwanted load disturbance.

In this paper, implementation of neural network based controller for controlling liquid level in a conical tank is presented. The issue of analysing the dynamic behaviour of process represented by non-linear models is the main concern in this work; this is motivated by the fact that situations do arise when it is undesirable to neglect the inherent nonlinearities of a process.The conical tank system which exhibits the non-linearity is taken as system for the research.It is highly nonlinear due to the variation in area of cross section of the level system with height. The performances are compared with conventional IMC-PID controller and the results are tabulated.

II TEST SYSTEM

The conical tank system (CTS) that is available in the institution is taken as the test system. The schematic of the CTS is shown in figure.1. The real time system has a conical tank, reservoir and water pump, current to pressure convertor, compressor, Differential Pressure Transmitter (DPT), DAQ chord and a Personal Computer which acts as the controller and forms a closed loop. The inflow rate to the conical tank is regulated by changing the stem position of the pneumatic valve by passing the control signal from computer to I/P converter through digital to analog converter (DAC). The operating current for regulating the valve position is 4-20 mA, which is converted to 3-15 psi of compressed air pressure. The water level inside the tank is measured using DPT and converted to an output current range of 4-20 mA. This output current is given to the controller through analog to digital converter (ADC). The DAQ card is used for interfacing the personal computer with the conical tank system thus forming a closed loop.

Fig.1 Conical Tank Trainer

III SYSTEM IDENTIFICATION

System identification is normally done using step response methods. The process dynamics is analysed from open loop response with varying input percentages. The percentage of opening of control valve which is a manipulated variable is chosen as 32%, 35%, 38%, 40%, 42%, 45%. The open loop response of the system is shown in Fig.2. The system is found to be first order plus dead time process (FOPDT). Therefore the transfer function for FOPDT process is given by the equation,

$$G(s) = \frac{ke^{-tds}}{Ts+1}$$

From the open loop response, transfer function for all control valve position is found from the TABLE.I given below.

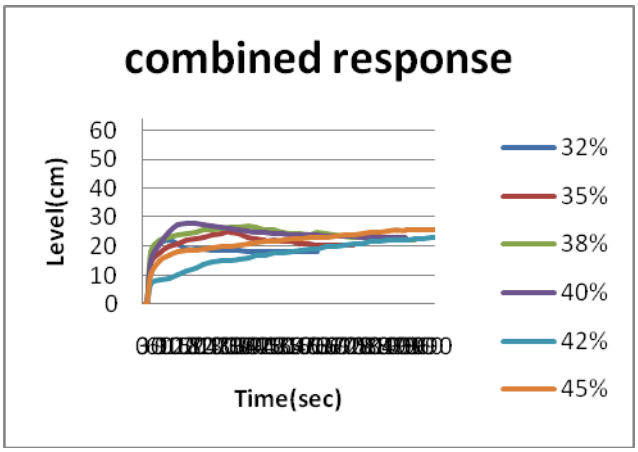


Fig.2 Open loop response

TABLE.I Transfer function

Input(%)	System gain (k)	Delay time (T_d)	Time constant (τ)
32	1.12	14	22.02
35	1.09	8	35.55
38	1.09	7	31.17
40	1.08	12	30.31
42	1.03	17	49.77
45	1.11	15	43.63

IV CONTROL STRATEGIES

4.1. IMC Tuning Technique

The IMC technique is one of the recent traditional tuning techniques that yield better values among the techniques available for conventional methods. The controller has to be designed for maintaining the optimal set point of the system after deriving the transfer function model. This can be achieved by properly selecting the tuning parameters k_p, K_i, $k_d$for a PID controller. The tuning parameters for First Order Plus Delay Time (FOPDT) is given below,

$$\mathbf{K_p} = 2T + C/2k(\lambda + \tau)$$

$$\mathbf{K_i} = 1/\tau_i \; ; \qquad \boldsymbol{\tau_i} = T + (\tau/2)$$

$$\mathbf{K_d} = T\,\tau/(2T + \tau)$$

Where $\lambda = 0.25\,\tau$

4.2. Perceptron Network

The perceptron is an algorithm for supervisedclassification of an input into one of several possible non-binary outputs. It is a type of linear classifier, i.e. a classification algorithm that makes its predictions based on a linear predictor functioncombining a set of weights with the feature vector. The algorithm allows for online learning, in that it processes elements in the training set one at a time.

ALGORITHM:

The following steps have to be followed while training the network.

Step 1: Initialize weights and bias.

i.e, $w_1, w_2, \ldots w_n = b = 0$ and

learning rate α= 0 to 1.

Step 2: Activate the inputs.

$X_i=S_i$

Step 3: Calculate the net input to the output unit

$$Yin = \sum_i xi.wi$$

Step 4: Calculate Y.

$$Y= f(Yin) = 1 ; Yin > \theta$$

$$0 ; -\theta < Yin < \theta$$

$$-1; Yin < -\theta$$

Step 5: Match with target.

If Y = t, $w_i(new) = w_i(old)$

$b(new) = b(old)$

if Y ≠ t, $w_i(new) = w_i(old) + \alpha.t.x_i$

$b(new) = b(old) + \alpha.t$

Step 6: Stop the iteration once all targets are reached.

V SIMULATION

5.1. IMC Tuning Technique

The Simulink model and closed loop response using IMC tuning technique is obtained for 40% with k_p=0.59, k_i=0.023, k_d=10.10 is shown in fig.6.1 and 6.2 respectively.

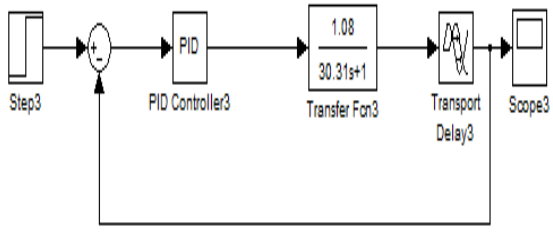


Fig.6.1. Simulink model for IMC

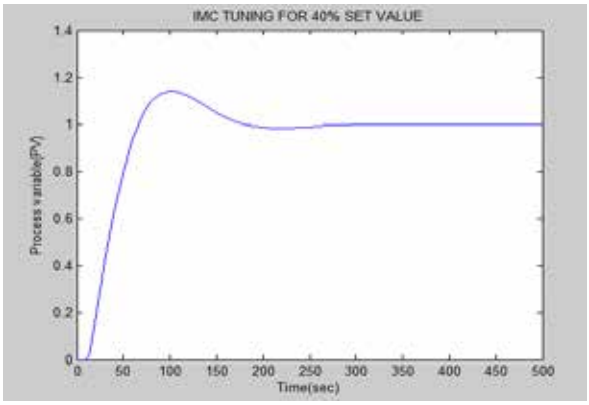
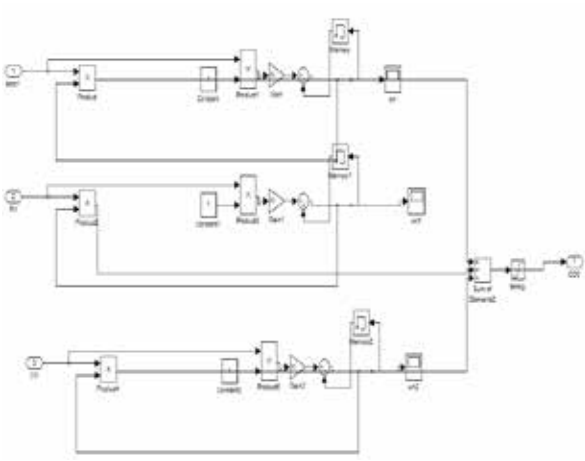


Fig. 6.2. Response of IMC

5.2. Neural Controller

The MATLAB Simulink model for neural controller trained using perceptron network and its response is shown in fig.6.3 and 6.4 respectively. Here the inputs used to perform control action are error signal which is the difference between process variable and set point, process variable (PV), controller output (CO).



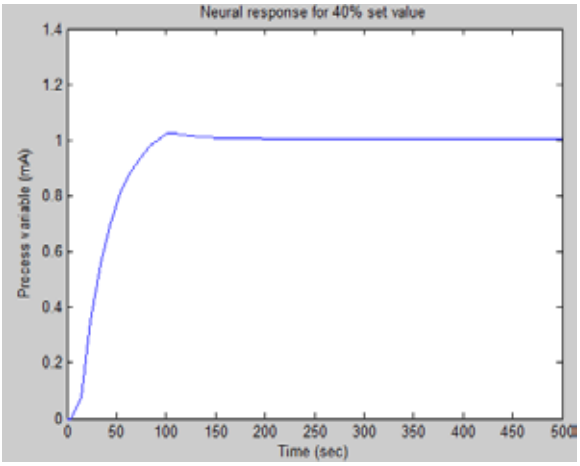


Fig.6.3. Simulink model of perceptron controller Fig.6.4.Response of perceptron controller

VI CONCLUSION

From the simulation results obtained for different setpoint values, neural network controller shows better performance compared to conventional IMC tuning technique. The perceptron neural network controller has fast settling time and minimum overshoot. Thus neural network controller can be applied to nonlinear varying processes.Table.2 shown below shows the comparison between the performances of IMC tuned controller and neural controller.

TABLE.II Comparison between IMC and Neural controller

Inputs %	Settling time (sec)		Peak overshoot	
	IMC	Neural controller	IMC	Neural controller
32	180	150	1.1	1.05
35	280	150	1.2	1.02
38	330	150	1.2	1.015
40	280	200	1.15	1.025
42	430	300	1.16	1.028
45	400	250	1.16	1.032

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A MOSFET AND CNTFET BASED DESIGN OF MULTIVALUED LOGIC

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ABSTRACT

In modern VLSI systems a large proportion of power is consumed by interconnect and switching. The reduction of static and dynamic power dissipation are the major challenges in the rapid growth of the VLSI technology. With the emerging nanometric technologies, Multiple valued logic(MVL) circuits have attracted significant attention due to its advantages in information density and operating speed. The main contributions include the implementation of Ternary logic in the Carbon Nano Tube FET's (CNTFET) and their various performance metrics like static power consumption, propagation delay and power delay product are compared with the existing MOSFET based ternary logic gates. Compared to the complementary logic family the pseudo – NCNTFET MVL logic family requires a smaller circuit area with a similar propagation delay on average, with a larger power delay product and static power consumption.

Keywords: Multiple valued logic, carbon nanotube field-effect transistor, ternary logic, power delay product.

I. INTRODUCTION

The scaling of CMOS technology has not brought significant improvements in integrated circuits, but it has also raised the power consumption in advance digital designs. As CMOS approaches physical and technological limits, new devices have been proposed to implement nanoscale circuits, such as those based on multiple-valued logic (MVL). Traditionally the digital computation is performed on two valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean space. Multiple-valued logic allows more than two levels of logic; implementations of ternary, quaternary, penta for various applications. MVL enjoys many advantages over its binary counterpart; for example, each wire can transmit more information, so that the number of interconnections in the chip can be reduced, resulting in a lower circuit complexity. In particular, CNTFETs have attracted significant attention as an alternative to silicon-based Mosfets for implementing MVL gates due to its potential advantages such as high mobility of charge carriers.

II. MULTI VALUED LOGIC

Multiple-valued logic allows more than two levels of logic; implementations of ternary, quaternary, penta for various applications. MVL enjoys many advantages over its binary counterpart; for example, each wire can transmit more information, so that the number of interconnections in the chip can be reduced, resulting in a lower circuit complexity. Multi value logic replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic.

With an increasing density of chips, the number of inter chip connections is greatly increased as more and more functions are put on the same chip; thus, the size and performance of the chip is mostly dominated by wiring rather than devices. One of the most promising approaches to solve the interconnection problems is the use of multiple-valued logic (MVL) inside the VLSI chip. The number of interconnections can be directly reduced with multiple-valued signal representation. The reduced complexity of interconnections makes the chip area and the delay much smaller than others.

From the view point of reduction of interconnections, advantages of K-valued logic system in submicron VLSI is chip density. The chip area in submicron VLSI is almost determined by the interconnections. In K valued logic the number of interconnections can be reduced to1 / log2 K in comparison with binary logic. If this effect can be applied to 2-dimensional geometry, the reduction ratio becomes 1/(log2 K)2 .

The total area of interconnections is determined by the number of interconnections and their length. The interconnection length is also determined by the complexity of the interconnections, so that it is clear that the use of MVL is very useful for compact VLSI implementation.

2.1 Logic Levels of Switching

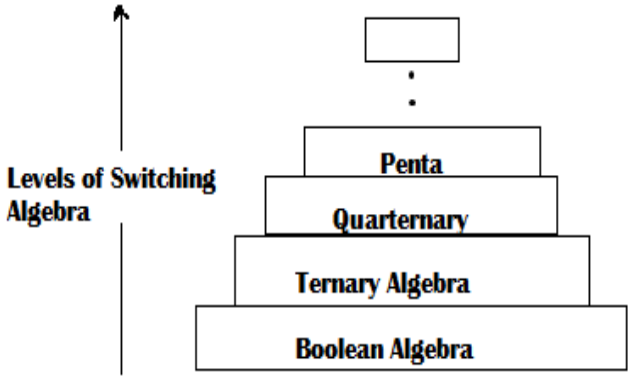


Fig. 2.1.1 Logic levels of switching

Logic gates constitute the foundation blocks for digital logic. Traditional binary gates are use in current digital devices. The multivalued logic gates have not been standardized but ternary and quaternary gates are two commonly used multivalued logic gates described in literature.

2.2 Ternary Logic

The most generally used switching circuit components today are two-valued or binary. The electrical conditions controlling these switching circuit components are also generally two-valued or binary. But integrated circuits can now handle multiple valued signals & switching at high speed rather than binary signals, especially at data communication level because of the reduced interconnections & switching [6].

Utilization of multi valued logic (MVL) reduces the number of signals involved in the communication, increasing their information content. In such a way, an interconnection-limited design can be realized with MVL like for the asynchronous circuits and comparable performance than a classical binary design may be obtained [7]. Among various types of MVL, the ternary logic receives more attention than others because of lower interconnection cost estimation and a simple electronic circuit implementation method [8].

Ternary and quaternary circuits have been studied increasingly in recent years. Quaternary circuits have the practical advantage that a four-valued signal can easily be transformed into a two-valued signal. However, based on the following considerations, we feel that ternary circuits may be of more theoretical significance than others:

- Since 3 is the smallest radix higher than binary, ternary functions and circuits have simpler form and construction. They can be studied and discussed easily, yet they still display the characteristics of multivalued elements.
- As a measure of the cost or complexity of multi- valued circuits, the product of the radix and the number of signals has been proposed. Since 3 is the digit nearest to e = 2.718, ternary circuits will be more economical according to this measure.
- If balanced ternary logic (1,0, - 1) is used, the same hardware may be used for addition and for subtraction.
- Since 3 is not an integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.

Ternary gates are designed by the standard MOS technology in two ways. In one way, dynamically controllable circuits are suggested. Here it is necessary to include special clock oscillators that occupy a considerable area on the crystal and can cause an excess number of switching events and excessive noise components in digital circuits. The other way implies the design of ternary circuits that do not require any supplementary control signals.

2.3 Scope of Multivalue Logic

Since inception digital devices have been designed using binary logic till date. Researchers have found the development in binary logic is cumbersome, complex and difficult to understand. Since multivalued logic enables

more information to be packed in a single digit researchers have been working on multivalued logic for many years [1]-[3]. With development of novel electronic devices and optical devices, it is now possible to implements circuit for more complicated logic system [4]-[6].

Many of these devices are capable of dealing with more than two logic states but they are at experimental stage. Some multivalued logic systems such as ternary and quaternary logic schemes have been developed but successful implementation is yet to become available.

Ternary logic has several advantages over binary logic. Since it require half the number of digits to store any information than its binary equivalent it is good for storage; the ternary storage mechanism is less than twice as complex as the binary system.

Though their design principles of resistive loaded designs are valuable in various factors, they still suffer from large static power consumption due to the presence of resistors. Compared to the resistive loaded design the complementary logic family shows some improvement. But above all, the implementation of pseudo logic in the basic set of logic gates like inverter, nand and nor gate are presented in this project shows an efficient result and compared with the above implementations.

III. WAY OF IMPLEMENTING TERNARY LOGIC

3.1 MOSFET

CMOS integrated technology is considered to be the best choice for implementing the ternary logic circuits for the following reasons:

1. CMOS multivalued circuits are expected to share three principal advantages of CMOS binary circuits: zero static power dissipation in either stable state, low-output impedance in either state or elimination of passive elements (resistors).
2. Any multivalued signal can be transmitted through a CMOS transmission gate.
3. In contrast with the pn-junction threshold of a bipolar transistor, the MOS transistor's threshold may easily be changed during fabrication, simplifying the task of responding to a multilevel input signal.

3.1.1 Ternary Inverter

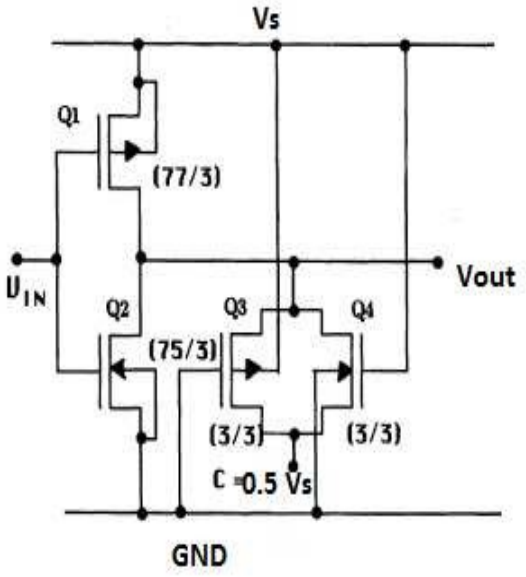
For the ternary inverter the inputs are given as {0, 1, 2} and it yields the output {2, 1, 0}. Because of its ability to produce {1} at the output, ternary inverter is used as the primary building block for the proposed SRAM cell and its CMOS implementation is based on the design in [2]. A high resistance transmission gate is connected between the output of a low-resistance threshold modified binary inverter and 0.5Vs to produce the middle level voltage [1]. As mentioned, the threshold voltage of transistors Q1 and Q2 is made half of the supply voltage whereas transistors Q3 and Q4 were simulated with threshold voltages as specified.

3.1.2 Ternary NAND Gate

A general ternary NAND is a device with two inputs x_1, x_2 and three outputs y_0, y_1, and y_2 such that $Y_i=C_i(z)$ Where $z=$ max (x_1, x_2) for i=0, 1 or 2. If the output is taken to be y_0, y_1, and y_2 the device is referred to as the negative

ternary NAND (NTNAND), a standard ternary NAND (STNAND), or a positive ternary NAND (PTNAND), respectively. On the other hand, if z= min (x_1, x_2) for i=0, 1 or 2, then the general ternary NOR will function as general ternary NOR.

The ternary nand gate were designed and implemented by connecting a CMOS transmission gate to the common drain output of a binary CMOS NAND gate. The transmission gate at the output helps to pull out the middle level voltage. If the output is taken to be y_0, y_1, and y_2 the device is referred to as the negative ternary NAND (NTNAND), a standard ternary NAND (STNAND), or a positive ternary NAND (PTNAND), respectively. On the other hand, if z= min (x_1, x_2) for i=0, 1 or 2, then the general ternary NOR will function as general ternary NOR.



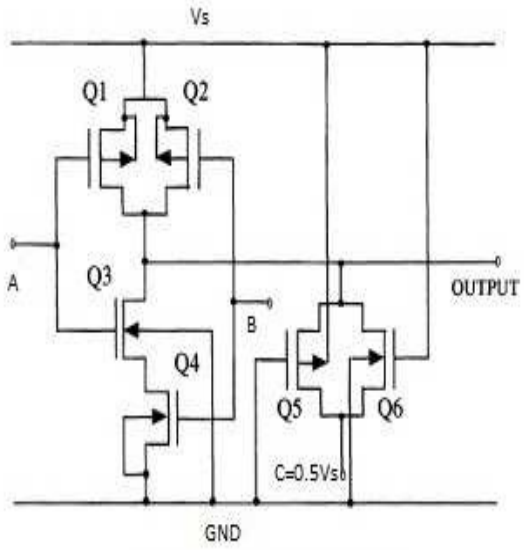


Fig 3.1 MOSFET – Ternary NOR Inverter **Fig 3.2 MOSFET – Ternary NAND Gate**

3.2 CNTFET

CNTFETs utilize semiconducting single-wall CNTs to assemble electronic devices [8]. A single-wall CNT (or SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (*n*,*m*). A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (*n*,*m*): the nanotube is metallic if $n = m$ or $n - m = 3i$, where *i*is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following

$$DCNT = \frac{\sqrt{3a0}}{\pi}\sqrt{n^2 + nm + m^2}$$

wherea_0 = 0.142 nm is the interatomic distance between each carbon atom and its neighbor. Fig. 1 shows the schematic diagram of CNTFET [14]–[16]. Similar to the traditional silicon device, the CNTFET also has four terminals. As shown in Fig. 1, undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state [8]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

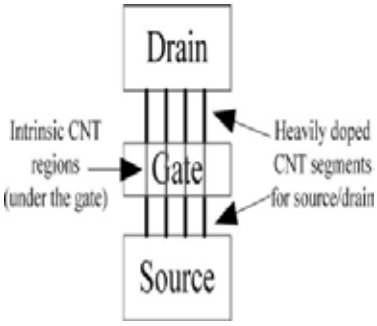


Fig 3.3CNTFET structure with four CNTs in channel

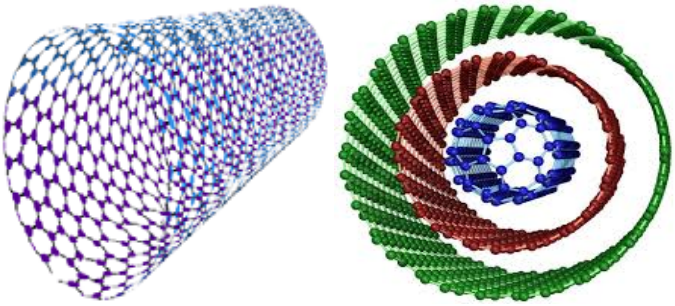
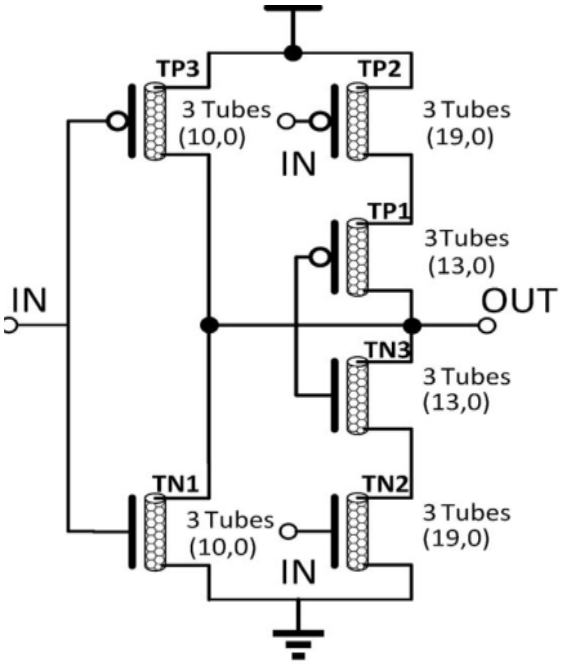


Fig 3.4 CNTFET – Single walled and Multiwalled Tubes

3.2.1 Ternary Inverter

One of the most widely used logic design style is static complementary CMOS; the main advantages of the complementary design are robustness, good performance, and low power consumption with small static power dissipation. A complementary CNTFET network can also be used for ternary logic design to achieve good performance, low power consumption, and to avoid the use of large resistors and reduce area overhead. Fig 3.5 consists of six CNTFETs. The chiralities of the CNTs used in T1, T2, and T3 are (19, 0), (10, 0), and (13, 0), respectively. From equation, the diameters of T1, T2, and T3 are 1.487, 0.783, and 1.018 nm, respectively. Therefore, the threshold voltages of T1, T2, and T3 are 0.289, 0.559, and 0.428 V, respectively. The threshold voltages of T5, T6, and T4 are −0.289, −0.559, and ‗0.428 V, respectively.

When the input voltage changes from low to high at the power supply voltage of 0.9 V, initially, the input voltage is lower than 300 mV. This makes both T5 and T6 turn ON, both T1 and T2 turn OFF, and the output voltage 0.9 V, i.e. logic 2. As the input voltage increases beyond 300 mV, T6 is OFF and T5 is still ON. Meanwhile, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output, and from the output to n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V, i.e., half of the power supply voltage. As shown in Table I, half V_{dd} represents logic 1. Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition.



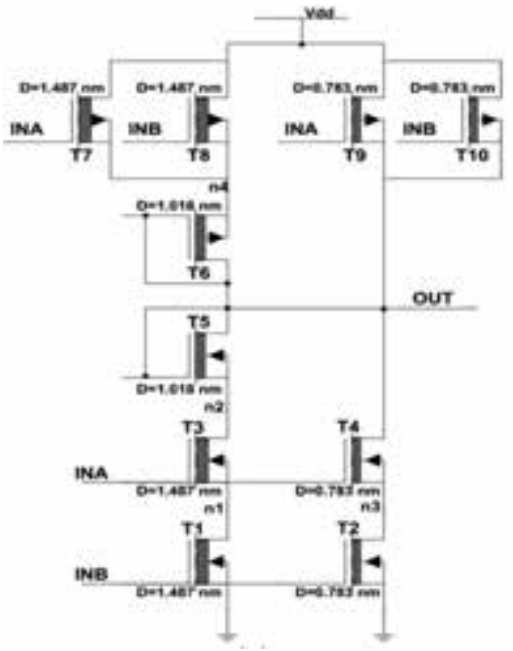


Fig 3.5 CNTFET – Ternary Inverter **Fig 3.6 CNTFET – Ternary NAND**

3.2.2 CNTFET - Ternary NAND

The circuits for the two-input ternary NAND is shown in Fig 3.6 respectively. Each of these two gates consists of ten CNTFETs, with three different chiralities. They are essentially the same as their binary CMOS counterparts, except for the transistors of different threshold voltages. In these two gates, similar to the STI circuit of Fig 3.5, the transistors with diameters of 1.487, 0.783, and 1.018 nm have threshold voltages of 0.289, 0.559, and 0.428 V, respectively, as established using threshold voltage.

IV. PSEUDO LOGIC

4.1 PSEUDO NCNTFET Ternary Gates

Pseudo-NMOS logic is an example of ratio-ed logic which uses a grounded PMOS load and an NMOS pull-down network that realizes the logic function [5]. The main advantage of this logic is it uses only N+1 transistors verses 2N transistors for static CMOS. In this logic the high output voltage for any gate is Vdd and the low output voltage is not 0volt. This results in decreased noise margin.

The main drawback of this logic is very high static power consumption as there exists a direct path between Vdd and ground through the PMOS transistor. In order to make low output voltage as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. But to increase the speed particularly when driving many other gates the PMOS transistor size has to be made larger. Therefore there is always a trade-off between the parameters noise margin, static power dissipation and propagation delay.

When the input is logic 0, TN1, and TN2 in all three designs [as shown in Fig 3.7 are OFF . Since the output is expected to be logic 2 and the P-type CNTFET has a strong capability to transfer a high voltage, TP1 and TP2 in the pseudo-NCNTFET STI [see Fig 3.5] are both working in the deep triode region (or deep linear region). The equivalent resistances of TP1 and TP2 are small and negligible, as shown in Fig 3.7. TP3 and TP2 in a complementary STI [see Fig 3.5] are both turned ON and operate in the deep triode region. Therefore, the static power consumptions for all three designs are very small under this scenario, as confirmed by the SPICE simulation results.

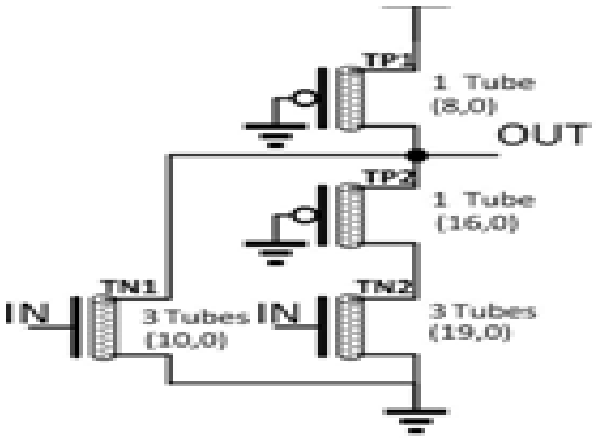


Fig 3.7 Pseudo NCNTFET Ternary Inverter

V. COMPARISON OF MOSFET and CNTFET

Binary and ternary logic gate function inverter and NAND logic are designed in both CMOS and CNTFET technologies. Power reduction is achieved in the ternary logic with the marginal cost of delay and hence the power delay product. Compared to MOSFET power delay product CNTFET shows greater reduction in power which is shown in the below table.

Circuit Model	MOSFET RESULTS			CNTFET RESULTS		
	DELAY	POWER	PDP	DELAY	POWER	PDP
BINARY_INVERTER	24ps	886uw	21.2f	22ps	48uw	1f
TERNARY_INVERTER	9ns	190uw	1.7p	8ns	6uw	48f
BINARY_NAND	60ps	704uw	42.2f	40ps	49uw	1.9f
TERNARY_NAND	10ns	277uw	2.7p	9ns	8uw	72f

Table: 5.1 Comparison of CMOS vs CNTFET for Inverter and NAND Gates

Circuit Model	MOSFET RESULTS			CNTFET RESULTS		
	DELAY	POWER	PDP	DELAY	POWER	PDP
Pseudo Binary Inverter	12.8ps	1.64mw	20.9f	11.3ps	1.42mw	16f
PseudoTernary Inverter	190ps	3.01mw	57f	9ns	1.06mw	9.5p

Table: 5.2 Comparison of Pseudo logic of MOSFET & CNTFET

VI. CONCLUSION

In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices. The binary logic is limited due to interconnect which occupies large area on a VLSI chip. This problem is overcomed by a heuristic methodology of implementing a multivalued logic such as a Ternary logic. Here low power dissipation MOSFET and CNTFET logics are implemented which is comprised of a set of ternary inverters and ternary nand gates. Extensive HSPICE simulation result shows that the proposed CNTFET designs shows a better improvement than the existing MOSFET based designs in various performance metrics. The later implementation of the pseudo- NCNTFET MVL requires a smaller area with a similar propagation delay but with larger PDP and static power. As a result, Ternary logic can be utilized when only power is a major concern and pseudo ternary logic can be used when transistor count and circuit area are important. Future work will address the reliability of proposed MVL designs and the effects of chirality variation.

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BIOGRAPHICAL NOTES

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DEVELOPMENT OF HYBRID ENERGY SYSTEM FOR OFF-GRID REMOTE AREA

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ABSTRACT

Renewable energy can be seen as one of the important prospect of today's research, as it enlightens the lives of millions of people by fulfilling multiple necessities of their daily life and simultaneously overcomes the ill effects caused by the non-renewable sources. Present study is based on the development of a hybrid energy system for supplying the load demand of 5 unelectrified villages of Almora district in Uttarakhand, India with the help of the available resources of the area such as solar, hydro, biomass and biogas with the addition of diesel generator by using HOMER software. HOMER software is used to analyze the best configuration among a set of systems for electricity requirement for 254 households whose total population is 965. The system is designed to fulfill the daily and the peak demand of each day. From the optimization results, it is found that an optimum HES comprising of 5 kW SPV, 20.5 kW hydro turbines, 5 kW biogas generators, 15 kW biomass gasifier, 5kW diesel generators and 10kW of converter with 20 storage batteries, has been found suitable for the study area. The COE and renewable fraction are 0.079 $/kWh as minimum and 81% as maximum respectively.

Keywords: Cost of Energy (COE), Hybrid Energy System (HES), HOMER, Net Present Cost (NPC), Renewable Fraction (RF).

I. INTRODUCTION

Rural electrification plays a vital role in electrifying unelectrified rural households. In India, more than 200 million people in rural areas do not have access to grid electricity. Over 80,000 villages remain to be un-electrified, as it is difficult to electrify them by grid electricity due to high capital cost, poor voltage regulation and low load factor [1]. Therefore the electrification of remote and non-electrified areas is a big challenge which requires cost effective approaches that can supply power to these areas.

The off-grid remote areas are mostly rich in renewable energy resources like hydro, solar, biomass, biogas, wind etc. Several researchers explained the techno economic viability of biogas plants in rural areas [2, 3]. Hybrid Energy System (HES) are found cost effective solutions to energize such areas and can remove the infeasibility related to a single energy source by taking advantages of all the available resources [4]. Due to the intermittent nature of most of the renewable energy sources, conditions may arise, when the demand exceeds the generation. The use of battery, as storage may improve the power quality and can store the excess energy required during the peak time. DG can be an another solution to such problem as it can meet the demand by manipulating the DG operation that can improve battery life and charge it if a lower set point is reached. The system size can also

be reduced by effectively selecting suitable combination of generators [5]. A proper tuning of DG and battery storage may also help to reduce the fuel consumption [6, 7].

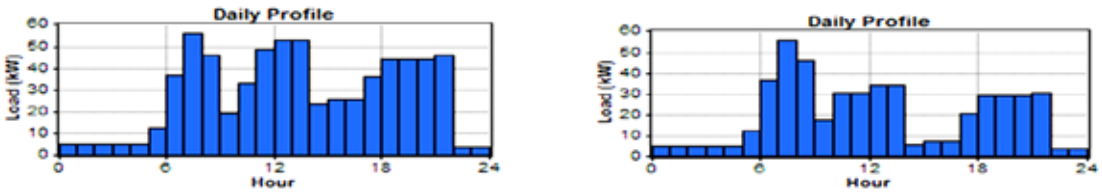
The present paper deals with the development of HES for five unelectrified villages in the Almora District of Uttarakhand, India. The area is rich in renewable resources such as solar, hydro, biomass, biogas etc. The paper covers the assessment of demand and potential of available renewable energy. Optimization of cost effective HES for the area has been carried out using HOMER [8-12]. Based on load following strategy, HOMER found the best combination of components for the development of HES in terms of NPC (Net Present Cost) and COE (Cost of Energy) for the study area.

II. PROFILE OF THE STUDY AREA

Uttarakhand (formerly Uttaranchal), a Northern State of India, has a total area of 53,484 km², of which 93% is mountainous and 65% is covered by forest [13]. There are 13 districts in Uttarakhand grouped into two divisions: Kumaon and Garhwal. Almora a district of Kumaun division is located at 29.62°N 79.67°E and consists of 11 blocks. The block consists of 227 villages with a population of 60,620. Out of 227 villages, 5 un-electrified villages named as: (1) Seli (2) Tapari (3) Sirani (4) Nailpar (5) Chimkholi, are chosen for the present study. These villages have 254 households and 11 hamlets with a population of 965.

III. LOAD ASSESSMENT

The energy demand was estimated by considering the household loads (light, TV, fan, radio), commercial load (light and fan for shops, flour mill), industry load (saw mill or paddy huller) and community load (post office, gram panchayat office, hospital, school, street light and water pumping). The total energy requirement of the area based on summer (April-September) and winter (October-March) seasons is 675.78kWh/day with peak load of 55.49 kW and 486.18kWh/day with peak load of 55.49 kW respectively. “Fig. 1” shows daily profile of load for summer and winter season respectively.



(a) summer season (b) winter season

Fig. 1: Daily Profile of Load of the Area

IV. RESOURCE ASSESSMENTS

In this area, solar, hydro and biomass are the major resources and wind as a minor. The estimation of potential of available renewable energy resources as well as the energy demand of the study area is carried out as follow:

4.1 Micro Hydro Power (MHP)

Micro Hydro Power (MHP) up to 100 kW is selected, as it plays an important role in meeting the energy needs of domestic, commercial, industrial and community through mechanical power generated by hydro turbines. Annual energy from hydro in kWh is determined by (1)

$$MHP = 9.81 \times Q \times \rho \times H \times 8760 \text{ (kWh / year)} \quad (1)$$

where Q is discharge of water, ρ is water density and H is required head.

Tapari is considered as one of the feasible site selected due to the presence of significant amount of hydro potential. For this site, the average discharge (Q) of 0.116 m^3/sec and head (H) of 22m is considered. The total annual potential is about 208MWh/yr. "Fig. 2" shows the hydro resource availability throughout the year with minimum stream flow of 97 L/s in the month of January and December and the maximum flow of 146 L/s in the month of July.

4.2 Solar Energy

Solar radiation data are taken from HOMER software for the study area having 29.34/ 34.09// N Latitude and 79.54/ 01.36// E Longitude. "Table 1" shows daily and monthly global solar radiations [14], from which it is clear that May has the maximum solar radiation of about 229kWh/m^2 whereas December has minimum of about 111kWh/m^2. Average solar radiation of the year is about 162kWh/m^2. Total solar energy potential of the area is found about 1948 kWh/m^2/year.

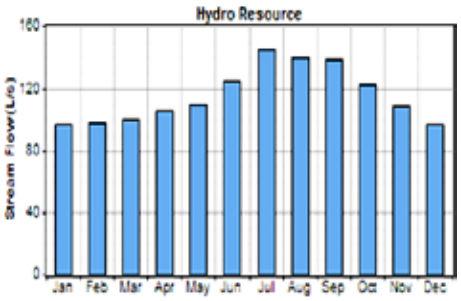


Fig. 2: Hydro Resource Availability

Table 1: Daily and Monthly Global Solar Radiation Data

Month	Clearness index	Daily Total Radiation (kWh/m^2)	Monthly Total Radiation (kWh/m^2)
January	0.662	3.966	122.95
February	0.651	4.694	131.43
March	0.662	5.827	180.64
April	0.669	6.848	205.44
May	0.665	7.38	228.78
June	0.586	6.684	200.52
July	0.463	5.201	161.23
August	0.471	4.952	153.51
September	0.566	5.242	157.26
October	0.7	5.364	166.28
November	0.687	4.292	128.76
December	0.641	3.587	111.19
Annual			1948

4.3 Biogas Energy

To assess the biogas potential, cows, buffalos, goat, horses and mules are considered. Based upon the survey, the total population of cattle from 5 villages is found as 1920. The total biogas potential was calculated on the basis of dung collection efficiency of 70%, biogas yield per kg of wet dung as 0.036 m^3/kg, calorific value of biogas as 4700 kcal/m^3, conversion factor of 860 [15], generator efficiency 95% and engine efficiency as 28%. The gas production is based on the production of biogas/kg cattle dung as 0.036m^3/kg while the energy available/day is calculated by the (2):

Energy available (kWh/day) = (Total Gas Yield (m^3)*4700*0.28*0.95)/860 (2)

The biogas production from the dung is evaluated based on the assumption that 10 kg/day dung will be available from cow/horse/mule, 15 kg/day from buffaloes and 1kg/day from goat. The available cattle dung from the study area is about 10481 kg/day. Therefore, the biogas availability in the study area is about 265m^3/day; from which about 385 kWh/day of energy can be produced. About 232m^3/day is proposed to be made available for cooking while the balance 47 kWh/day generated by using DG set for 8hrs/day can be converted for electricity. Biogas for cooking is based on gas requirement of 0.24m^3/person/day [16]. This comes out as 232m^3/day.

4.4 Biomass Energy

The biomass potential assessment is based on agriculture and forest waste available in the area. "Table 2" gives the total forest area of all the 5 villages with annual energy from biomass i.e. crop and forest practices. About 202.39 Ton/yr of biomass waste and 11.76 Ton/yr of foliage is available with a total of 214.15 Ton/yr equivalent to 157.59kWh/day.

For the above table, it is assumed that from the total foliage, only 60% is used for biomass and the electricity generated can be calculated by (3).

Total available energy for electricity (kWh/yr) = (Total fuelwood available (T/yr) × 1000 × CV_{BM} × η_{BM})/ (365×860×(operating-hrs/day))[17] (3)

Table 2: Village wise Forest Area and available Energy

Village name	Forest Area (ha)	Total Foliage available @(160 kg/ha/yr)	60% of foliage available for use as biomass (T/yr)	Total Available biomass (Crop + Forest) (T/yr)	Total available energy for electricity (kWh/day)
Nailpar	9.37	1499.2	0.9		
Seli	29.55	4728	2.84		
Tapari	9.35	1496	0.9		
Sirani	47.37	7579.2	4.55		
Chimkholi	26.83	4292.8	2.58		
Total	122.47	19595.2	11.76	214.15	157.59

From the above "Table 2", it is clear that crop and forest provide about 202 T/yr and 12T/yr biomass respectively. For calculating biomass available from forest, it is assumed that more than 160kg/ha/yr foliage is available from the forest [18]. Total available biomass from crop and forest, is about 214 T/yr. To calculate total energy available for electricity, the calorific value (CV_{BM}) is considered as 1100, conversion efficiency (η_{BM}) as 21% and operating hours/day as 10 hrs. So the total electricity generated is about 158kWh/day.

V. CONFIGURATION OF THE PROPOSED HYBRID ENERGY SYSTEM COMPONENTS

The major components of hybrid energy system are SPV, MHP, biogas generator, gasifier based diesel generator, batteries and converters. For economic analysis, capital costs, replacement and O&M costs of each unit is defined in HOMER software in order to simulate the system. "Table 3" shows different economic parameters of system components used for the development of HES.

The sizes of SPV module are considered as 0, 5, 10, 15, 20 and 30 kW. Life of 20 years and derating factor of 90% are considered with no tracking system. For micro hydro turbine, head of 22m and design flow of 100 lps, turbine efficiency as 95% and life 25 years, are considered. Size of biogas generator is considered as 5 kW and gasifier as 15 kW. Operating hours for biogas generator is taken as 15000 hrs and minimum load ratio as 30%. Sizes of diesel generator are considered as 0, 5, 10, 15, 20, 25, 30, 40 and 50kW. Surrette 6CS25P battery is considered whose manufacturer is Rolls/Surrette.

VI. RESULT AND DISCUSSION

The HES given by HOMER is shown in "Fig. 3". "Table 4" shows the optimized results of hybrid energy system. It is found that several configurations are possible on the basis of minimum net present cost (N.P.C.)

and cost of energy (C.O.E.).Result shows that the total cost of first configuration i.e. MHP-Diesel-Biogas-Gasifier comes out as 210,779 $ with COE of 0.078$/kWh, renewable fraction as 78% and emissions as 263,472 kg/yr (carbon dioxide) whereas in second configuration i.e. PV-MHP-Diesel-Biogas-Gasifier, NPC is 215,181 $ with COE 0.079 $/kWh, renewable fraction as 81% and emissions as 247,787 kg/yr (carbon dioxide). This shows that both the configurations have almost same COE but second configuration has greater renewable fraction and less carbon emissions. So second configuration is considered as the best configuration having system specifications as 5 kW SPV, 20.5 kW MHP, 5 kW diesel generator, 5 kW biogas generator, 15 kW gasifier and 20 storage batteries in addition to 10 kW capacity converter.

Table3: Economic Analysis of System Components

S. No.	Components	Capital Cost	Replacement Cost	O & M Cost
1	Solar Photovoltaic (per kW)	6000 $	5000 $	10 $/yr
2	Micro Hydro Turbine (per kW)	1400 $	1200 $	135 $/yr
3	Biogas Generator (per kW)	650 $	600 $	0.025 $/hr
4	Gasifier (per kW)	215 $	210 $	0.05 $/hr
5	Diesel Generator (per kW)	1000 $	900 $	0.02 $/hr
6	Battery	1000 $	800 $	30 $/yr
7	Converter	700 $	550 $	100 /yr

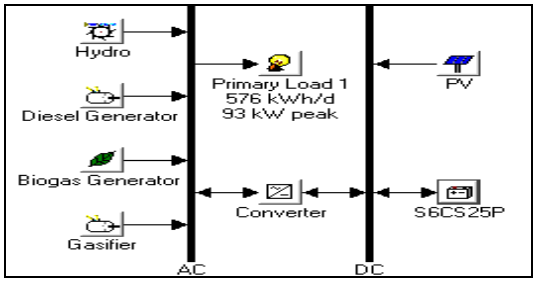


Fig 3: complete hybrid energy system

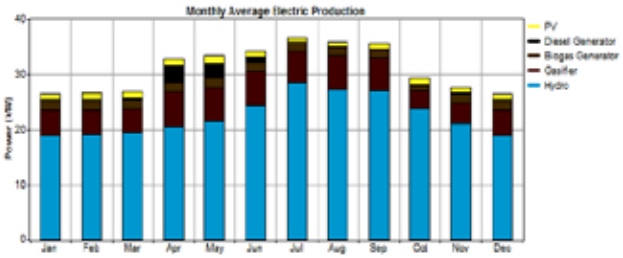


Fig. 4: electricity production by different components of HES

Table 4: Results of Optimization of Hybrid Energy System for Study Area

PV (kW)	Hydro (kW)	Diese (kW)	Bio (kW)	Gasi (kW)	S6CS25P	Conv. (kW)	Initial Capital	Operating Cost ($/yr)	Total NPC	COE ($/kWh)	Ren. Frac.	Diesel (L)	roducer Ga (kg)	Biomass (t)	Diese (hrs)	Bio (hrs)	Gasi (hrs)
	20.5	10	5	15	20	5	$ 52,340	12,394	$ 210,779	0.078	0.78	4,577	172,703	386	1,975	2,920	3,650
5	20.5	5	5	15	20	10	$ 80,840	10,509	$ 215,181	0.079	0.81	2,259	166,122	381	1,993	2,920	3,650
	20.5	15	5	15			$ 33,840	15,166	$ 227,716	0.084	0.78	8,012	153,282	381	2,615	2,920	3,650
5	20.5	15	5	15		5	$ 67,340	14,784	$ 256,334	0.095	0.80	6,939	145,456	367	2,405	2,920	3,650
10	20.5		5	15	40	20	$ 132,840	10,502	$ 267,093	0.099	0.84		159,200	367		2,920	3,650
30		25	5	15	40	20	$ 276,440	53,654	$ 962,322	0.355	0.32	35,142	198,949	398	4,911	2,920	3,650
		30	5	15	40	10	$ 94,440	70,452	$ 995,049	0.367	0.06	52,495	203,790	398	5,622	2,920	3,650
		40	5	15			$ 57,440	97,361	$ 1,302,035	0.480	0.05	69,684	196,264	398	8,760	2,920	3,650
5		40	5	15		5	$ 90,940	96,675	$ 1,326,769	0.489	0.10	68,007	192,184	398	8,760	2,920	3,650

From “Fig. 4” it is observed that the share of electricity from SPV is 9,899 kWh/yr (4%), 197,930 kWh/yr from MHP (73%), 5,846kWh/yr from diesel generator (2%), 13,992kWh/yr from biogas generator (5%) and 44,625kWh/yr from gasifier(16% of the total). Monthly average electricity production from different resources is shown in “Fig. 4”. Minimum average production months are December, January, February and March with 26 kW and maximum average production month is July with 37 kW.

The paper signifies the involvement of various available energy resources and their role in the development of HES for a remote area. An optimum HES consisting of 5 kW SPV, 20.5 kW hydro turbines, 5 kW biogas generators, 15 kW biomass gasifier, 5 kW diesel generators and 10 kW of converter with 20 storage batteries, has been taken for electrification of 5 villages. Optimization and simulation has been done using HOMER software. The results indicate that the proposed HES offer the most economically feasible solution for the study area. The COE of the optimal HES comes around 0.079$/kWh with NPC 215,181$ as minimum and the renewable energy fraction accounts for about 81% of the total generation with carbon emissions of 247,787kg/yr which is found to be the most economical solution.

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SELECTIVE CATALYTIC REDUCTION OF NO_X FROM AUTOMOBILE EXHAUST IN THE ABSENCE OF REDUCTANT ON NON-NOBLE METAL OXIDE CATALYST

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ABSTRACT

The present investigation employ's for the first time, a novel catalytic system involving sintered calcium phosphate as the carrier for selective catalytic reduction of NO_x from the automobile exhaust emissions without involving ammonia as a reductant. Initially, ceramic beads were coated with the slurry of calcium phosphate, dried and sintered (labeled as SCaP). The copper oxide was deposited by direct reduction and then calcined to 400^oC. The samples were characterized using XRD, SEM and UV - DRS. The efficiency of the catalyst in controlling NO_x content was tested using plug flow reactor, connected to the automobile exhaust stream of the 4-stroke engine through a flow controller. The reduction in the NO_x content was analyzed at different flow-rates and at different temperatures.

Keywords: Copper catalyst, NO_x reduction, SCaP support, Selective Catalytic Reduction.

I. INTRODUCTION

Growing urbanization, life style changes, increase in volume and number of movement of goods etc., have led to the spurt in vehicle population, which is expected to grow close to 1.3 billion by 2030 [1]. Vehicular exhausts, in general, are of great environment threat, as they are the major contributor of air pollution. The gaseous phase of these emissions constitutes mainly carbon monoxide (CO), unburnt hydrocarbons (HC) and nitrogen oxides (NO_x) [2]. The percentage of CO and HC emitted from diesel and gasoline engines can be controlled by using Pt or Pd as the catalyst. But the reduction of NO_x under lean environment in the case of diesel engine is the greatest challenge [3]. In order to meet this, selective catalytic reduction (SCR) technology is designed, which injects a liquid reductant (generally, automotive grade urea) into the chamber containing a SCR catalyst (Cu/ZSM-5) [4]. The urea undergoes decomposition and hydrolysis releasing ammonia which rapidly reacts with NO_x from the exhaust stream in presence of catalyst and converts it into N_2 and water. Eventhough, the NO_x reductions upto 90% is achieved by the above technology, it exhibits a few practical limitations such as exhaust temperature of 200°C is required for complete decomposition and hydrolysis of urea and having a freezing temperature of -11°C is not acceptable for cold climate . The optimum dosage of urea is required for complete reduction of NO_x, otherwise it would lead to slippage of ammonia which sometimes forms ammonium nitrate below 200°C [5].

To overcome the above demerits, the present investigation involves preparing a copper based catalyst using a non-conventional support, viz., sintered calcium phosphate (SCaP) that would reduce the amount of NO_x without involving reductants. The conventional supports that are generally used for deposition of metal oxides includes zirconia, chromia, alumina, silica, titania, magnesia, etc.

For the first time, SCaP was used as the carrier for depositing fine particles of CuO by DRC method [6]. The expected advantage of using SCaP as the support is its good thermal stability and large surface area. This terminal $–PO^-$ groups are responsible for fixing the active species on the support.

II. EXPERIMENTAL WORK

Initially the ceramic beads (cordierite) of 4 mm diameter were subjected to washings with distilled water and 20% nitric acid solution in order to remove the impurities and enhance the adherence of the wash coat material (SCaP). The slurry of calcium phosphate, prepared by mixing calculated quantities of calcium carbonate and phosphoric acid was coated on the ceramic beads. The coated beads were dried at 120°C for 12h and sintered to 650°C for 90 min. The SCaP coated ceramic beads were labeled as SCaP– CER.

SCaP-CER was introduced into the beaker containing copper nitrate solution and agitated well. Ammonia was added in drops followed by addition of hydrazine hydrate. The contents were dried at 110°C for 4 h and calcined at 400°C for 90 min. The final catalyst is labeled as Cu/SCaP-CER.

The samples were characterized using XRD, SEM and UV-DRS techniques. Powder XRD pattern was recorded on a Rigaku SMART Lab-9kW, equipped using Cu-K_β target and scan speed of 4°/min in the 2θ range of 20 – 70°. SEM images of Cu/SCaP-CER was recorded using FESEM – Carl Zeiss, SUPRA-55. UV spectrum in diffuse reflectance mode was recorded using Perkin Elmer spectrometer.

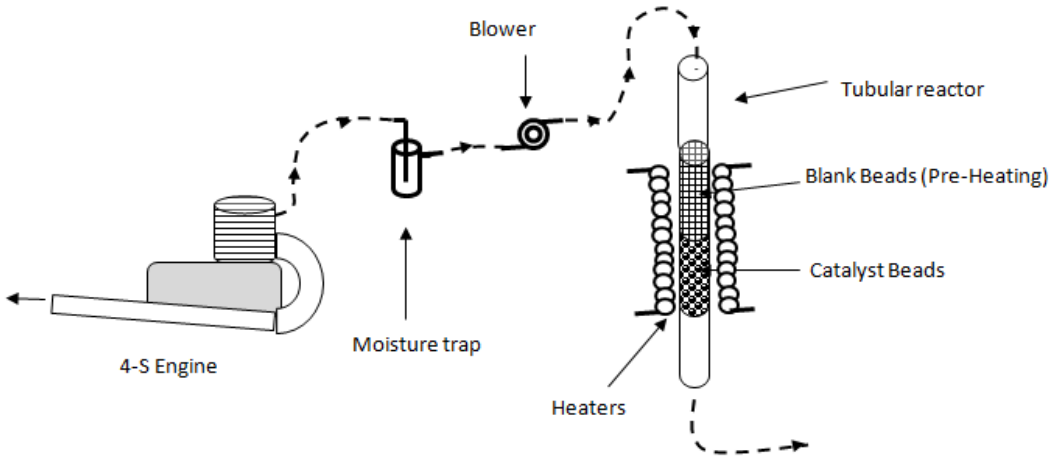


Fig.1: Schematic representation of reactor set-up

The catalytic efficiency of the catalyst was studied in a tubular flow reactor fitted with heater, controlled by thermocouple fixed at catalyst bed. The reactor is made up of SS310 grade steel tube of 3 cm diameter and 3.5 feet length fixed with perforated disc at the centre inside the reactor to hold the catalyst beads.

A part of exhaust gas from the 4-stroke engine was passed on to the reactor through a moisture trap and a speed controlled blower through which the space time can be altered (Fig.1). The exhaust gas was monitored for

carbon monoxide (CO), nitrogen oxides (NO_x) and hydrocarbons (HC) using Technovation fuel efficiency monitor (PFM-33, Prima Equipment, Vadodara).

The engine was maintained at idling condition throughout the study. For studying the influence of space-time on the reaction, the gas flow-rates were adjusted to 1.2, 1.75, 2.5 & 3 LPM through the reactor. Initially, a blank run (without catalyst) was carried out and the values of CO, HC & NO_x were recorded at different flow-rates. 100 mL of the catalyst beads (weighing about 100 grams) was loaded in the reactor by gently tapping the sides and 100 mL of blank ceramic beads (without catalyst) was introduced above the catalyst bed as pre-heating zone. The exhaust gas was then passed on to the tubular reactor for 15 minutes to reach steady-state and the values of CO, HC and NO_x were recorded. While studying the influence of different parameters, the reactor was flushed with air for 2 minutes between each variation to confirm absence of occluded gases from the earlier runs, if any.

III. RESULTS & DISCUSSION

The XRD patterns of the support SCaP sintered at 650^{o}C and Cu/SCaP-CER (1% CuO) are represented in Fig.2. An extra peak in the catalyst at 2θ = 35.5, confirms the presence of copper species as CuO (PDF No.65-2309) [7].

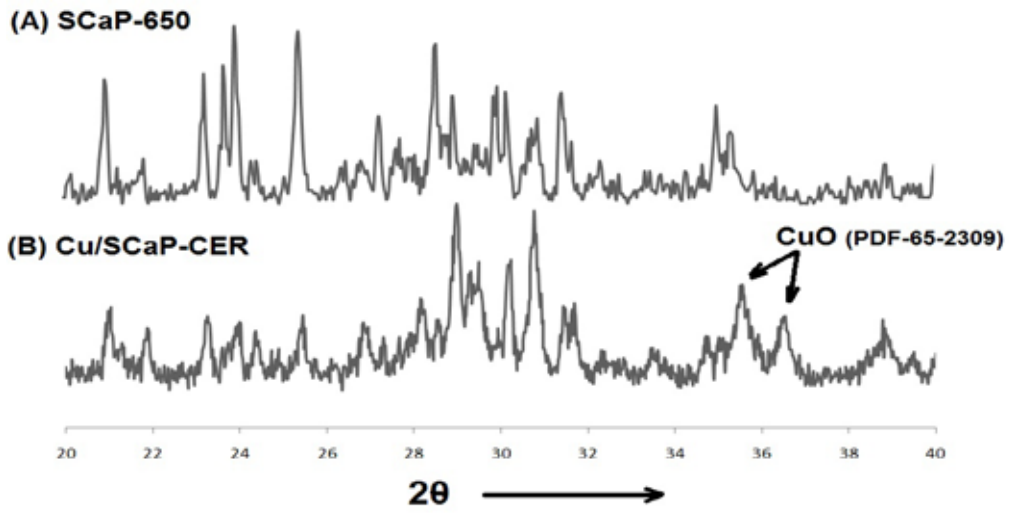


Fig.2: XRD pattern of (A) SCaP-650 (support) and (B) Cu/SCaP-CER (catalyst)

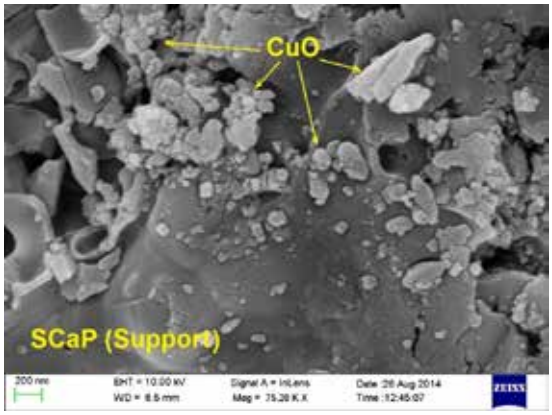


Fig. 3: SEM image of Cu/SCaP-CER (1% CuO)

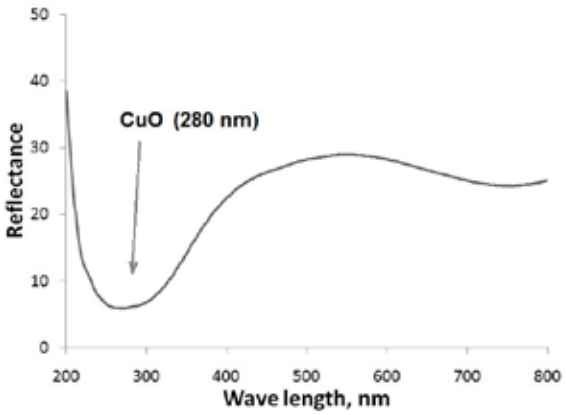
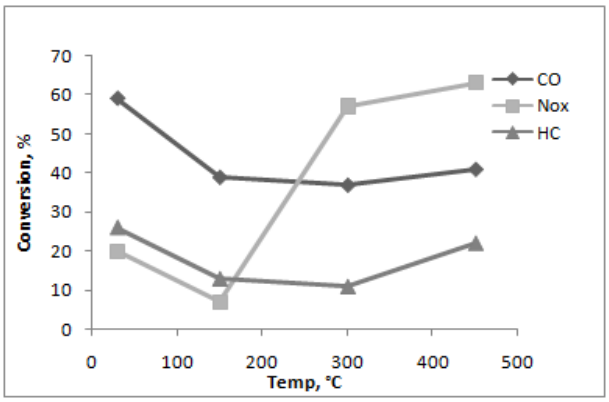


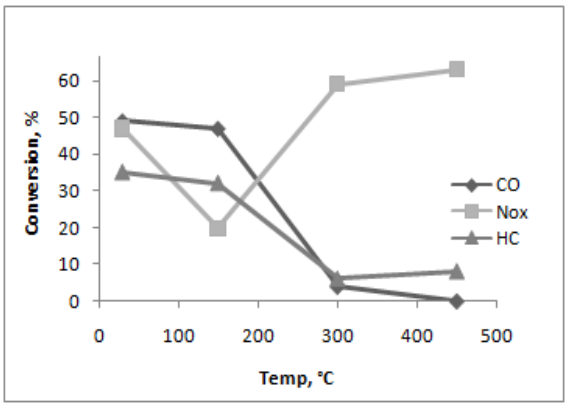
Fig. 4: UV-DRS of Cu/SCaP-CER (1% CuO)

SEM image of Cu/SCaP-CER (1% CuO) catalyst showed the average particle size in the range of 60 to 90 nm (Fig. 3). The UV-DRS spectra of the catalyst shows a band at 280 to 300 nm thereby further confirming the presence of CuO, thus supporting XRD observation (Fig. 4) [8].

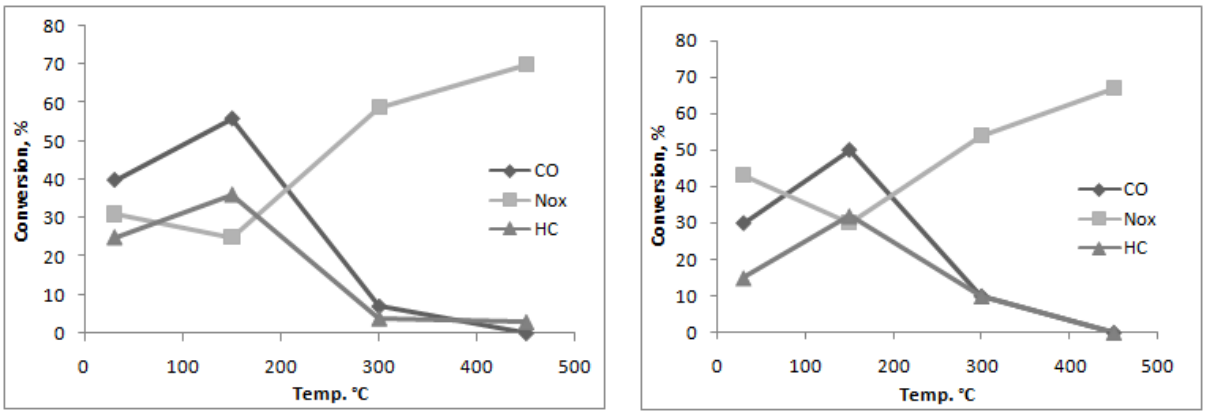
The efficiency of the catalyst in controlling the automobile exhaust gas pollutants was studied by passing the gas through the reactor with different flow-rates at different temperatures. Initially, the reactor was maintained at room temperature (30°C) and the exhaust gas was passed at the rate of 1.2 LPM. After passing for 15 minutes, the composition of the exhaust gas from the reactor was measured. The values were compared with that of blank-run at corresponding flow-rate (1.2 LPM) and conversion of CO, HC and NO_x were calculated. Similarly, the experiments at flow-rates of 1.75, 2.5 and 3 LPM were carried out. While studying the influence of temperature on the reaction, the catalyst bed was heated to 150°C and maintained for 15 minutes in the flow of air. Then exhaust gas at 1.2 LPM was passed for 15 minutes and analyzed for CO, HC and NO_x. Similarly, experiments were repeated for different flow-rates at 300° and 450°C.



(A) Flow-rate: 1.2 LPM



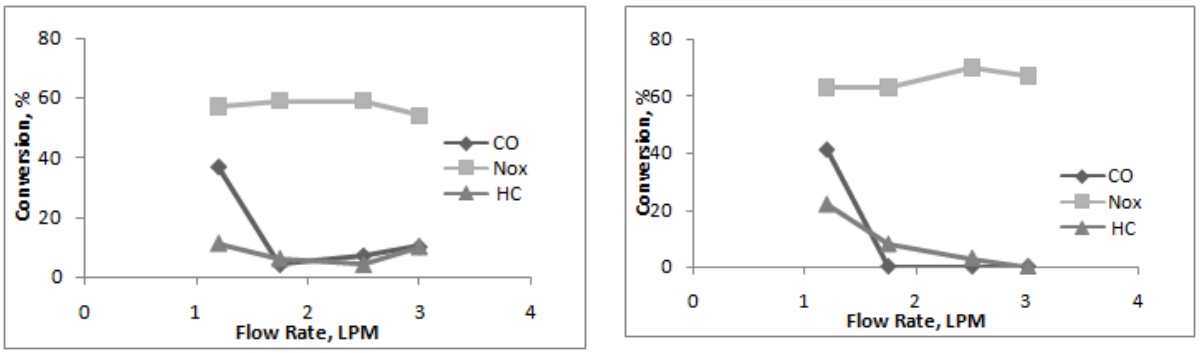
(B) Flow-rate: 1.75 LPM



(C) Flow-rate: 2.5 LPM **(D) Flow-rate: 3 LPM**

Fig.5: Conversion of CO, HC & NO_x over Cu/SCaP-CER Catalyst: Influence of Temperature

The influence of temperature on conversion of CO, HC & NO_x was recorded at different flow-rates and the conversion graphs are presented in the Fig.5. Conversion of CO & HC was found to be nearly constant at lower flow rate (Fig.5A). Increase in temperature decreases the conversion of CO & HC at higher flow-rates (Fig.5B-5D). The conversion of NO_x increases with temperature at all flow-rates (Fig.5A–5D).



(A) Temperature - 300°C **(B) Temperature - 450°C**

Fig.6: Conversion of CO, HC & NO_x over Cu/SCaP-CER Catalyst: Influence of Flow-rate

The influence of flow-rate on conversion of CO, HC and NO_x at different temperatures are presented in Fig.6A & 6B. It was observed that conversion of NO_x remains constant above 300°C irrespective of flow-rate. Surprisingly, the conversion of CO & HC came down to zero at higher flow rates.

It can be concluded from the above results that CO & HC in the exhaust stream does not influence the conversion of NO_x and hence, reduction of NO_x follows first order kinetics.

Table 1: Conversion of NO_x with temperature at different flow-rates.

S.N.	Flow rate, LPM	Space-time (τ), min	Temperature, °C	NO_x Conv.%	Rate Constant (k), min^{-1}	Activation Energy for NO_x, kJ mol^{-1}
1.	1.2	0.0833	30	20	2.68	22.2
2.			150	7	0.87	

3.			300	57	10.13	
4.			450	63	11.98	
5.	1.75	0.057	30	47	11.11	13.3
6.			150	20	3.90	
7.			300	59	15.6	
8.			450	63	17.4	
9.	2.5	0.04	30	31	9.28	12.4
10.			150	25	7.19	
11.			300	59	22.29	
12.			450	70	30.1	
13.	3	0.033	30	43	16.86	9.7
14.			150	30	10.7	
15.			300	54	23.3	
16.			450	67	33.25	

For first order kinetics, the rate of the reaction is given as:

$$-r_A = kC_A$$

for PFR the rate constant is related to concentration and space-time as follows:

$$\tau = C_{Ao} \int_0^{Xa} dX_A / k_{CA}$$

where τ is the space time, C_{Ao} is the initial concentration and X_A is the conversion of NO_x.

$$\text{and } C_A = C_{Ao}(1-X_A)$$

Assuming there is no change in density of gas during the course of reaction after reaching steady state, the rate constant at different temperatures and flow rates were calculated and given in the Table 1.

Arrhenius plot of ln(k) Vs 1/T gives a straight line (Fig.7) and the activation energy for the catalyst at different flow rates were calculated and given in the Table 1. The activation energy increases with increase in space time. For tubular reactor, such an observation was made by Yashimoto *et.al.*[9].

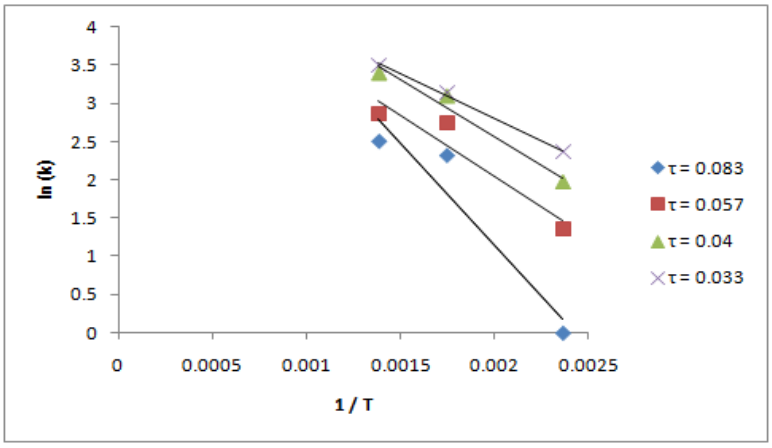


Fig.7: Arrhenius Plot

IV. CONCLUSIONS

A new catalytic system has been developed by depositing fine particles of CuO over non-conventional support, viz., sintered calcium phosphate. The phase purity has been confirmed by XRD, presence of CuO was confirmed by XRD, UV-DRS and particle size by FE-SEM analysis. The catalyst showed 30% reduction of NO_x at room temperature which increased to 70% at 300°C. Conversion of CO & HC was found to be 40 - 60% at lower flow-rate which reduced to zero at higher flow rates. Thus the present catalytic system was found to be efficient in reduction of NO_x.

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POWER REDUCTION IN CONTENT ADDRESSABLE MEMORY

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ABSTRACT

Content Addressable Memory (CAM) is a special type of memory which is very helpful in search engines and are much faster. CAM structure composed of conventional semiconductor memory SRAM with some additional circuitry for compare operation. CAM does the operation of returning the address location for a search word in a single clock cycle. CAM performs three types of operations namely READ, WRITE and COMPARE operation. CAM rarely does the READ and WRITE operation and in major scenarios CAM is used for comparing the Search word with the existing database and returning the corresponding address location within a single clock cycle. CAM compares the data word in parallel for each bit and hence consumes higher power. In order to reduce power, the conventional CAM is modified to perform with extra additional count bit as an index bit for each data word. In that way, the time and power consumption can be reduced. In this project, a parity bit based comparison is proposed in contradiction to existing count bit comparison to reduce power. This reduces power to a promising manner.

Keywords: CAM, Associative Memories, Low Power, Parity Bit, Low Power ML, Memory Lookup Table

I. INTRODUCTION

Modern digital systems require the capability of storing and retrieving large amounts of information at high speeds. Memories are circuits or systems that store digitalinformation in large quantity. Semiconductor memory is an electronic data storage device which often used as computer memory implemented on a semiconductor based integrated circuits. Semiconductor memory has the property of random access, which means that it takes the same amount of time to access any memory location, so data can be efficiently accessed in any random order. A memory, which in one word time finds a matching segment and reads the remainder of the word, has been called by one of these names as Content-Addressed Memory (CAM) Data Addressed Memory (DAM), Content Associative Memory (CAM).

II. MEMORY ORGANIZATION

One of the most important fundamental features of any computing system is the ability to store data to memory, recall the data, and overwrite the data. In a semiconductor memory chip, each bit of binary data is stored in a tiny circuit called a “Memory cell” consisting of one to several transistors. The memory cells are laid out in rectangular arrays on the surface of the chip. The 1-bit memory cells are grouped in small units called “words” which are

accessed together as a single memory address. Memory is manufactured in word length that is usually a power of two, typically N=1, 2, 4 or 8 bits. Data is accessed by means of a binary number called a memory address applied to the chip's address pins, which specifies which word in the chip is to be accessed. If the memory address consists of M bits, the number of addresses on the chip is 2M, each containing an N bit word. Consequently, the amount of data stored in each chip is N2M bits. The data capacity is usually a power of two: 2, 4, 8, 16, 32, 64, 128, 256 and 512 and measured in KB-bits, MB-bits, GB-bits or TB-bits, etc. Currently the largest semiconductor memory chips hold a few GB of data, but higher capacity memory is constantly being developed.

Semiconductor memories are broadly classified into three categories which are shown in below table.

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Table 2.1 Memory Classification

Read Write Memories are classified into two categories as

1. Random Access Memories
2. Non – Random Access Memories.

Random-access memory (RAM) is a generic term that refers to both SRAM and DRAM or, indeed, any type of memory where you can arbitrarily (randomly) access stored data. Non- Random Access Memories are also termed as “Serial Access Memories”. These are type of memory in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device that is related to the serial-access port and its associated functions.

Content Addressable Memory is one such Serial Access Memories which access the data in a sequence and the storage device moves through all information up to the point it is attempting to read or write. These are type of memory which is used for Permanent storage unlike the Random access memories which are used as the temporary Storage.

III. CONTENT ADDRESSABLE MEMORY

Content Addressable Memories (CAMs) are hardware search engines that are much faster than algorithmic approaches for search intensive applications. CAMs are composed of conventional Semiconductor memory especially SRAM with added comparison circuitry that enable a search operation to complete in a single clock cycle. CAM operates in three modes

- READ
- WRITE
- COMPARE

3.1 CAM Architecture

A small model is shown in below figure shows CAM consisting of 4 words, with each word containing 3 bits arranged horizontally (corresponding to 3 C cells). There is a match -line corresponding to each word (ML0, ML1, etc.) feeding into match line sense amplifiers (MLSAs), and there is a differential search line pair corresponding to each bit of the search word (SL0, SL$\overline{0}$, SL1, SL$\overline{1}$, etc.). CAM search operation begins with loading the search-data word into the search-data registers followed by pre-charging all match lines high, putting them all temporarily in the match state. Next, the search line drivers broadcast the search word onto the differential search lines, and each CAM core cell compares its stored bit against the bit on its corresponding search lines. Match lines on which all bits match remain in the pre-charged-high state. Match lines that have at least one bit that misses, discharge to ground. The MLSA then detects whether its match line has a matching condition or miss condition. Finally, the encoder maps the match line of the matching location to its encoded address.

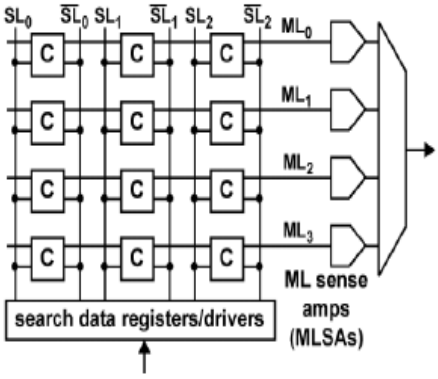

Fig 3.1 CAM Architecture

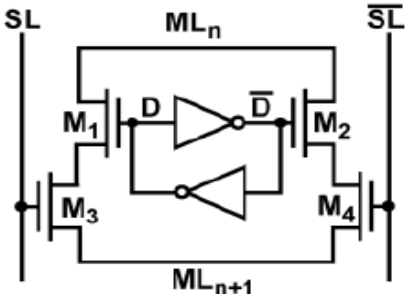

Fig 3.2 10T - NOR based CAM CORE CELL

3.2 Challenges in CAM Design

Full parallel search operation leads to critical challenges in designing a low-power system for high-speed high-capacity CAMs:

- Power hungry nature due to the high switching activity of SL and the ML.
- A huge surge-on current (i.e., peak current) occurs at the beginning of the search operation due to the concurrent evaluation of the ML may cause a serious IR drop on the power grid, thus affecting the operational reliability of the chip.

As a result, numerous efforts have been put forth to reduce both the peak and the total dynamic power consumption of the CAMs.

3.3 Advantages of CAM

Major advantage that CAM offers are high speed functionality. Other advantages are

- Data Storage and retrieval capabilities.
- Programming simplification based upon the possibility of ignoring the placement of data in memory and extensive use of content addressing and ordered retrieval.
- Periodicity of structure lends itself to integrated circuit techniques and batch fabrication. Inter connections between components become shorter and less tangled, reducing propagation delays and simplifying layout and checkout. Since the structure is periodic, it can be easily expanded in size
- The periodic structure may permit an organization which is tolerant of memory or circuit element failures. If a cell fails, it may be possible to avoid its further use with little loss to the system capability.

3.4 Count Bit Based CAM

In general, a CAM has three operation modes: READ, WRITE, and COMPARE, among which “COMPARE” is the main operation as CAM rarely reads or writes. It starts a compare operation by loading an n-bit input search word into the search data register. The search data are then broadcast into the memory banks through n pairs of complementary search-lines SL and ~SLs directly compared with every bit of the stored words using comparison circuits. Each stored word has a ML that is shared between its bits to convey the comparison result. Location of the matched word will be identified by an output encoder, as shown in Figure 1. During a pre-charge stage, the MLs are held at ground voltage level while both SL and ~SLs are at VDD. During evaluation stage, complementary search data is broadcast to the SL and ~SL. When mismatch occurs in any CAM cell (for example at the first cell of the row D= “1”; ~D=“0”; SL =“1”; ~SL=“0”), transistor P3 and P4 will be turned on, charging up the ML to a higher voltage level. A sense amplifier (MLSA) is used to detect the voltage change on the ML and amplifies it to a full CMOS voltage output. If mismatch happens to none of the cells on a row, no charge up path will be formed and the voltage on the ML will remain unchanged, indicating a match.

Since all available words in the CAMs are compared in parallel, result can be obtained in a single clock cycle. Hence, CAMs are faster than other hardware- and software-based search systems. They are therefore preferred in high-throughput applications such as network routers and data compressors. However, the full parallel search operation leads to critical challenges in designing a low-power system for high-speed high-capacity CAMs. The power hungry nature due to the high switching activity of the ML and the SL and a huge surge-on current (i.e., peak current) occurs at the beginning of the search operation due to the concurrent evaluation of the SL may cause a serious IR drop on the

power grid, thus affecting the operational reliability of the chip. As a result, numerous efforts have been put forth to reduce both the peak and the total dynamic power consumption of the CAMs.

3.4.1 Pre Computation Scheme Design

The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison. These extra bits are derived from the data bits and are used as the first comparison stage. For example, in below figure number of "1" in the stored words are counted and kept in the Counting bits segment. When a search operation starts, number of "1"s in the search word is counted and stored to the segment on the left of figure. These extra information are compared first and only those that have the same number of "1"s (e.g., the second and the fourth) are turned on in the second sensing stage for further comparison. This scheme reduces a significant amount of power required for data comparison, statistically. The main design idea is to use additional silicon area and search delay to reduce energy consumption. The previously mentioned pre-computation and all other existing designs shares one similar property. The ML sense amplifier essentially has to distinguish between the matched ML and the 1-mismatch ML. This makes CAM designs sooner or later face challenges since the driving strength of the single turned-on path is getting weaker after each process generation while the leakage is getting stronger. This problem is usually referred to as Ion/Ioff.

IV. PROPOSED METHOD

A versatile auxiliary bit is introduced to boost the search speed of the CAM at the cost of less than 1% area overhead and power consumption. This newly introduced auxiliary bit at a glance is similar to the existing Pre-computation schemes but in fact has a different operating principle.

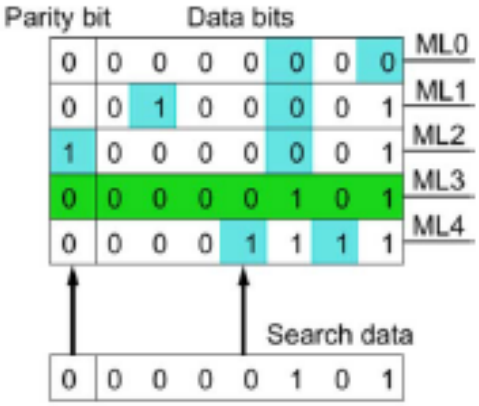

Fig 4.1 a) Conceptual View of Pre-computation based CAM design **b) Conceptual View of Parity based CAM design**

The parity bit based CAM design is shown in above figure consisting of the original data segment and an extra one-bit segment, derived from the actual data bits. Technique is to obtain only the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word and ML. Thus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage

as in conventional CAM. Hence, the use of this parity bits does not improve the power performance. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below.

In the case of a matched in the data segment (e.g., ML3), the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment (e.g.,ML2), numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment (e.g., ML0, ML1 or ML4), the parity bits are the same and overall it has two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only have to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed designgreatly improves the search speed and the I_{on}/I_{off}ratio of the design**.**

Table 4.1 Memory Lookup Table for Parity based design

Parity Bit	Data
0	1111
1	0010
0	0011
0	0000
0	0101
0	0110
1	0111
1	1000
0	1001
0	1010
1	1011
0	1110

V. SIMULATED RESULTS

The Memory circuits are developed through Verilog HDL using XILINX ISE Simulator (Version 9.2i). Read, Write and Compare operations for both the techniques are simulated along with their power analysis. Power analysis is carried out using XILINX Power analyzer tool.

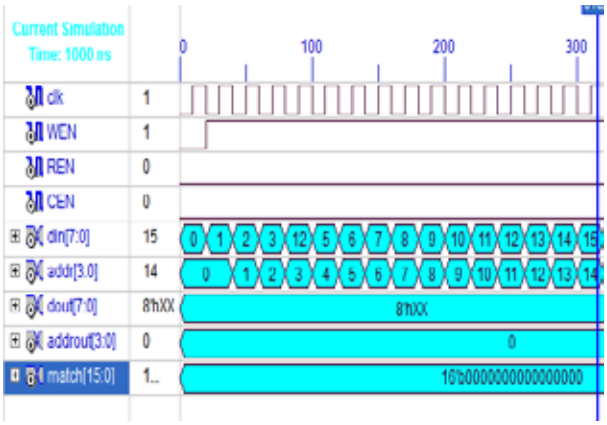

Fig. 5.1 Write Operation of CAM

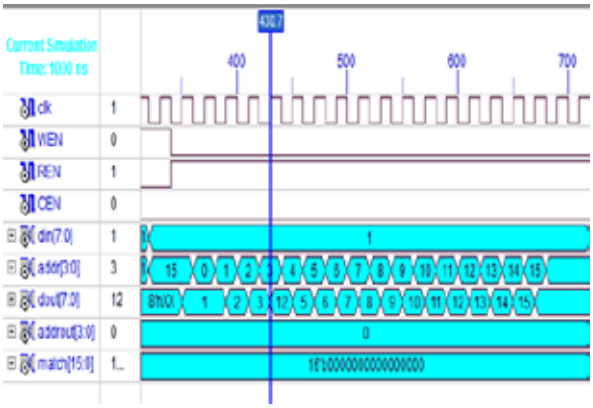

Fig 5.2 Read Operation of CAM

Table 5.1 Memory Look-up Table

Count Bit	Address	Data
1	0000	0001
1	0001	0010
2	0010	0011
1	0011	0100
2	0100	0101
2	0101	0110
3	0110	0111
1	0111	1000
2	1000	1001
2	1001	1010
3	1010	1011
2	1011	1100

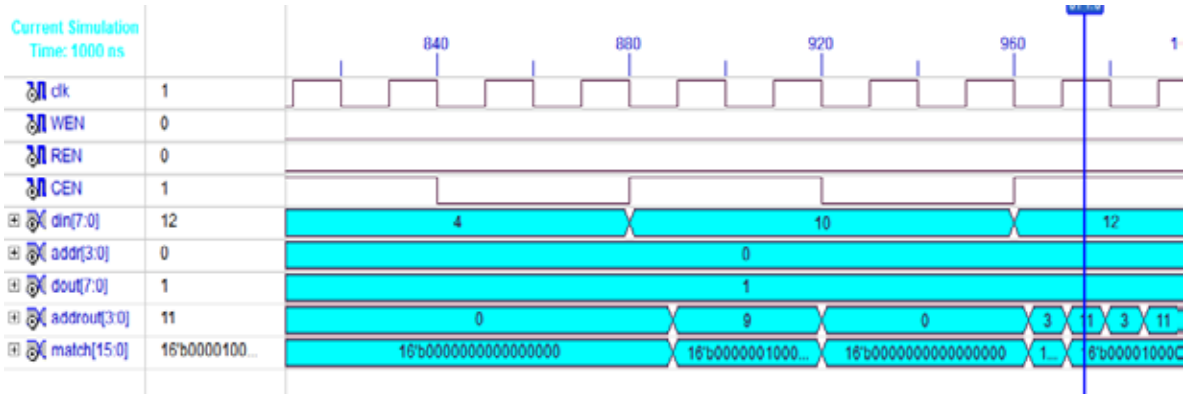

Fig 5.3 Compare Operation of CAM

CAM circuits are developed for both read, write and compare operation for both pre computation based and parity based design techniques. From Results we analyzed that Parity based CAM circuits consume less power when compared to the count bit based pre computation CAM. Also the search speed is also better in the parity based CAM design.From the above power comparison table, it is clear that Content Addressable Memory logic implemented based on Parity bit logic consumes lesser power when compared to the Content Addressable Memory logic implemented with the conventional pre-computation based design of logic implementation using Count bit method.

Table 5.2Power Consumption in Count and parity based technique.

Power Analysis	**RESULTS**	
	COUNT BASED CAM	PARITY BASED CAM
Total Power Consumption	95mw	91mw

VI. CONCLUSION

Reliability of a product describes the ability of a system or component to perform its required functions under stated conditions for a specified period of time. Quality of product is decided based on reliability of the chip. For an Integrated Circuit (IC), as a critical product specification under today's aggressive technology scaling, reliability has always been very difficult and costly to measure, and to achieve in leading-edge technology. In this paper, a novel low-power and highly reliable Content Addressable Memory logic has been proposed to increase the search speed and reduce the power consumption during compare operation. Thus two various techniques are developed to identify the reduction in power consumption. CAM consumes higher power during compare cycle and hence necessary measures are taken to reduce the power in compare cycle. Basically the existing conventional CAM follows the

approach of pre-computation method of adding an extra count bit which stores the number of count based comparison and hence the new technique proposed is based on the parity bit based comparison which helps in power reduction. Both these techniques are developed and simulated to analyze the power consumption and simulated results shows that Parity based CAM boost the search speed with reduced power consumption.

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BIOGRAPHICAL NOTES

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THE STUDY OF DYNAMIC BEHAVIOUR OF INTERLINKED POWER SYSTEM USING SIMULINK

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ABSTRACT

Practically all power system is interconnected in nature. In multi area interlinked power system the variation in load is a big obstacle .The basic intent of automatic load frequency control is to maintain total generation of system with total system requirement so that the frequency and the real power exchange with associated system are unaffected. Any dissembling between generated power and the consumed power results variation in system frequency scheduled frequency. The variation in frequency causes the system collapse, so in order to avoid such a problem we have to control the frequency variation in interlinked power system. This paper presents different Simulink results which shows the dynamic behavior of multi area interrelated power system with different conventional controller with 1% step load change, and it is found that these results are improved with the help of optimal control technique i.e. LQR method.

***Keywords*: Automatic generation control, tie line power, optimal controller, Area control error etc.**

I INTRODUCTION

In previous years, largemodification have been done into the power system across the world. For the efficient and feasible operation of interlinked power system, itis required to maintain the total generation with the total demand along with system losses. Generally in present days all power systems are interconnected with their neighboring areas. In an interlinked power system the load is changes continuously so corresponding real power also changes which ultimately effect the system frequency. In orderto maintain the system frequency and real power demand the generator input must be regulated accordingly. In a large interlinked power system manual regulation of generator input is very difficult, so for this purpose there are various automatic controlling devices are used to control the generator input. These devices are basically the controllers which reduces the difference between total generation and total demand. The mismatch between total generation and total demand causes system frequency change from its schedule value, which ultimately resulting the system collapse [1-2]. Now in this paper the dynamic response of isolated power system, two area power system as well as three area power system are analyzed with PI and PID controller, these responses are improved by the use of optimal control mechanism(by LQR) [3-8]. The utilization of the advance optimal control mechanism (LQR) on power system shows that an optimal controller can provide better system response[9-14]. This paper ends with the simulation results of these controllers which shows that the dynamic behavior of power system is improved with the help of optimal control scheme in comparison to PI, PID controller[15].

II MODELLING OF POWER SYSTEM

2.1 An isolated power system with ALFC

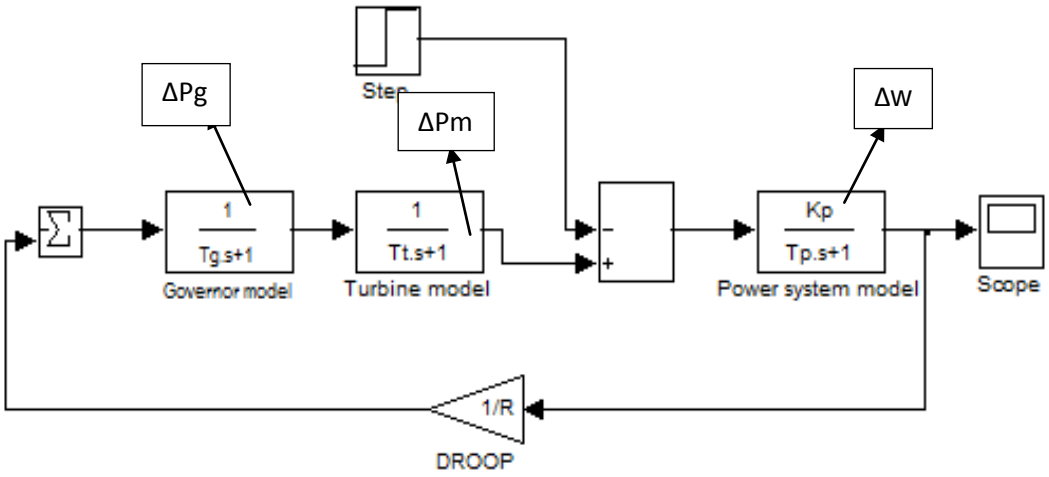


Fig .1: Single area power system without controller

Where Δwis the change in frequency for a step change in load. Here the change in frequency is not zero, so to keep frequency at its schedule value,a PI controller will be use.

2.2 Isolated power system employing Integral controller

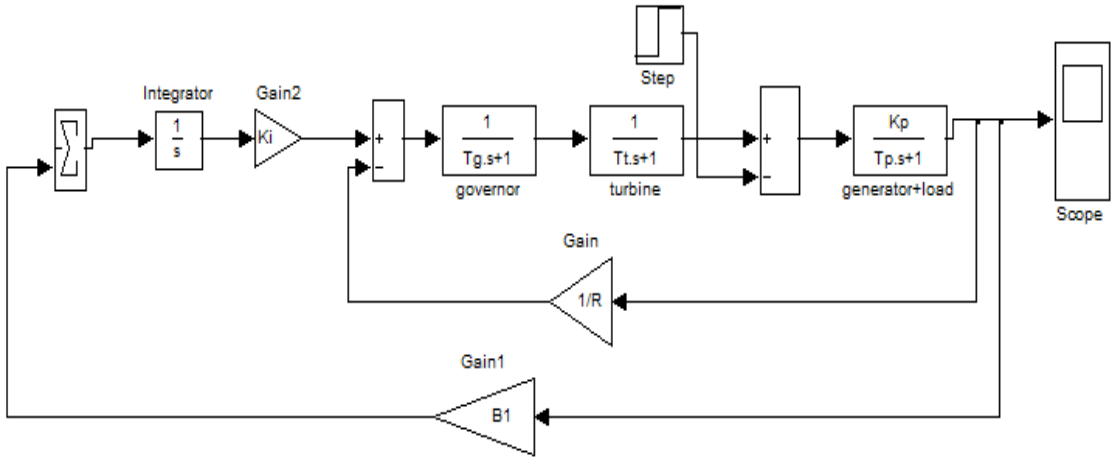


Fig.2

The automatic load frequency control loop (ALFC) is shown in fig.2.Here we use secondary loop which keeps thefrequency its nominal value. To maintain Δw=0 an integrator is used. Basically the integrator is used to measure the average error during a particularperiod of time and will remove the offset. The ability to retain its nominal value, this property of integrator is called rest action. As load on system changes continuously, so to maintain frequency at its nominal value the generation is adjusted automatically[16].

2.3 Designing of two area interlinked power system using integral controller

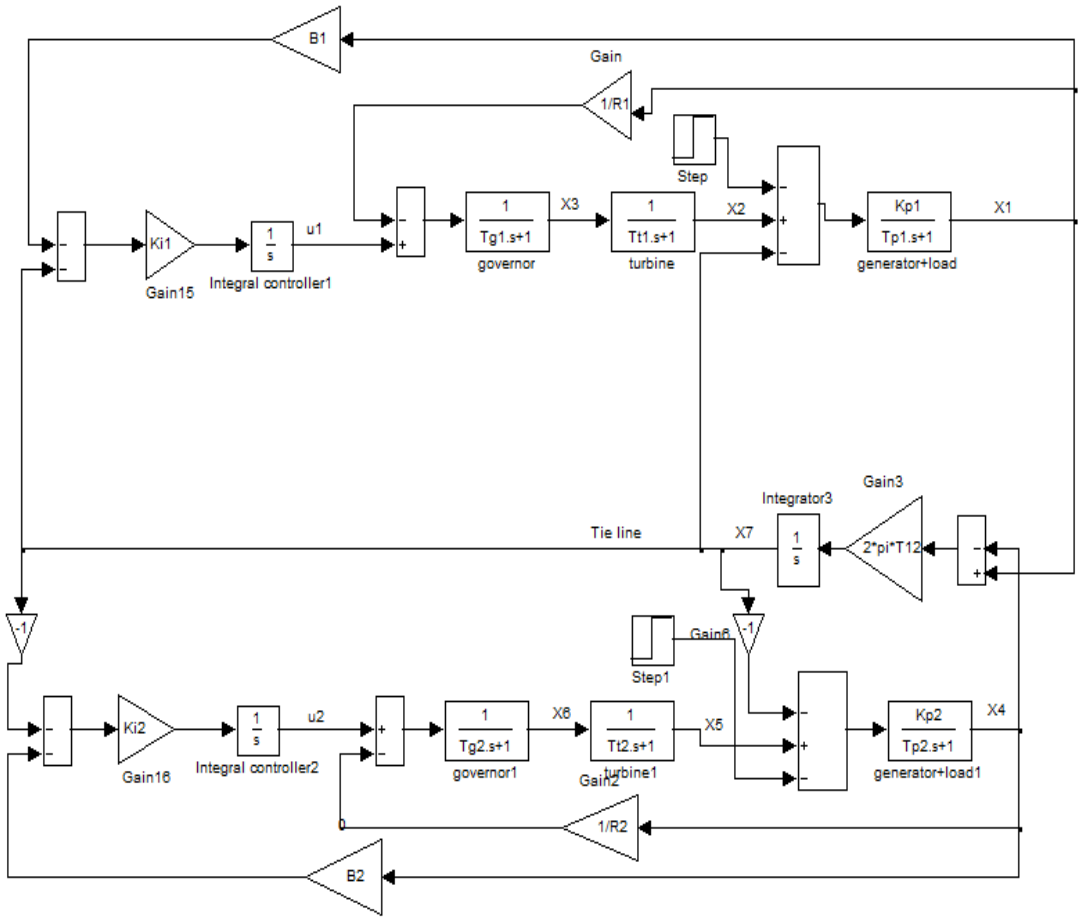


Fig.3

The block diagram representation of two interlinked power system with non-reheat turbine shown in fig.3. The two area are interconnected with the help of tie line.Both the area are provided by integral controller. There are total nine blocks which represent whole two area interconnected power system. The state equation can be formed easily with the help of transfer function of blocks. There are two controlling input named u_1 and u_2[2] [5] [9].

Equation of controlling input is written as

For area 1

$$\dot{u_1} = -Ki1(B_1 x_1 + x_7) \quad \text{..... (1)}$$

For area 2

$$\dot{u_2} = -Ki2(B_2 x_4 - x_7) \quad \text{..... (2)}$$

2.4 Linearization of two area interconnected power system using state space analysis

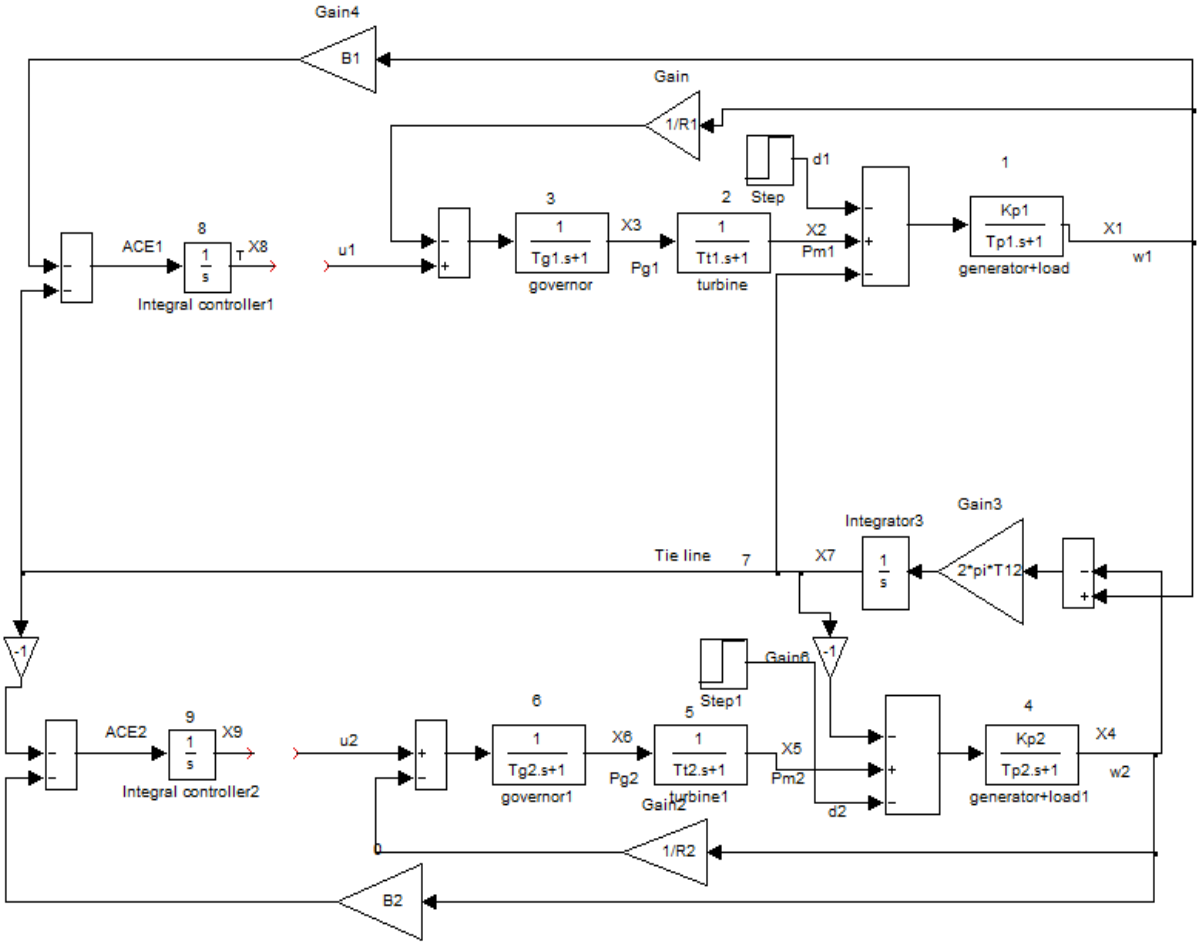


Fig.4

The generalized state space representation of two interconnected power system shown in fig.4. d1 and d2 are the disturbances in area1 and area2 respectively.

The state equations can be written as

For block 1

$x_1 + T_{p1}\dot{x_1}$= Kp1 $(x_2 - x_7 - d1)$

$\dot{x_1} = -\frac{1}{Tp1}x_1 + \frac{Kp1}{Tp1}x_2 - \frac{Kp1}{Tp1}x_7 - \frac{Kp1}{Tp1}d1$ ..... (3)

For block 2

$\dot{x_2} = -\frac{1}{Tt1}x_2 + \frac{1}{Tt1}x_3$ ..... (4)

For block 3

$\dot{x_3} = -\frac{1}{R1\,Tg1} - \frac{1}{T_{g1}}x_3 + \frac{1}{T_{g1}}u_1$ ..... (5)

For block 4

$$\dot{x}_4 = -\frac{1}{T_{p1}}x_4 + \frac{K_{p2}}{T_{p2}}x_{5+}\frac{K_{p2}}{T_{p2}}x_7 - \frac{K_{p2}}{T_{p2}}d2 \quad \text{(6)}$$

For block 5

$$\dot{x}_5 = -\frac{1}{T_{t2}}x_5 + \frac{1}{T_{t2}}x_6 \quad \text{(7)}$$

For block 6

$$\dot{x}_6 = -\frac{1}{R_2 T_{g2}}x_4 - \frac{1}{T_{g2}}x_6 + \frac{1}{T_{g2}}u_2 \quad \text{(8)}$$

For block 7

$$\dot{x}_7 = 2\pi T_{12}x_1 - 2\pi T_{12}x_4 \quad \text{(9)}$$

For block 8

$$\dot{x}_8 = B_1 x_1 + x_7 \quad \text{(10)}$$

For block 9

$$\dot{x}_9 = B_2 x_4 - x_7 \quad \text{(11)}$$

In general form these state equation can be written in single state equation

$$\dot{X} = Ax + Bu + Fd \quad \text{(12)}$$

Where A is a matrix of order 9×9 called state matrix, B is a matrix of order 9×2 called control matrix and F is a matrix of order 9×2.

And the vector ‘x’,‘d’, ‘u’ is written as

$x = [x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8 x_9]^T$, $u = \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}$, $d = \begin{bmatrix} d_1 \\ d_2 \end{bmatrix}$

2.5 Designing of optimal controller

The performance of system can be described in terms of cost which is to be minimized by LQR technique.

$$J = \frac{1}{2}\int_0^\infty (x^T Qx + u^T Ru)dt \quad \text{(13)}$$

Where ‘Q’ is ‘state weight matrix’ which is positive semi definite matrix. And ‘R’ is control semi definite symmetric weight matrix. The value of Q and R chosen according to requirement of the system.

For designing of optimal controller put

$$u = -Kx$$

Where feedback gain matrix ‘K’ is obtained by the solution of Riccati equation, which is given as

$$A^T P + PA - PBR^{-1}B^T P + Q \quad \text{(14)}$$

$K = R^{-1}B^{T}P$ …….. (15)

The system with state feedback is given by

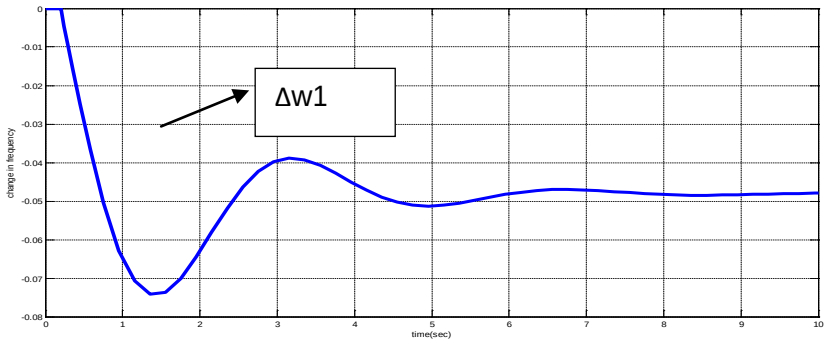
$\dot{x} = (A - BK)x$

For the stability of system the eigenvalues of $(A - BK)$ must have negative real part.

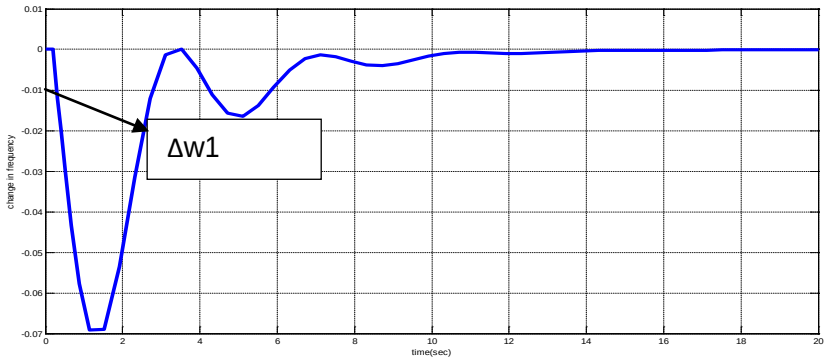
By MATLAB command $[K, P] = lqr2(A, B, Q, R)$

III SIMULATION RESULTS

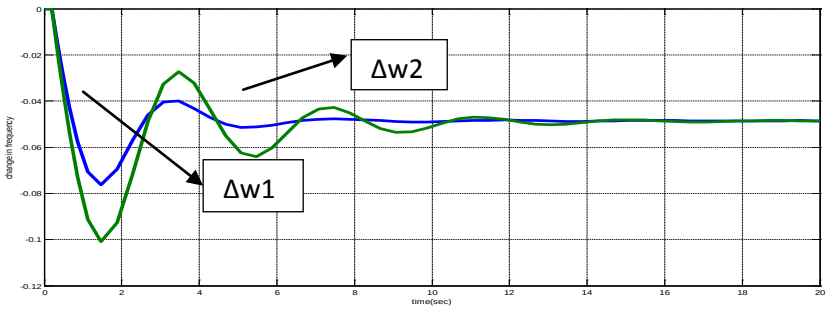
The results of Simulink are shown with PI and PID controller and the disturbance is taken as 1% for the systems. Later these results are improved by advance optimal control system.



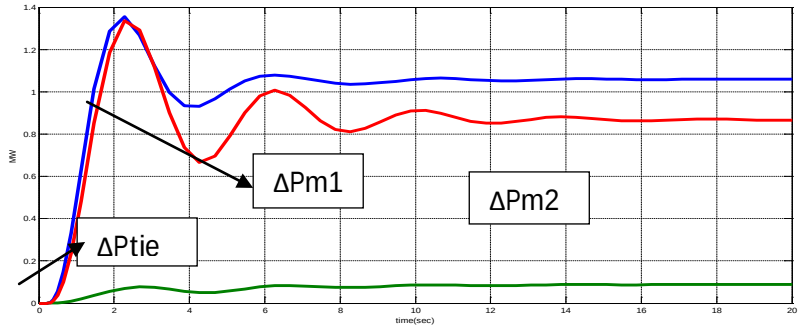
Frequency response of single area without controller



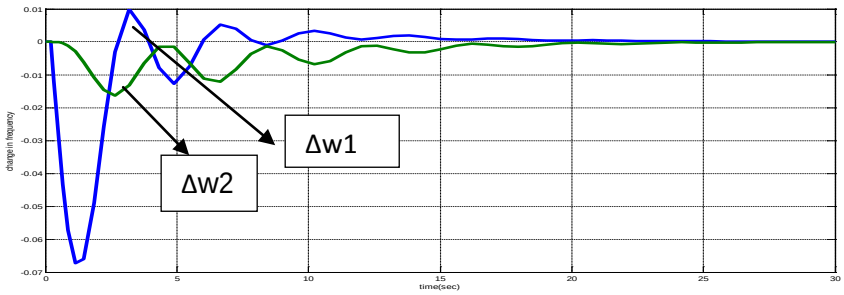
Frequency response of single area using integral controller



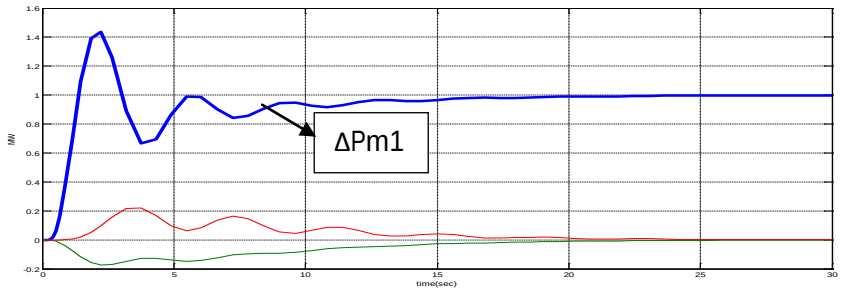
Frequency response of two area without controller



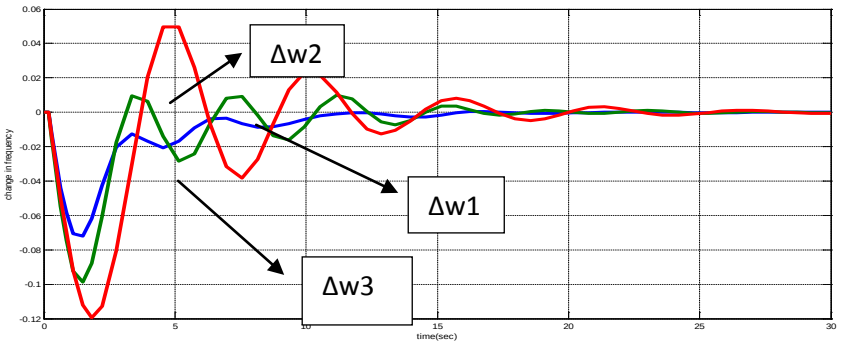
Power deviation of two area without controller



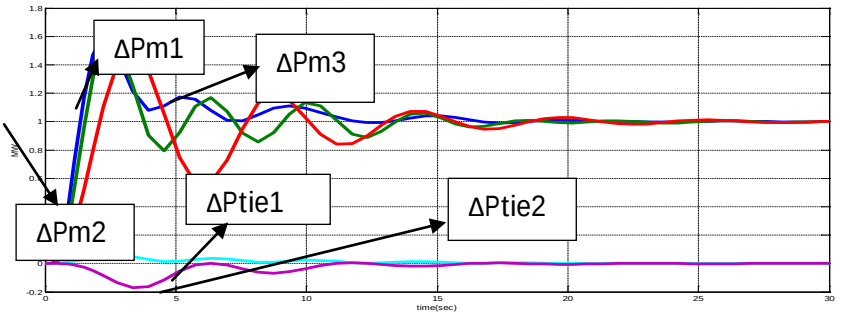
Frequency response of two interlinked power systemusing integral controller



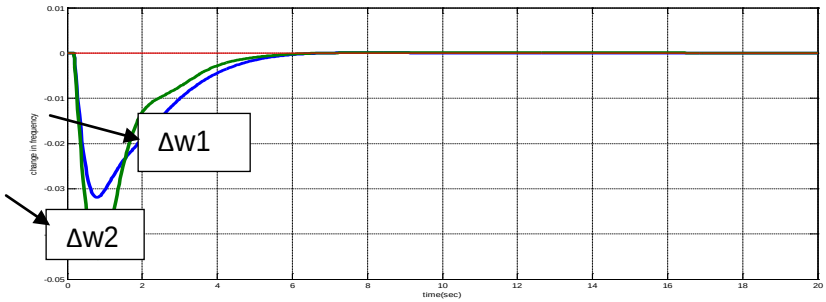
Power deviation response of two interlinked power system using integral controller



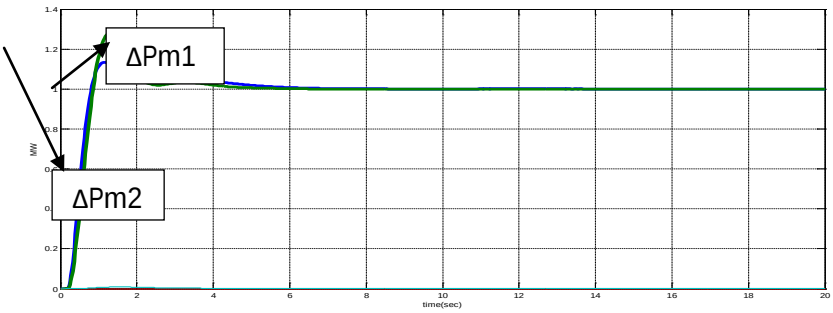
Frequency response of three interlinked power system using integral controller



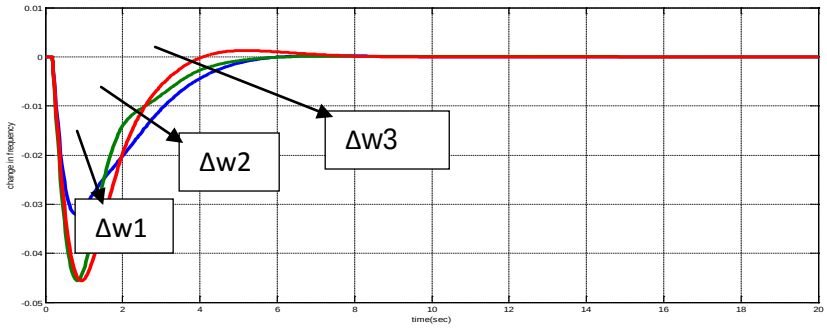
Power deviation of three interlinked power system using integral controller



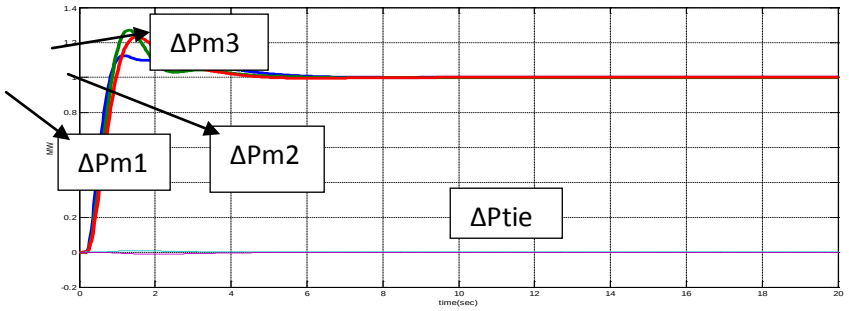
Frequency response of twointerlinked power system using PID controller



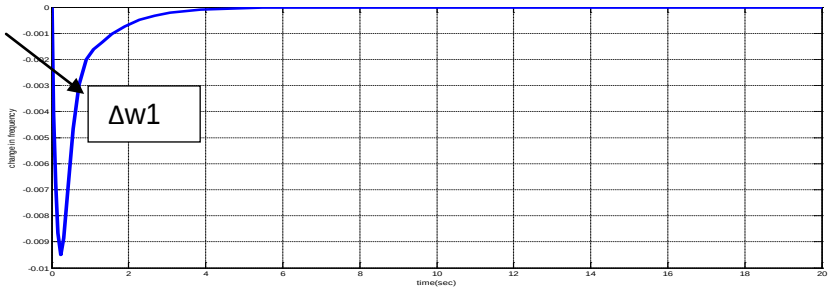
Power deviation response of two interlinked power system using with PID controller



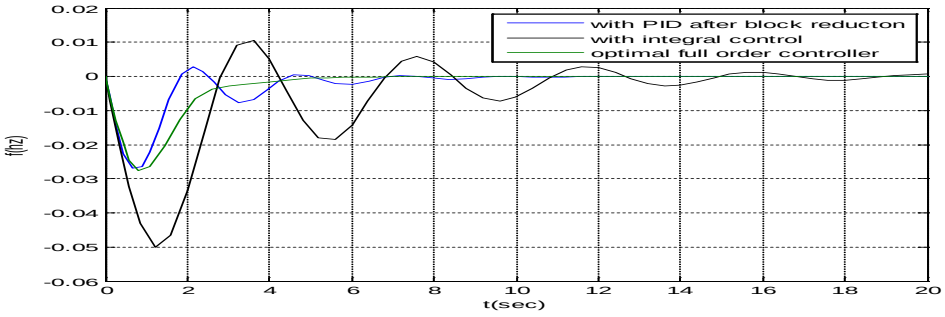
Frequency response of three interlinked power system using with PID controller



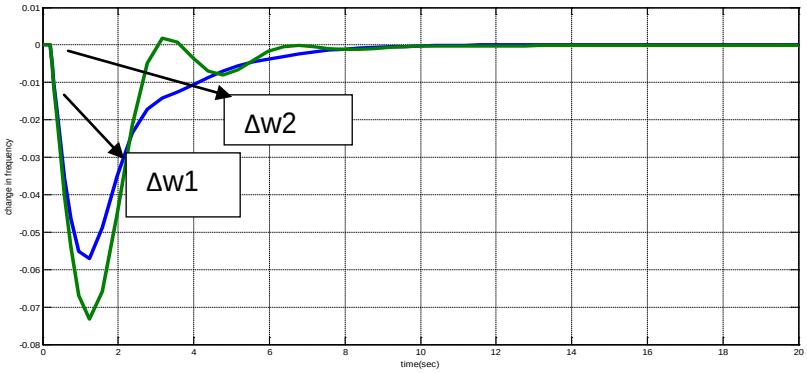
Power response of three interlinked power system using with PID controller



Frequency response of single area using optimal controller



Comparative study of simulation result (for first area)



Frequency response of two interlinked power system optimal controller (LQR technique)

IV CONCLUSIONS

In this paper the dynamic behavior of single area, two area and three area interlinked power system is examine with various controllers. It is found that PID controller gives better performance than PI controller. We have also tried to develop an optimal controller for two area interconnected power system. Finally it is concluded that LQR method gives more improved response in comparison to PI and PID controller.

Appendix:

System parameters –

$T_{g1} = 0.2$ pu

$T_{t1} = 0.5$ pu

$T_{p1} = 12.5$ pu

$K_{p1} = 1.25$ pu

$T_{g2} = 0.3$ pu

$T_{t2} = 0.6$ pu

$T_{p2} = 8.88$ pu

$K_{p2} = 1.11$ pu

2*pi*$T_{12} = 1.4$ pu

$R_1 = 0.05$ pu

$R_2 = 0.0625$ pu

$B_1 = 20.6$ pu

$B_2 = 17$ pu

For PID controller (3 area power system)

K_P	K_I	K_D
0.63	0.74	0.93
0.91	0.875	1.0
1.20	1.15	1.2

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