RELIABILITY ASSESSMENT OF LOW POWER AND PARAMETRIC INTERRUPTION BREAK REDUCTION IN TSV (THROUGH-SILICON-VIA) BASED 3D-ICS

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ABSTRACT

Power consumption and Reducing the parametric interruption has become an important concern in 3D IC technologies. This paper deals with both low power and parametric interruption analysis for Through-Silicon-Via (TSV) based on 3D ICs. Initially considering about TSV count, wire length, and the parameter interruption break could occur in a TSV. The wire length reduction based on tree generation Method of Mean and Medians (3D MMM) algorithm. It can be establish possible number of TSV count to minimize the overall power consumption. Parametric interruption break could occur in a TSV of a 3D-ICs due to manufacturing imperfection. Finding of such a break is must for imperfectness diagnosing, yield learning, and /or reliability viewing. To test those defect, paper is about an innovative plan-for-testability technique titled as Inconsistent Output Threshold (IOT). Disclosing that by dynamically shifting output of a TSV from a normal inverter to a Schmitt-Trigger inverter, the parametric interruption break on the TSV can be characterized and detected. Utilizing IOT analysis technique for further derive the propagation delay of each TSV participating in an oscillation ring through extract process. In this process, have consider bother the strength of the two TSV drivers, and then measure their effects in terms of change in the oscillation ring's period. By some following analysis, the propagation delay of each TSV can be revealed so the parametric delay fault on TSV can be characterized and perceive. SPICE simulation reveals that this model remains good change when there is significant process variation. A scalable test infrastructure indicates that the test time is modest at only 0.126 ms and 0.0527 ms for 2 TSVs, when the test clock is running at 10 MHz.

Keywords: 3-D ICs, Inconsistent Output Threshold, Oscillation ring, Parametric interruption, Through-silicon-via.

I. INTRODUCTION

A 3D integrated circuits, the idea behind 3D IC's is to mount two or more dice on top of each other. An individual die is now so thin it would be possible to mount 100 on top of each other to form a cube. Another technique is to take a group of dice that all perform an identical function (for example like memory chips) to build them into a 3D stack. In a modern framework, it will involve at least one die being mounted on the top of

another die, with the lower die employing TSVs to allow the upper die to communicate with the lower die and the SiP substrate. It can have a memory die attached to a logic die (or vice versa), or an analog/RF die attached to a digital logic die. [10] and so on.

A through-silicon-via (TSV) is a vertical electrical connection passing completely through a silicon wafer or die. TSVs are a high performance technique used to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the VIAs(Vertical Interconnect Access). It is substantially higher because the length of the connections is shorter [15]. A 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies interconnecting them vertically, so that they behave as a single device. By using TSV technology 3D ICs can pack a great deal of functionality into a small "footprint." The different devices in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and other materials into a single IC [13].

A catastrophic fault is a sudden and total failure of some system where recovery is impossible. Catastrophic failures often lead to cascading system failures. The term is most commonly used for structural failures but has often extended for many other disciplines where total and irrecoverable loss occurs [14]. The stages of the ring oscillator are often differential stages that are more immune to external disturbances. This renders are also available in non inverting stages. A ring oscillator can be made with a mix of inverting and non inverting stages by providing the total number of odd inverting stages. The oscillator period in all cases is equal to twice the sum of the individual delay in all the stages [12]. In unspecialized, a TSV is a inaccurate interconnecting conductor, with very petite resistance but extensive condenser. An in-depth investigating of the interlink inactivity supporter can be institute in [17].

A design for outspoken break menstruation was planned, in which the oscillation strip construct was applied to remember the inactivity of a cadre in a closed-loop sort [5]. Moreover, the RO can be used to essay stuck-at faults and retard faults related with the connect wires in a 2-D IC, as demonstrated in [13], [14], and [18]. These schemes, though potent, may not be pronto practical to the TSVs in a 3-D IC. Very lately, a method was planned in to notice parametric detain faults. It incorporates a transistor connecting at each TSV to make a voltage mortal with the faulty resistivity of the TSV, and uses an similarity comparator to observe the resulting voltage to execute a pass/fail try. The method requires an analog reference voltage scattered to all TSVs low effort. In this theme, we give a two-step characterization-based judge method [8]. Prototypic, we resemble the propagation break crossways a TSV with a resistive unsettled charge. Wares, passing a tryout resolution either based on a test threshold or finished outlier reasoning.

At the intuition of this method is a new technique called *Inconsistent Output Threshold* (IOT) [21]. The IOT group is implemented with an RO structure consisting of two TSVs and a enumerate of logic entrepreneur. The great dimension that differentiates it from all previous RO-based schemes is that each TSV's turnout inverter is outfitted with a shifting threshold, significant that it can be obsessed to bear equal a natural CMOS logic inverter or a Schmitt-Trigger inverter (with unbalanced 0 à 1 and 1 à 0 thresholds) [22][23]. The most eminent conception of this theme can be explicit are given by dynamical the TSV's output inverter from a normal one to an Schmitt Trigger, the undulation period of the RO will change, with the disagreement reflecting the propagation delay crossways the TSV. The rest of this paper is corporate in next portion II provides aspect aggregation, including essential electrical model of a TSV, and a short review of IOT analysis [21]. Portion III

proposes the new architecture supporting the IOT scheme and its operations. Portion IV presents the experimental results, and Portion V concludes this paper.

II. TSV STRUCTURE

The TSVs that are fabricated after all the transistors and metal layers are formed. Fig. 1. shows the cross-sectional view that a die with TSVs. Circuits in a die use the top-level metal (front metal) to connect a TSV with other circuit elements in the design and the bottom of a TSV is connected with some back metal which is utilized to link to another die's front metal when two dies are bonded.

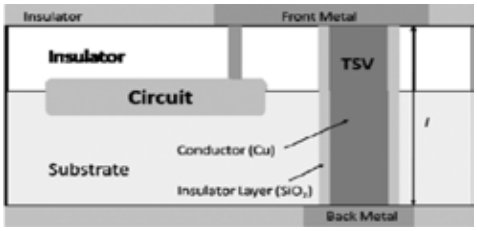


Fig 1: Cross Section View of TSV

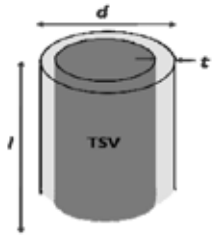


Fig 2: Cylindrical Structure of TSV

The conductor of TSVs could be copper or other metal material. It is isolated from Si substrate with insulator layer (e.g., SiO). Fig. 2. Shows the 3-D structure of a TSV as in a cylinder shape [9].

2.1 RC MODEL

Analytically, model of resistance and capacitance of TSV by the following equations, where *l* and *d* are the length and diameter of the TSV, *t* is the thickness of the insulator (SiO_2) between the silicon substrate and the Copper material inside the TSV ρCu is the Copper resistivity and ϵSiO_2[6].

$$R = \rho \times l/A \quad (1)$$

Providing parasitic RC characteristics of TSV and Micro-bumps, the capacitance changes according to voltage Vg, depends on Vfb & Vth the dielectric constant of SiO_2.

Accumulation : (Vg < Vfb)

$$C = Cox \quad (2)$$

Depletion : (Vfb < Vg < Vth)

$$C = Cox\ Cdep / (Cox + Cdep) \quad (3)$$

Inversion : (Vg > Vth)

$$C = Cox\ Cdep / (Cox + Cdep) \quad (4)$$

TABLE 1: Values of resistance and capacitance

	Normal	Best	Worst
Resistance (mΩ)	46	39	56
Capacitance (fF)	122	105	141

The values of resistance and capacitance are calculated according to voltage Vg depends on three regions from that three cases values normal, best and worst are obtained. We can use the normal or best values to do the RC modeling for TSV.

III. TSV INTERRUPTION MODEL

3.1 TSV Modeling

For a TSV with physical parameters resistance (RTSV) and capacitance (CTSV) are to be deliberate using length, surrounding oxide wideness, and length. Supported on an analytical TSV RC models presented, the significant term invariable of this wire. This is an extremely small valuate compared to the essential gate delay (which is in the extent of tens to hundreds of picoseconds in a exemplary 0.25μm impact). Nevertheless, the condenser of a TSV is much larger than that of an on-chip interconnect [17]. As a prove, the detain caused by a TSV is not in the wire itself, but in its dynamic gate. Supported on this observation, have defined the TSV delay as the overall propagation delay crosswise the TSV structure and its driver gate [13].

3.2 Delay Model in Transmission Line of A TSV

A TSV can be viewed as a transmission conductor, which takes its effect of its inductance and its conductance to surface, as shown in Fig. 3. This image also shows the connections of the R, L, C, and G as celebrity that the effects of the inductance L and the conductance G may not be negligible when the TSV is utilized for transmitting a high frequency analog signal. To verify the above statement, perform of the RLCG model, with the inductance increased 1000× from its typical value to 2.8 nH. The waveforms will occurs to applied input as 0→1 of the TSV inverting driver. In Fig. 4. A 1→0 transition is observed at the endpoint of the TSV B [9] [19]. The output transition at node B exhibits low-amplitude ripples due to the increased inductance but overall, the propagation delay of the signal remains almost unchanged. The CTSV will dominate the delay of a fault-free TSV. However, RTSV could have a significant impact on a faulty TSV if its value is large enough to be comparable to the effective on-resistance of the driver.

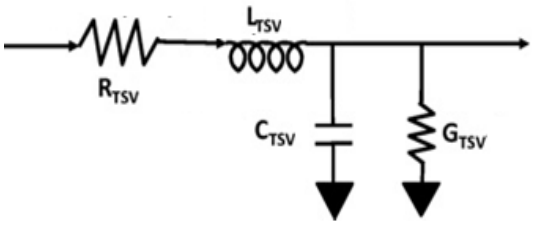


Fig 3: Transmission line-based circuit model for a TSV

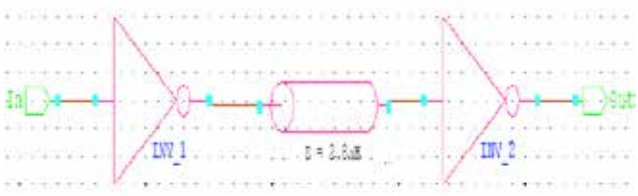


Fig 4: Simulation of a Signal propagating through a TSV

3.3 INPUT SENSITIVE ANALYSIS

In this section, review the most related previous work proposed in referred to as input-sensitivity (IS) analysis, which aimed to predict the capacitance of each TSV under test. As shown in Fig 5 two TSVs are paired to form a RO. The resulting period of the RO is twice the propagation delay around the ring. Observing the oscillation

period of this RO can reveal certain delay information. The RO can be dynamically set to one of three different configurations by tuning the strengths of the input drivers of the two TSVs, namely:

1) Normal configuration.
2) TSV1−driver−reduced configuration
3) TSV2−driver−reduced configuration

During test mode, the three RO configurations are turned on in sequence and the oscillation period of each configuration is measured. A procedure is then followed to map the measurement results to the capacitance and propagation delay across each of the two TSVs [20]. The main idea of the IS analysis is that the capacitance of a TSV can be reflected in the change of the oscillation period of the RO, while perturb the driving strength of the input buffer of that TSV, regardless of the periphery circuit in the oscillation ring. Although the IS analysis can capture the effect of the TSV capacitance, it has a limitation of not being able to factor in the effect of the TSV resistance (which affects the wire part of the TSV delay) when the TSV is highly resistive [19] [20]. This is a drawback that might not be very detrimental if one only attempts to use it to gauge the TSV's capacitance or to profile the delays across mostly fault-free TSVs. But it is a problem if one attempts to measure the delay across a faulty TSV with a resistive open fault.

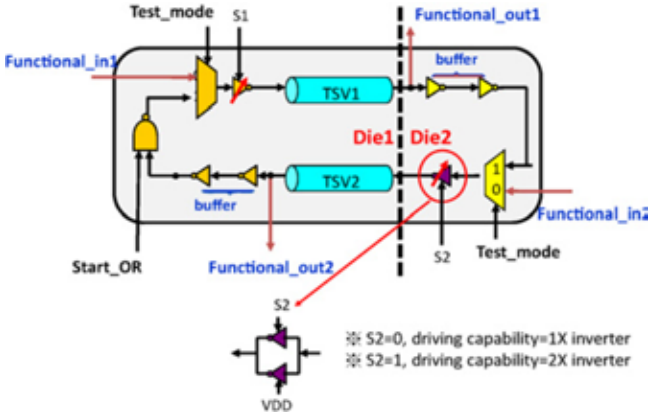


Fig 5: Architecture for a TSV pair

IV. INCONSISTENT OUTPUT THRESHOLD TECHNIQUE

4.1 Operating of Schmitt Trigger Inverter

The having investigated the behavior of high-gain amplifier with no feedback, now turn to amplifier with positive feedback, also known as Schmitt Triggers. Schmitt Trigger is a wave shaping circuit, used for generating of square wave. It is a bi-stable circuit in which two transistor switches are connected re-generatively [22]. It has a hysteresis property, The hysteresis in Schmitt trigger is valuable when conditioning noisy signals for using digital circuit. The noise does not causes false triggering and so the output will be free from noise. The input import that a larger-than practice input voltage drop is required to change the output logic level. In opposite line, impoverishment a higher voltage to locomote the output of a Schmitt Trigger inverter from "1" to "0," and lower voltage to alter the output from "0" to "1" as shown in Fig. 6.

The hysteresis property requires two different thresholds:

1) A high-to-low threshold, is given as HL

2) A low-to-high threshold, is given as LH , as can be seen in the voltage transfer curve obtained by SPICE simulation using a 0.25 µm CMOS process. The high-to-low threshold, HL, is the input voltage beyond which one can change the output state from "1" to "0," while low-to-high threshold, LH, is the input voltage below which one can change the output state from "0" to "1." In detail, the drive-up path and the drive-down path of an Schmitt Trigger inverter are each composed of two transistors in cascade. The hysteresis property is created by slightly dragging the voltage of the mid points of the drive-up and drive-down paths, to take advantage of the body effect of MOS transistors.

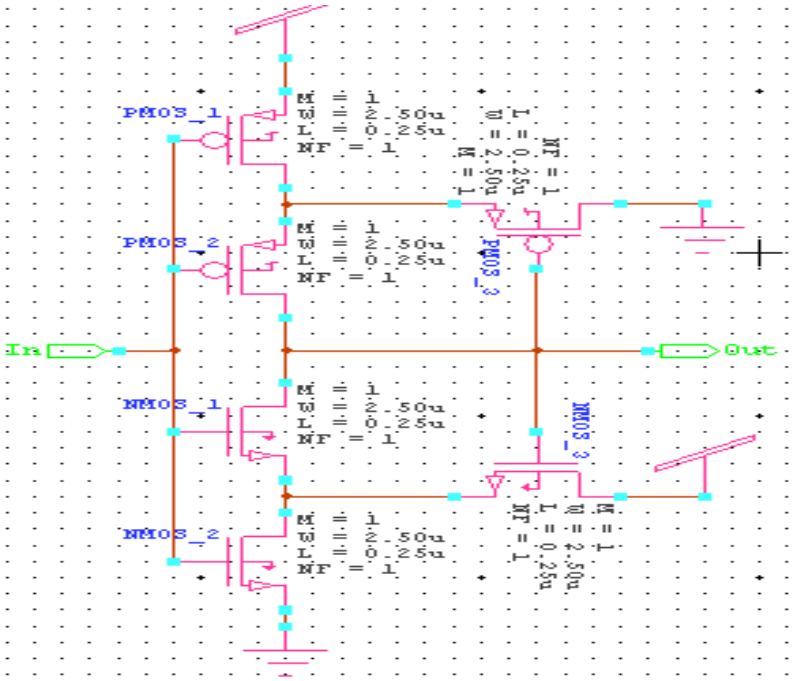


Fig 6: Schmitt – Trigger Inverter

4.2 Structure of IOT Analysis

As illustrated in Fig. 7. a pair of TSVs is configured into an RO, similar to the IS analysis. To support the IOT analysis, there is a change in the output inverter of each TSV with variable threshold, as defined. A IOT inverter is the combination of a normal CMOS inverter and an ST inverter, with the function depending on the value of a control signal 'X'.

In other words, a IOT inverter operates in two different modes:

1) Common approach
2) Schmitt Trigger approach

When X = 0, IOT inverter = Common CMOS inverter. While X = 1, IOT inverter = Schmitt Trigger inverter.

There are two IOT inverters in a test unit composed of two TSVs as shown in Fig. 7, one for each TSV. Their controlling signals are denoted as X_1 (for the IOT inverter of the TSV_1) and X_2 (for the IOT inverter of the TSV_2).

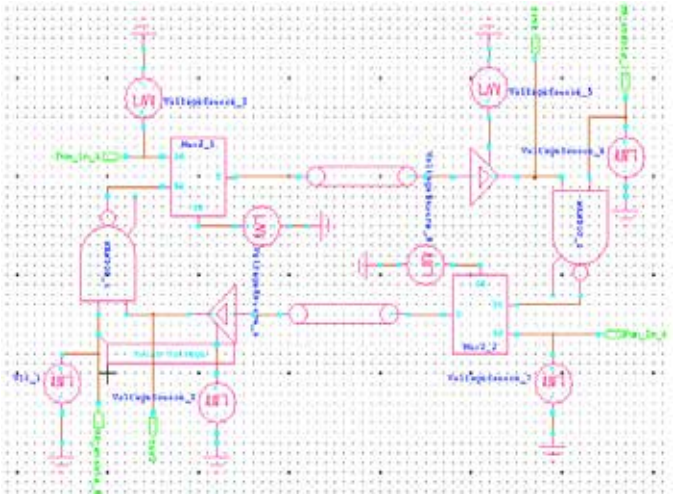


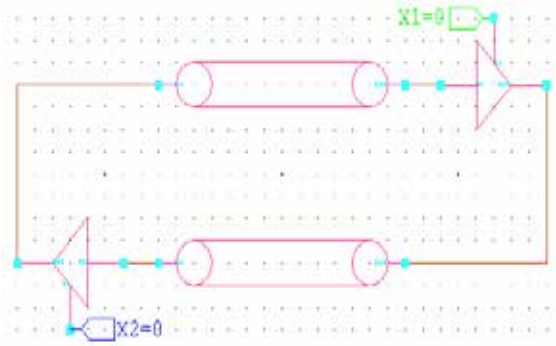
Fig 7: Schmitt of a TSV Supporting IOT

Based on the value combination of <X_1, X_2>, three configurations in IOT analysis are as summarized in (Fig. 8., Fig. 9., Fig. 10.)

1) Normal Design: (X_1, X_2) = (0, 0), i.e., both IOT inverters are in their Common approach. The oscillation period of the RO is denoted as T_{REF}

2) TSV_1-in-ST Design: (X_1, X_2)= (1, 0), i.e., the IOT inverter associated with TSV_1 is in the Schmitt Trigger approach, while that of TSV_2 is in its common approach. The oscillation period of the resulting RO is denoted as $T_{ST1.}$

3) TSV_2-in-ST Design: X_1, X_2 = (0, 1), i.e., the IOT inverter associated with TSV_2 is in the Schmitt Trigger approach, while that of TSV_1 is in its common approach. The oscillation period of the resulting RO is denoted as T_{ST2}.



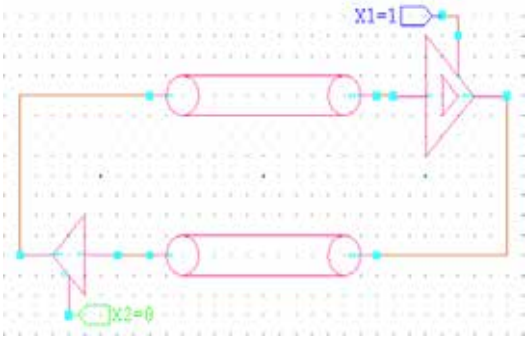


Fig 8: Common Configuration **Fig 9: TSV1 in Schmitt Trigger**

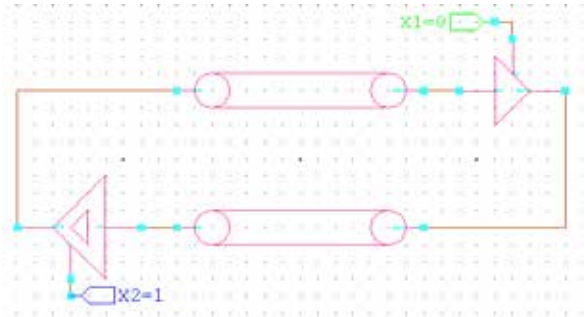


Fig 10: TSV2 in Schmitt Trigger

A IOT inverter can be realized by a schematic as shown in Fig. 11. Its equivalent circuit is depicted when the control signal X is "0" (in which case it becomes to a common inverter). When the control signal X is "1" (in which case it becomes to an Schmitt Trigger inverter).

4.3 Overall Flow

There are three major steps in the measurement phase for each test unit (composed of a TSV pair) shown in Fig. 12.

In step 1, activating the RO in its normal configuration and measuring the result oscillation period, denoted as T_{REF}.

In step 2, activating the RO in its TSV1-in-ST configuration and measuring the resulting oscillation period, denoted as T_{ST1}.

In step 3, activating the RO in its TSV2-in-ST configuration and measuring the resulting oscillation period, denoted as TST2. In the prediction phase, following computations are to be done.

$$\Delta T_{ST1} = T_{ST1} - T_{REF} \qquad \Delta T_{ST2} = T_{ST2} - T_{REF}$$

The two derived timing parameters ΔT_{ST1} and ΔT_{ST2} can be regarded as the timing signatures of the two TSVs (ΔT_{ST1} for TSV1 and ΔT_{ST2} for TSV2). They are correlated with the TSV delays, with the following rationale.

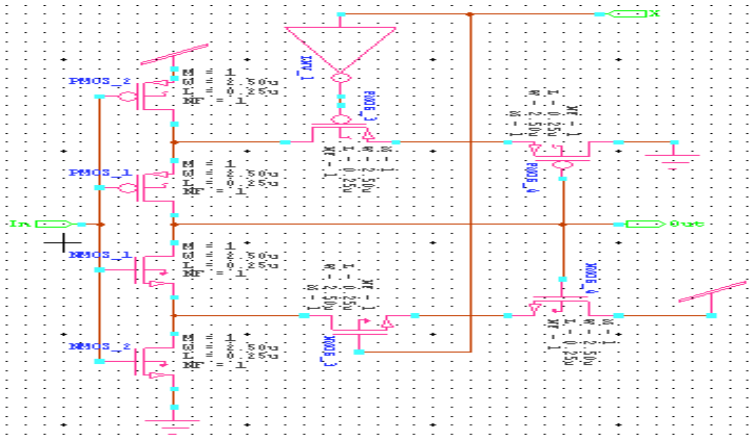


Fig 11: Operation Between a common and ST inverter

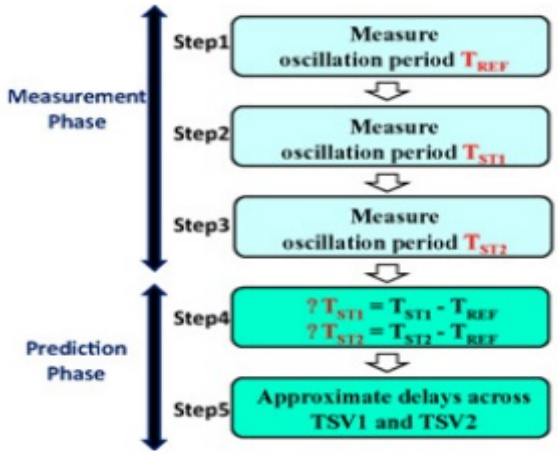


Fig 12: Overall Flow for TSV delay observation

A larger TSV delay (due to excessive R) induces a larger rise/fall time in the signal waveform at the endpoint of the TSV. At the output of the IOT inverter, the rise/fall time will translate into a measurable period difference between the normal configuration and the TSV-in-ST configuration. It is notable [9],[19],[20] that the delays due to the peripheral circuitry in the RO (such as the multiplexers and the triggering XOR gates) have been canceled out, since to calculate $\Delta T_{ST} = (T_{ST} - T_{REF})$ and thus ΔT_{ST} will reflect only the delay across the associated T_{SV}. It is also notable that even though the traditional oscillation ring formed by a TSV pair without IOT inverters might be able to reflect the extra TSV delay for fault detection, it has one major drawback compared to this method, when observing a larger-than-normal oscillation period using the traditional oscillation ring, it cannot be concluded whether the extra delay is caused by a TSV or other circuitry in the oscillation ring. In contrast, IOT scheme provides a zoom-in view to each TSV delay and provides higher characterization resolution as well as diagnostic capability.

V. EXPERIMENT RESULT

The simulation results that take into account the process variation of our CMOS 0.25µm process.

5.1 IOT Analysis

When X = 0, IOT inverter = Common CMOS inverter.

While X =1, IOT inverter = Schmitt Trigger inverter. When X = 0 and X = 1, The delay measurement are calculated for voltage 0.5 V and frequency at 10 MHz. The maximum difference delay between both approaches 0.13nS.

5.2 Delay and Power Calculation

For Example: TSV Model: C_{TSV} = 50pF, L_{TSV} = 2.8pH, $G_{TSV} = 0.1n\Omega^{-1}$, R_{TSV} = 30mΩ, 3KΩ.

Fig. 13. shows simulation results that takes into account the process variation of our CMOS 0.25 µm process for a TSV with C_{TSV} = 50 pF. In this analysis, a noise-free power supply voltage is given for each TSV faults. Based on the above results, one test flow for parametric delay fault detection can be proceeding as follows. For a test unit, it derives the ΔT_{ST1} and ΔT_{ST2} for the two TSVs by the IOT analysis, respectively. Which are shown in below graph.

At Measurable Phase Of ΔT_{ST1} and ΔT_{ST2} $\Delta T_{ST1} = T_{ST1} - T_{REF} = 0.1265 \times 10^{-6}$sec

$\Delta T_{ST2} = T_{ST2} - T_{REF} = 0.05273 \times 10^{-6}$sec

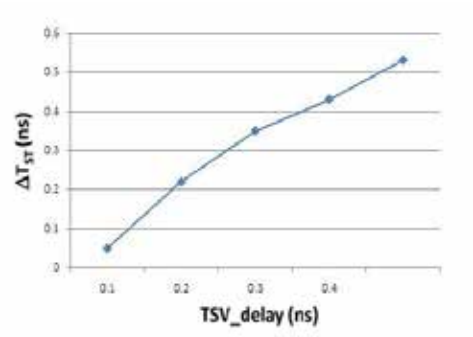


Fig 13: The measurement of Overall Flow for TSV delay Observation

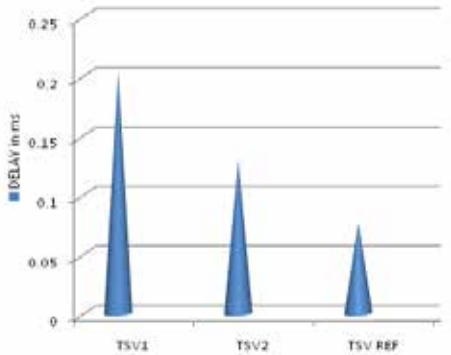


Fig 14: Comparison of T_{REF}, T_{SV1}, T_{SV2} delay Measurement

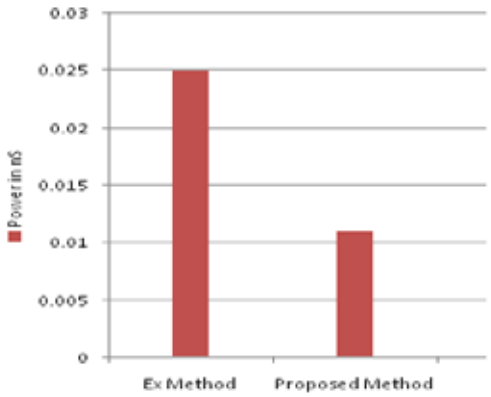


Fig 15: Comparison of Power Calculation

VI. CONCLUSION

The parametric delay reduction methods for TSVs are mostly for gross delay with the values exceeding a target system clock period. It is unique in its ability to characterize the extra delay across a TSV with a resistive open fault. A IOT scheme using only logic circuit was proposed. In this scheme, dynamically switching the inverter of a TSV from a normal inverter to an Schmitt Trigger, the propagation delay across the TSV can be approximated. SPICE simulation validates that there exists a linear relationship between the TSV delay to be quantified and the quantity that can be measured (denoted as ΔT_{ST} by the proposed scheme). The oscillating period of T_{REF}, T_1, T_2 are measured and ΔT_{ST1} and ΔT_{ST2} are calculated. By over flow TSV-delay prediction approximate delay across TSV_1 and TSV_2 are calculated and delay reduced using Schmitt-Trigger inverter. For future enhancement to analyze crosstalk behavior of TSVs in 3-D integrated system.

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RELIABILITY IMPROVEMENT IN ZERO BYPASS MULTIPLIER

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ABSTRACT

Digital multipliers are among the most critical arithmetic function all units. The overall performance of these systems depends on the through put of the multiplier. Mean while, the negative bias temperature instability effect occurs when a p MOS transistor is under negative bias ($V_{gs} = -V_{dd}$), increasing the there should voltage of the p MOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature in stability, occurs when an MOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aw are multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher through put through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column-or row-bypassing multiplier.

Keywords: AHL, NBTI, PBTI.

I.INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units inmanyapplications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The through put of these applications depend son multipliers, and if the multipliers are too slow, he performance of entire circuits will be reduced. Furthermore, negative bias temperature in stability (NBTI) occurs when a pMOS transistor is under negative bias ($V_{gs}= -V_{dd}$). In this situation, the interaction between inversion layer hole sand hydrogen passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H_2 molecules [20].When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (V_{th}), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing he NBTI effect .However, there verse reaction does not eliminate all the interface traps generated during the stress phase, and V_{th} is increased in the long term. Hence it is important to design are liable high performance multiplier.

A faster way to implement multiplication is to resort to an approach similar to manually computing a multiplication. The entire partial product are generated at the same time and organized in an array. A multi operand addition is applied to compute the final product. The approach is illustrated in the Fig.1. This set of operation an be mapped directly in to hardware. There structure is called an array multiplier and combines the following three functions: partial- product generation, partial-product accumulation and final addition.

Four important types of multipliers are available. 1. Array, 2.Baughwooley 3.Braun 4. Wallace tree are constructed using different types of adder cells presented. Then find out the best one in the performance characteristics like power dissipation, speed and area.

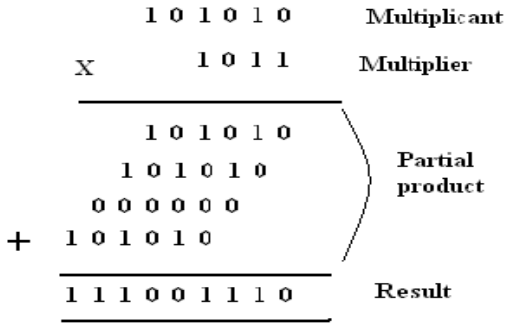

Fig.1. Example of manual multiplication

II. NBTI AND PBTI

Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are the two well-known circuit reliability issues in these conductor devices. The NBTI in PMOS transistors and the PBTI in the NMOS transistors occur when the transistors are biased in the strong inversion region. The NBTI and PBTI stresses cause the threshold voltage (V_{th}) of transistors drift strongly depending on the stress time and stress condition. This degrade the transistor performance over time. NBTI has been dominant in the poly-gate CMOS technologies. However, both NBTI and PBTI become significant in the high-k metal gate process.

Negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (V_{gs}= $-V_{dd}$). In this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H_2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage(V_{th}), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect.

However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and V_{th} is increased in the long term. Hence it is important to design a reliable high performance multiplier. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias.

III.BACKGROUND AND RELATED WORK

These are the modules used to achieve reliable high performance multiplier even after aging occur. These are the modules in aging aware reliable high performance multiplier.

1. Array Multiplier

2. Column Bypass Multiplier

3. Row Bypass Multiplier

4. Razor flip-flop

5. AHL Circuit

3.1. Array Multiplier

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. Many researchers have tried and are trying to design multipliers which offer either of the following high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. Thus making them suitable for various high speed, low power, and compact VLSI implementations. Generally as all we know multiplication goes in two basic steps.

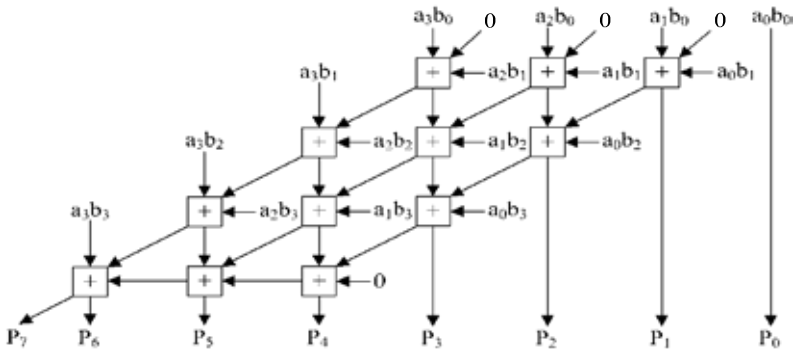

Fig.2.4×4 Array Multiplier

3.2. Column Bypass Multiplier

A column bypassing multiplier is an improvement on the normal array multiplier (AM).The AM is a fast parallel AM and is shown in Fig.2. The multiplier array consists of (n−1) row carry save adder (CSA), in which each row contains (n−1) full adder (FA) cells. Each FA in the CSA array has two outputs:

1) The sum bit goes down 2) The carry bit goes to the lower left FA. The FA in the AM are always active regardless of input states. In a low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig.3 shows a 4×4 column-bypassing multiplier. Suppose the inputs are 1010_2*1111_2, it can be seen that for the FA in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product a_ib_i. Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.

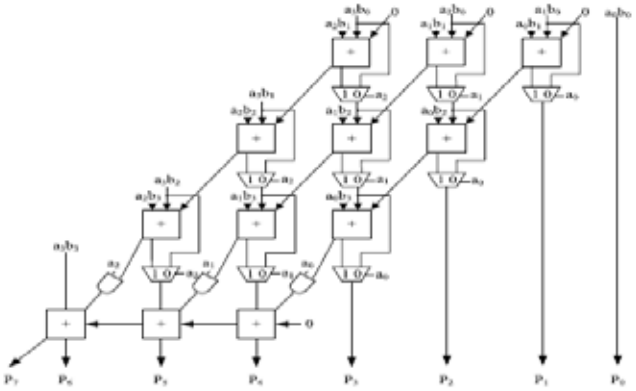

Fig.3. 4×4 Column Bypassing Multiplier.

3.3. Row bypass multiplier

A low-power row-bypassing multiplier is also proposed to reduce the activity power of the AM. Fig.4 is a 4×4 row-bypassing multiplier. Each input is connected to an FA through a tri-state gate. When the inputs are 1111_2 *1001_2, the two inputs in the first and second rows are 0 for FAs. Because b_1 is 0, the multiplexers in the first row select a_ib_0 as the sum bit and select 0 as the carry bit. The inputs are bypassed to FA in the second rows, and the tri-state gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similarly, because b_2 is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row because the b_3 is not zero.

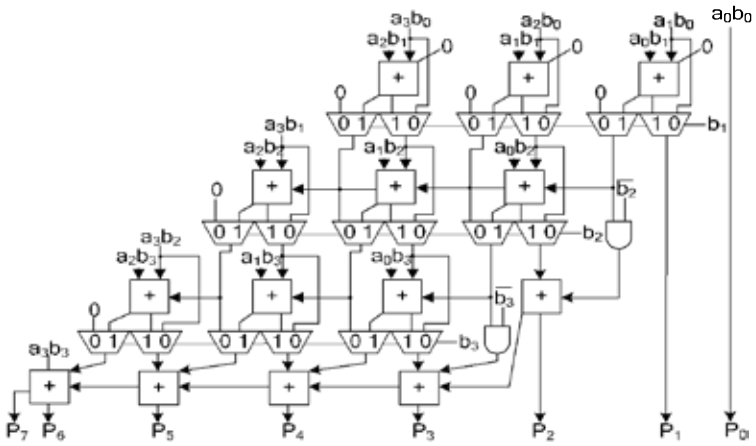

Fig.4. 4×4 Row Bypassing Multiplier.

3.4. Razor Flip-Flop

Razor relies on a combination of architectural and circuit level techniques for efficient error detection and correction of delay path failures. The concept of razor is illustrated in Figure for a pipeline stage. Each flip-flop in the design is augmented with a so called shadow latch which is controlled by a delayed clock. And illustrate the operation of razor flip-flop in Fig. 5. In clock cycle1, the combinational logic $L1$ meets the setup time by the

rising edge of the clock and both the main flip-flop and the shadow latch will latch the correct data. In this case, the error signal at the output of the XOR gate remains low and the operation of the pipeline is unaltered.

To guarantee that the shadow latch will always latch the input data correctly, the allowable operating voltage is constrained at design time such that under worst-case conditions, the logic delay does not exceed the setup time of the shadow latch [9]. By comparing the valid data of the shadow latch with the data in the main flip-flop, an error signal is then generated in cycle 3 and in the subsequent cycle, cycle 4, the valid data in the shadow latch is restored into the main flip-flop and becomes available to the next pipeline stage *L*2.

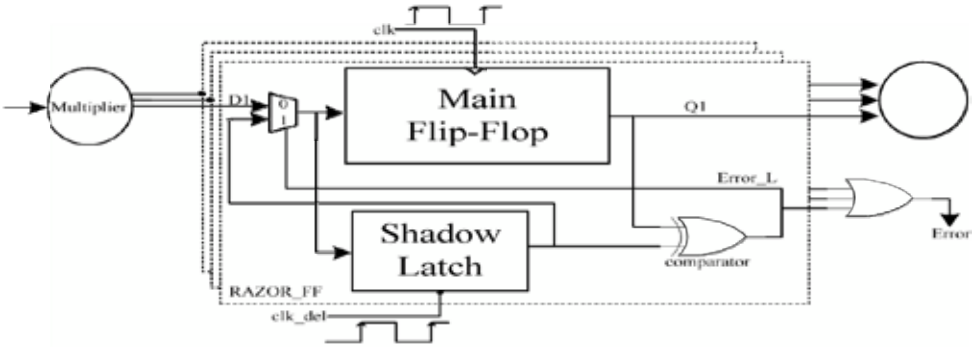

Fig .5. Razor flip-flop structure

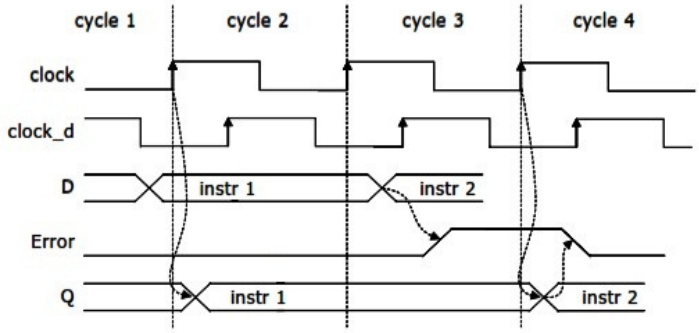

Fig. 6. Operation of Razor Flip-flop

3.5. Ahl Circuit

The AHL circuit is the key component in the aging-ware variable-latency multiplier. Fig. 7 shows the details of the AHL circuit. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect. The aging indicator is implemented in a simple counter that counts the number of errors.

These timing violations will be caught by the Razor flip-flops, which generate error signals. If errors happen frequently and exceed a pre-defined threshold, it means the circuit has suffered significant timing degradation

due to the aging effect, and the aging indicator will output signal 1; otherwise, it will output 0 to indicate the aging effect is still not significant, and no actions are needed.

The first judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (mr for the RBPM) is larger than *n*. If the number of zeros in the md (mr) is larger than *n*+1. They are both employed to decide whether an input pattern requires one or two cycles, but only one of them will be chosen at a time. In the beginning, the aging effect is not significant, and the aging indicator produces 0, so the first judging block is used. After a period of time when the aging effect becomes significant the second judging block is chosen. Compared with the first judging block, these judging block allows a smaller number of patterns to become one-cycle patterns because it requires more zeros in the multiplicand (mr).

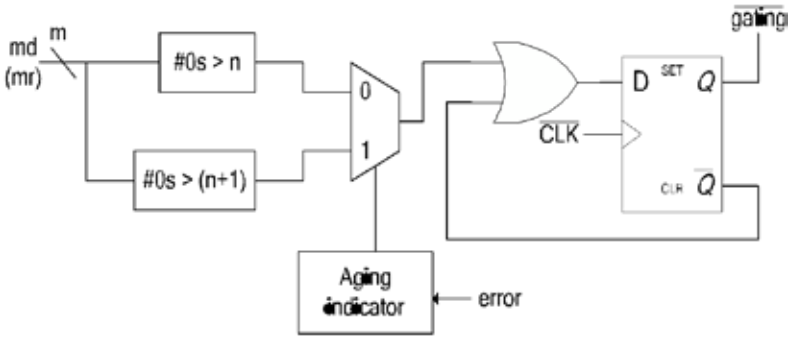

Fig. 7.AHL circuit

IV.PROPOSED METHOD

Aging Aware Reliable Multiplier's Operation

When input patterns arrive, the CBPM or RBPM, and the AHL circuit execute simultaneously. According to the number of 0's in the md (mr), the AHL circuit decides if the input patterns require 1 or 2 cycles. If the input pattern requires two cycles to complete, AHL will output 0 to disable the clock signal of the flip-flops. Otherwise, AHL will output 1 for normal operations. When the column or row bypassing multiplier finishes the operation, the result will be passed to the Razor flop-flop.

If timing violations occur, it means the cycle period is not long enough for the current operation to complete and that the execution result of the multiplier is in correct. Thus, the Razor flip-flops will output an error to inform the system that the current operation needs to be re-executed using two cycles to ensure the operation is correct. In this situation, the extra re-execution cycles caused by timing violation incurs to overall average latency. However, our proposed AHL circuit can accurately predict whether the input patterns require one or two cycles in most cases. Only a few input patterns may cause a timing variation when the AHL circuit judges incorrectly.

In summary, our proposed multiplier design has some key features. First, it is a variable latency design that minimizes the timing waste of the non critical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing violations and re-execute the operations using two

cycles. When the circuit is aged, and many errors occur, the AHL circuit uses these judging block to decide if an input is one cycle or two cycles.

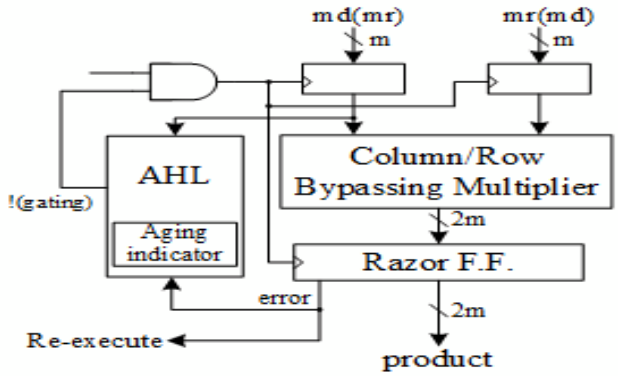

Fig. 8. Aging Aware Reliable Multiplier with AHL

V.SIMULATIONS AND RESULTS

A simulation result for Array Multiplier, CBPM, RBPM is simulated in a Xilinx ISE 9.2 and QUARTUS II 9.1 Web Edition. These tools will help to analyze its performance and calculate the power, delay (τ), total thermal power dissipation and core dynamic thermal power dissipation for all three.

For Reset = 1; Clk = 1; The error will be occur as the difference in data1 and data2 with respect to the normal and delayed clock for both md and mr bit. For the combination of 9*9 the output is 81 but here we obtain the result as 67 but after two clock pulse we get the actual value as 81 for a same input combination. This is shown in Fig. 9. Aging aware multiplier with missing data.

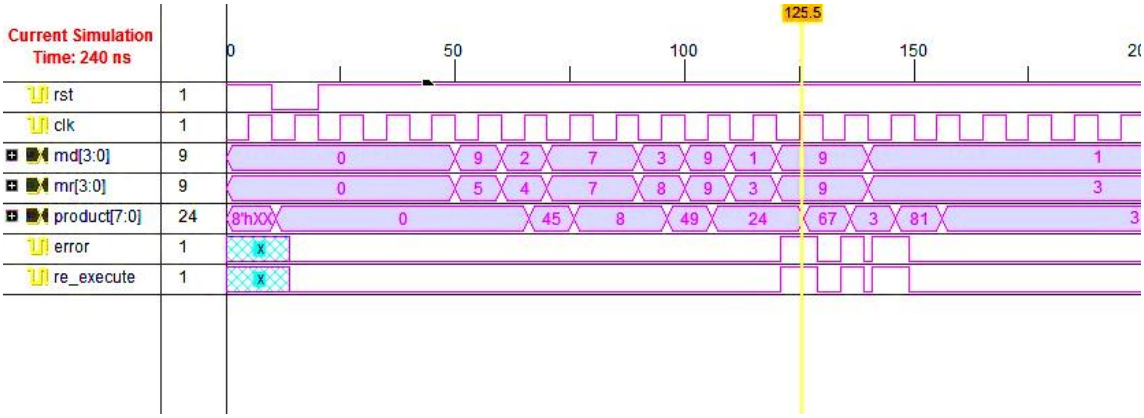

Fig. 9. Aging aware multiplier with missing data

The no of zeores in both multiplicand and multiplicator is calculated by using Xilinx as shown in Fig.10. No of zeroes for corresponding md bit.

Fig. 10. No of zeroes for corresponding md bit

Performance Comparison of AM, CBPM, RBPM

Performance Analysis of Array Multiplier, Column and Row Bypass Multiplier shown in Table.1

PERFORMANCE	AM	CBPM	RBPM
TOTAL COMBO LOGIC	32	31	40
MAX FAN-OUT NODE	b[1]	b[0]	b[2]
MAX FAN-OUT	9	10	12
TOTAL FAN-OUT	115	118	145
AVG FANOUT	2.40	2.51	2.59
DELAY	13.909ns	15.806ns	15.37ns
TOTAL THERMAL POWER	69.11mw	69.01mw	68.93mw
CORE DYNAMIC TPD	0.05mw	0.03mw	0.03mw

Table 1. Performance Comparison Between AM, CBPM, RBPM

VI.CONCLUSION

In this paper, we propose an aging-aware reliable multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. Note that in addition to the BTI effect that increases transistor delay, interconnect also has its aging issue, which is called electro migration. If the aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electro migration. In addition, our proposed variable latency multipliers have less

performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period. The pipeline error recovery mechanism must guarantee that in the presence of Razor-detected errors, an incorrect value does not corrupt register or memory state.

VII.NOMENCLATURE

CBPM -COLUMN BYPASS MULTIPLIER

RBPM - ROW BYPASS MULTIPLIER

NBTI - NEGATIVE BIAS TEMPERATURE INSTABILITY

PBTI - POSITIVE BIAS TEMPERATURE INSTABILITY

AHL - ADAPTIVE HOLD LOGIC

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BIOGRAPHICAL NOTES

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MULTI DOMINO DOUBLE MANCHESTER CARRY CHAIN ADDERS FOR HIGH SPEED CIRCUITS

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ABSTRACT

The carry look-ahead adders are designed till now by using standard 4 bit Manchester carry chain. Due to its limited carry chain length, the carries of the adders are computed using 4 bit carry chain. This leads to slow down the operation. A high speed 8 bit (MCC) adder in multi output domino CMOS logic is designed in this work. Due to its limited carry chain length this high speed MCC uses 2 separate 4-bit MCC. The 2 MCC namely odd carry chain and even carry chain are computed in parallel to increase the speed of the operation. This technique has been applied for the design of 8 bit adders in multi output domino logic and the simulation results are verified. Results prove that 8bit MCC produces less delay compared to conventional 4 bit delay. The reduced delay realizes better speed compared to the conventional designs. The existing design and the previous designs are designed and simulated using TANNER EDA.The delay of these designs is compared with 8 bit with 130 nm technology file. Implementation results reveal that the high speed comparator has delay of 41.64% less compared to the conventional designs

Keywords: Carry Look-Ahead (CLA) Adders, Manchester Carry Chain, Multioutput Domino Logic.

I. INTRODUCTION

Addition is the most commonly used arithmetic operationand also the speed-limiting element to make fasterVLSI processors. As the demand for higher performance processors grows, there is a continuing need to improve the performanceof arithmetic units and to increase their functionality. High-speed adder architectures include the carry look-ahead (CLA) adders, carry-skip adders, carry-select adders, conditional sum adders, and combinations of these structures. High-speed adders based on the CLA principle remain dominant, since the carry delay can be improved by calculating each stage in parallel.

II. FOUR BIT MCC

The 4-bit MCC is mainly used to reduce to computation time. The 4-bit MCC can perform the operation of 16 bit CLA. The MCC is mainly used to reduce the number of transistor count by using shared logic.

2.1 Domino Implementation for the Generate

The generate signal implemented in domino logic is shown in Figure 1. It consists of two inputs namely ai and bi and has one output gi. The two inputs are connected in series thus perform AND operation. Theoperation of

the circuit is controlled by clock signal. If the clock signal goes to value '0', then the circuit will enterinto precharge state and pmos will get connected to ground and output will maintain the value of 0. If theclock makes the transition from 0 to 1 then the circuit will enter into evaluation state and the outputdepends on the input value. Since generate signal possess AND operation.

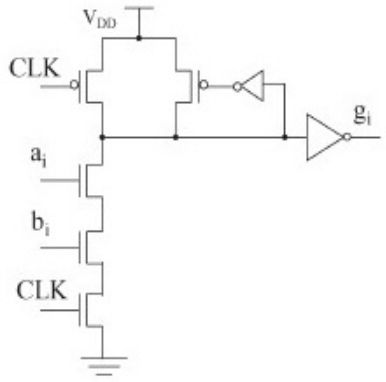

Fig. 1: Domino Implementation For the Generate

2.2 Domino Implementation for XOR Propogate

The propagate signal implemented in domino logic is shown in Figure 2. Here the propagate signal is implemented in XOR operation. The propagate circuit is controlled by clock signal. If clk goes to '0', then the circuit will enter into precharge state and the output remains in 0 value. If clk value is 1, then the output value depends on input value. Since this propagate signal is XOR operation based if both the inputs are different then output pi will maintain thevalue 1 else pi will have value 0.

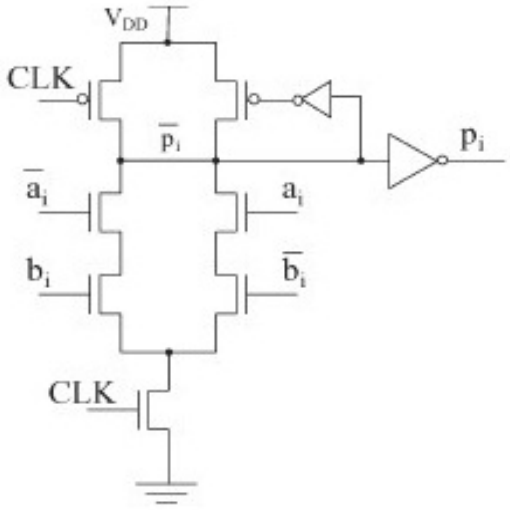

Fig. 2: Domino Implementation for XOR Propogate

2.3 Domino Implementation For OR Propogate

The propagate signal implemented in domino logic is shown in Figure 3. It consists of two inputs aI and bi and consists of one output signal ti. Here the propagate signal is implemented in OR operation.The propagate circuit is controlled by clock signal. If clk goes to '0', then the circuit will enter into precharge state and the output remains in 0 value. If clk value is 1, then the output value depends on input value. Since this propagate signal is OR operation based if any one of the inputs is 1, then output pi will maintain the value 1 else pi will have value 0

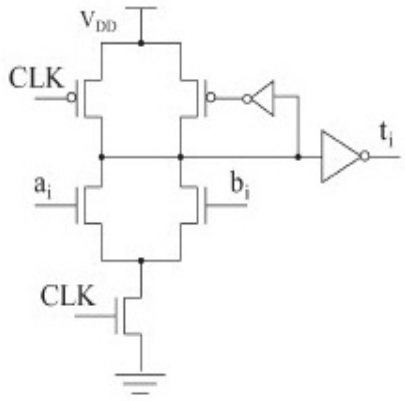

Fig. 3: Domino Implementation for OR Propogate

2.4 Conventional Four Bit MCC

Let A = $a_{n-1}a_{n-2}\cdot\cdot\cdot a_1a_0$ and B = $b_{n-1}b_{n-2}\cdot\cdot\cdot b_1b_0$ rep-resent two binary numbers to be added and S = $s_{n-1}s_{n-2}\cdot\cdot$ the computation of the carry signals is based on

$$c_i=g_i+z_i.c_{i-1} \qquad \text{(A)}$$

where$g_i = a_i \cdot b_i$ and z_i are the carry generate and the carry propagate terms, respectively

$$ci= gi+ zigi-1 + zizi-1gi-2 + \ldots + zizi-1 \ldots.z1g0+zizi-1 \ldots\ldots z0c-1. \qquad \text{(B)}$$

This conventional circuit consists of 4 bit two inputs namely p0, p1, p2, p3 and g0, g1, g2, g3. The operation of the circuit is controlled by clock signal. The input values are get from pi and gi values of the domino propagate and generate output values. If clock equals to '0', the circuit will enter into precharge state and no output will be obtained. If clock value is '1', then the output will depend on the input values. The inputs of propagate and generate signals from pi and gi willpossesses and the corresponding output carry signals namely c0, c1, c2, c3.

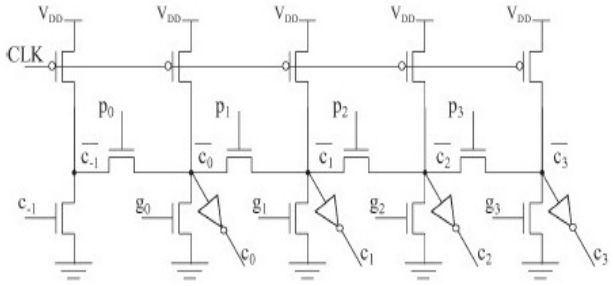

Fig. 4: Four Bit MCC

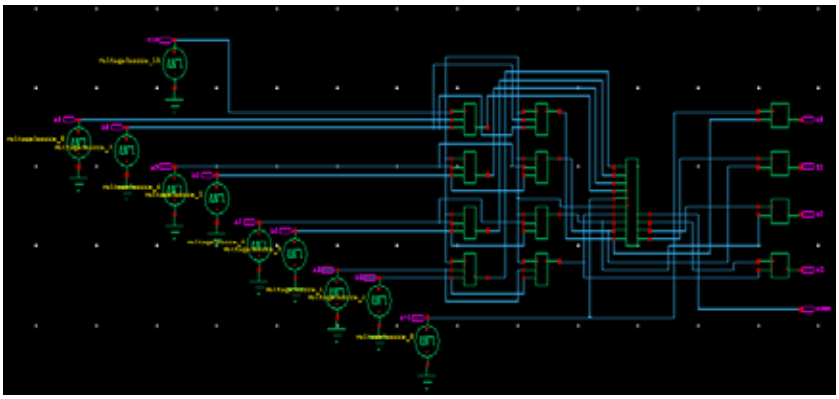

Fig. 5: Schematic Diagram for Four Bit MCC

III. EIGHT BIT MCC

The 8-bit MCC is mainly used to reduce the delay by increasing the speed. Here two 4-bit MCC is used and the carries are generate in parallel simultaneously. The use of the 8 bit adder as a basic block, instead of 4 bit MCC adder, can lead tohigh speed adder implementations. The derived here carry equations are similarto those for Ling carries equation. The derived carry equations allow the even carries separately of the odd ones. Implementation of the carries by two independent 4bit carries chains one chain computes the even carries, while the other chain computes the odd carries.

3.1 Implementation of Carry

Domino Logic implementation on of Carry Signals consists of two signals namely carry generate signal and carry propagate signals respectively. The Implementation of generate and propagate signals using domino logic

3.2 Even Carry Computation

This carry chain gets computed when input value has even values. Say i= 0,2,4,6. For the even input values say p0, p2, p4, p6 and g0, g2, g4, g6 the corresponding intermediate even carries say h0, h2, h4, h6 is obtained. The input values of propagate and generate signals are obtained from pi and gi respectively.

The even carries can be analytically given by

$$H2 = g2 + p2g0 \quad (1)$$

$$H4 = g4 + p4g2 + p4\ p2g0 \quad (2)$$

$$H6 = g6 + p6g4 + p6\ p4g2 + p6\ p4\ p2g0. \quad (3)$$

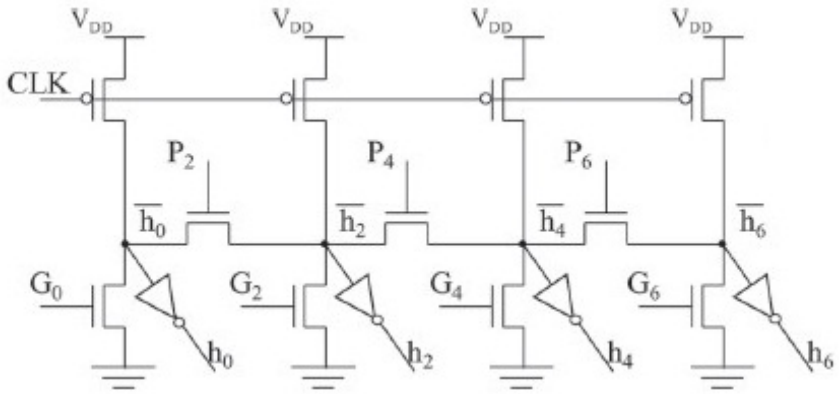

Fig. 6: Even Carry Computation

3.3 Odd Carry Computation

This carry chain gets computed when input value has odd values. Say i= 1,3,5,7. For the odd input values say p1, p3, p5, p7 and g1, g3, g5, g7 the correspondingintermediate odd carries say h1, h3, h5, h7 is obtained. The input values of propagate and generate signals are obtained from pi and gi respectively.

The odd carries can be analytically given by

$$H1 = g1 + pi\ .ci\text{-}1 \quad (4)$$

$$H3 = g3 + p3g1 + p3\ p1c\text{-}1 \quad (5)$$

$$H5 = g5 + p5g3 + p5\ p3g1 + p5\ p3\ p1g0. \quad (6)$$

$$H7 = g7 + p7g5 + p7\ p5g3 + p7\ p5\ p3g1 + p7\ p5\ p3\ p1c\text{-}1. \quad (7)$$

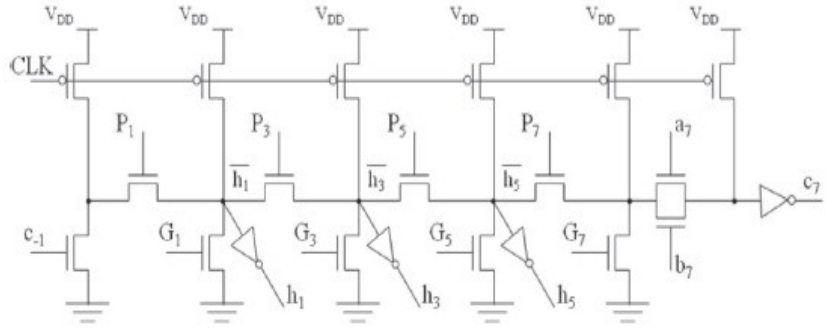

Fig. 7: Odd Carry Computation

3.4 Sum Bit Implementation

The sum has mux to selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output. A multiplexer is also called a data selector.when hi-1=0 it selects pi then hi-1=1 it selects piÅti-1

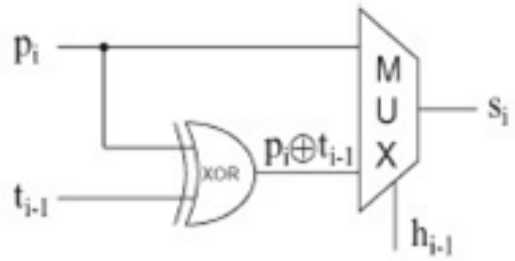

Fig. 8: Sum Bit Implementation

Fig. 9: Schematic Diagrm for Eight Bit MCC

IV.SIMULATION RESULTS

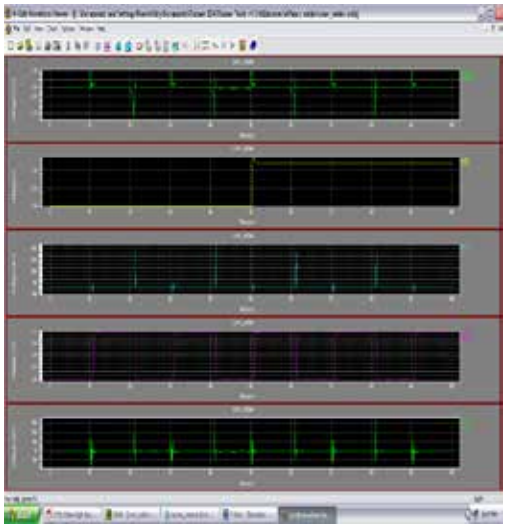

Fig. 10: OUTPUT FOR 4-BIT MCC

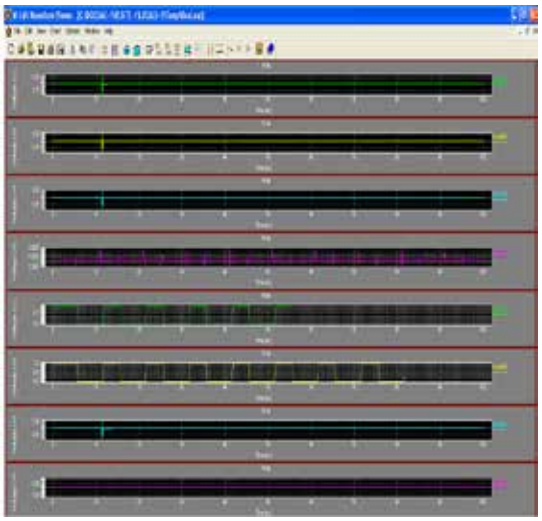

Fig. 11: OUTPUT FOR 8-BIT MCC

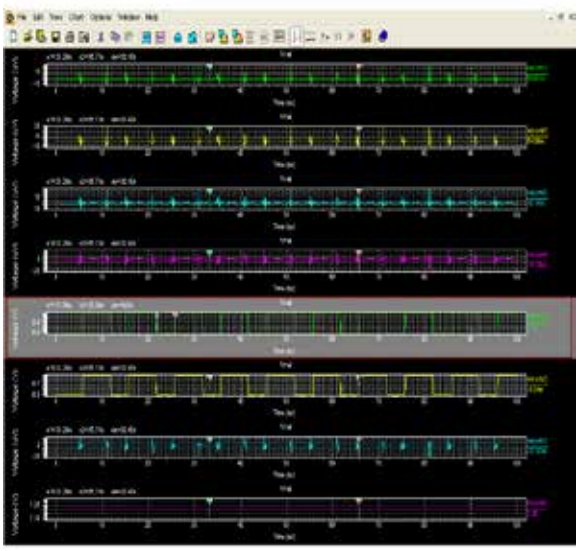

Fig. 12: DELAY IN 4-BIT MCC

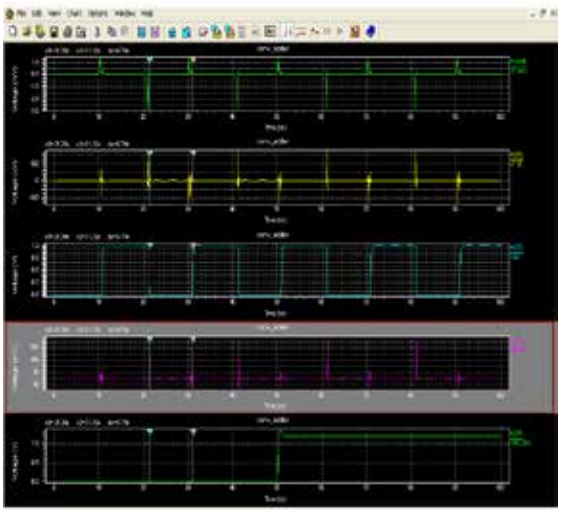

Fig. 13: DELAY IN 8-BIT MCC

4.1 Delay Reduction

Existing (4-bit MCC)	Proposed(8-bit MCC)	Delay percentage (%)
9.74(ns)	4.03(ns)	41.64%

Table 4.1 DELAY ANALYSIS

Delay reduction % = (9.74 - 4.03)/ 13.71 * 100 = 41.64%

V. CONCLUSION

An 8-bit adder is designed using Manchester carry chain. This circuitis designed and simulated using TANNER TOOLS software. This design realizes better improvement in reducing the delay by introducing parallelism concept in carry chains.To increase the speed of the operation by using two independent carry chain in parallel and thus reduces the time delay of the operation its performance is analysed by using 130nm with the supply voltage1.3v, 1.2v respectively. Thus, the proposed 8-bit Manchester carry chain is superior compared to 4-bit Manchester carry chain circuit.As a further work reducing the area of this chain and further reducing the delay by analyzing this design in submicron technology and implementing it in a variable bits like16 bit, 32 bit Manchester Carry Chain in multi output domino CMOS logic can be considered.

VI. NOMENCLATURE

CLA CARRY LOOK AHED ADDER
MCC MANCHESTER CARRY CHAIN
CMOS COMPLEMENTRY METAL OXIDE SEMICONDUCTOR
MOSFET METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

VLSI VERY LARGE SCALE INTEGRATED CIRCUIT

NM NANOMETER

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SURVEY ON METHODS OF PROTECTING COLOR INFORMATION BY HIDING IT

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ABSTRACT

Conversion from gray to color is known as colorization, this is the process of adding color to monochrome images such as old black and white photos, scientific illustrations etc. The widespread transmission of images and videos makes it necessary to find methods for securing images. Different methods are present for protecting colour information. This paper describes different approaches used. Some method uses color information hiding within the index image, some other methods hides color information in luminance image. A survey on four methods presented here.

Keywords: Index Image, Color Palette, Quantization, Layer Scanning Algorithm, Dwt.

I INTRODUCTION

The widespread transmission of images and videos often makes it necessary to find methods to secure them. For example, applications like confidential transmission, video surveillance, cultural heritage, military and medical applications need security functionalities. Data security thus becomes an important and integral component of modern day research on multimedia information.

Different methods are present for protecting color information. This paper addresses four of those methods.

In the next chapter first solution is palette based approach where color information is protected by hiding the color palette in index image. In that method the colors of the color palette are sorted to get an index image which is near of the luminance of the original color image. In the same time, consecutive colors in the color palette are close.

The other three methods are substitution based approach. These methods are based on wavelet decomposition and sub band substitution propose solutions to embed the color information in a gray level image. Their areas are image printing and perceptive compression. The second method concerned with color documents prepared digitally, which are to be printed using a black-and-white printer or transmitted using a conventional black-and-white fax machine. Therefore, the first problem is how to convert colors to black and white such that different colors would look different on paper too, even if they have the same luminance component. The second problem is the color-to-gray mapping should be reversible.

Third approach is about color embedding and recovery using a pseudorandomized saturation code based on a wavelet packet transforms to improve the color saturation of the recovered color image and preserve as many details

as possible from the original image. Fourth method proposes an accurate reversible algorithm without any distortion conditions such as a print-scan process for converting full color images to gray images while preserving the chroma and spatial resolution of the images.

II METHODS OF PROTECTING COLOR INFORMATION

The first method is palette based method. In this method low quality images are freely available but user need a key to get corresponding color image. Other three methods are substitution based approaches. In these methods the color information is protected by hiding it in corresponding luminance image.

2.1. Securing color information of an image by concealing the color palette

This paper presents a method to provide free Internet access to low quality images to all users and restricted access to the same images of better quality with the purchase of a key. That means a solution to give free access to gray level images whereas the user needs a key to view the corresponding image in color. The main objective of this method is thus to protect the color information of an image by embedding it in its corresponding gray level image.

The overview of the method is presented in Fig.1. To quantize the original color image, the luminance image is used in order to choose the number of colors, K $\in \mathbb{N}^*$. After quantization procedure, the color reordering algorithm is applied in order to get a reordered color palette and an index image close to the luminance image. The last step consists of embedding the color palette(message), in the index image(cover).

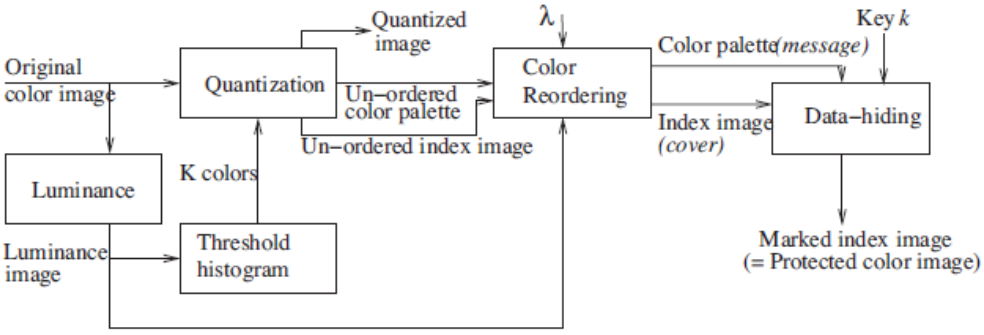

Fig 1: Overview of the method

2.1.1. Color quantization

Quantization means reducing the color number of a color image. The optimal solution, to extract the K colors from an image is obtained by solving Eq. (1):

$$\{P_{i,k}, C(k)\} = arg \min_{P_{i,k}, C(k)} \sum_{i=1}^{N} \sum_{k=1}^{K} P_{i,k}.d^2(I(i), C(k)),$$

$$\text{with } \forall i, \exists! k\prime, P_{i,k\prime} = 1 \text{ and } \forall k \neq k', P_{i,k} = 0, \quad \text{(1)}$$

where I is a color image of dimension N, C(k) is the kth color of the K searched colors, d() is a distance function in the color space, and Pi,k ∈ {0, 1} is the membership value of pixel i to color k. The constraint on Pi,k is that for all i there is a single k such that Pi,k = 1.

A solution to minimize Eq. (1), and then to obtain the K colors, is to use the ISODATA k-mean clustering algorithm. Pi,k is defined in Eq. (2):

$$\forall i, \forall k, P_{i,k} = \begin{cases} 1 & \text{if } k = \underset{\{k'\}}{arg}\{\min_{k' \in \{1,\ldots,K\}} d(I(i), C(k'))\}, \\ 0 & \text{else,} \end{cases}$$

$$\text{with } C(k) = (\sum_{i=1}^{N} P_{i,k} \times I(i))/(\sum_{i=1}^{N} P_{i,k}). \qquad \text{(2)}$$

In this approach, the number K is significant in comparison to the original number of colors. The problem with classical k-mean algorithm is, number of extracted colo

rs will often be below K, and is known as problem of "death classes". To overcome that problem, initialize the Pi,k values by solving the fuzzy c-mean equation given by Eq. (3):

$$\{P_{i,k}, C(k)\} = arg \min_{P_{i,k}, C(k)} \sum_{i=1}^{N} \sum_{k=1}^{K} P_{i,k}^{m} . d^2(I(i), C(k)), \qquad \text{(3)}$$

where m is a fuzzy coefficient (experimentally m is set at 1.6) and Pi,k are real values in the range [0, 1], named fuzzy membership values. Equation (3) is solved by a fuzzy c-mean algorithm. A quantized image is obtained once the quantization with K colors has been carried out. A color palette and its index image are associated with this quantized image. By applying just the quantization algorithm, the content of the index image does not semantically correspond to the luminance content of the original image. The color palette order should be changed to obtain an index image where its content are semantically close to the luminance content. Consequently the associated index image will change too.

2.1.2. Layer scanning algorithm

After color quantization, the K color image can be represented by an index image (based on Pi,k values) and a color palette (based on C(k) values). The index image is denoted index and is defined such that

$$\forall i \in \{1, \ldots, N\}, \text{index}(i) = arg \max_{k \in \{1,\ldots,K\}} P_{i,k}. \qquad \text{(4)}$$

The color palette is denoted palette and ∀k ∈ {1, . . ., K},

$$Pallette(k) = C(k)$$

The goal is then to find a solution by taking two constraints into account. The first constraint is to get an index image where each gray level is close to the luminance of the original color image. The second constraint is that two consecutive colors should be close in the color palette. The problem is to find a permutation function that simultaneously permutes the values of the index image and those of the color palette. The best permutation function is found by solving Eq. (5):

$$\Phi = \underset{\Phi}{\operatorname{argmin}} \left[\sum_{i=1}^{N} E_i^{ind} + \lambda \sum_{k=1}^{K-1} E_k^{palette} \right], \quad (5)$$

where E_I^{ind} (equation(6)) is the energy related to the index image and $E_k^{palette}$ (equation(7)) is the energy related to the color palette:

$$E_i^{\text{ind}} = d^2(Y(i), \Phi(\text{index}(i))),$$
$$E_k^{\text{palette}} = d^2(\text{palette}(\Phi^{-1}(k)), \quad \text{palette}(\Phi^{-1}(k+1)))],$$

where Y is the luminance of the original color image, and $\lambda \in R_+^*$ is a parameter controlling the weight assigned to the two energy terms. The Φ permutation function is a bijective function in N defined by $\Phi : \{1, \ldots, K\} \rightarrow \{1, \ldots, K\}$. The minimization of Eq. (7) is not feasible by using a derivative approach since Φ(·) and palette(·) are discrete functions. A metaheuristic approach could be used, such as evolutionist algorithms, for minimizing Eq. (5), but we prefer a less CPU consuming solution and a less memory costly solution. Eq. (5) is thus solved using an heuristic algorithm: the layer scanning algorithm. The aim of this algorithm is to find a reordering of K colors such that consecutive colors are close and the colors are reordered from the darkest to the lightest. This reordering defines, for each kth color, a k' position which gives the Φ function such that Φ(k) = k'.

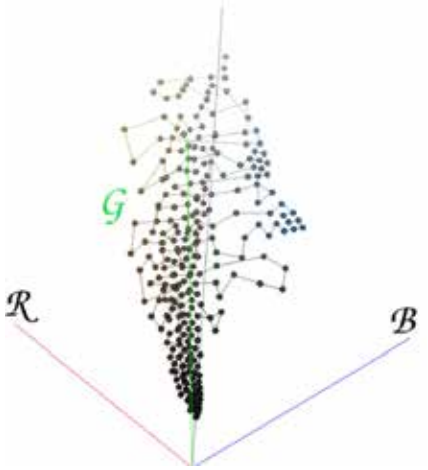

Fig 2: A view of the path built with the layer scanning algorithm in the RGB space.

To reorder the K colors, the algorithm scans the color space to build the reordered suite of colors. This scanning is obtained by jumping from color to color in the color space, and then choosing the closest color to the current one. The first color of this suite is chosen as the darkest one among the K colors. An additional constraint to this scanning is that the search is restricted to colors which are not too different in terms of luminance. This means that the scanning in the color space is limited to a layer defined on luminance information. This layer scanning algorithm could then be seen as a kind of "3D spiral scan" in the color space.

With the application of this layer scanning algorithm, we obtain a reordered color palette and its index image, which is semantically understandable. Note that the application of this algorithm does not change the informational

content. Indeed, this new color palette and the associated index image allow for the same color image to be built before and after processing the layer scanning algorithm. The energy shown in Eq. (6) is related to the index image as a function of the layer size. This energy is minimized when the layer size is small. For example, if the layer size is equal to 1 then the index image is built mainly as a function of the luminance of the palette colors. For the energy related to the color palette, Eq. (7), the variation as a function of the layer size differs from the previous one. In Eq. (5), parameter λ could give, as a function of its value, more importance to the color palette continuity or to the index image.

This layer running algorithm has an implicit hidden parameter which is the layer size used during the color running in the color space. Since our goal is to minimize Eq. (5), a satisfactory way to automatically set this parameter is to test all possible values for this layer size parameter and to keep the layer size value minimizing the equation. Knowing that the possible values of the layer size parameter belong to the range {1, . . ., K } and that it is very fast to make just one run in the color space, this gives an elegant and rapid solution to approximate Eq. (5).

Practically, λ depends on the parameter, $\alpha \in R^{*}_{+}$ given in Eq. (8):

$$\lambda = \alpha * \frac{N}{K - 1} \quad (8)$$

where N is the image size in pixels. With α set at 1, the same weight is given to the two constraints. With $\alpha \in [0,1]$, more importance is given to the luminance constraint, and inversely with ˛ greater than 1, more importance is given to the continuity of the color palette. Note that alpha is set by the user.

2.1.3. Color protection of an image by data-hiding

Embed data of the color palette into the index image. Spatial domain methods embed the information directly into the pixels of the original image. The main steps of this data hiding algorithm are the partitioning of the image into blocks of homogeneous size, the selection of one pixel in each block and the substitution of the gray level of each selected pixel by one of its two neighbors of the color palette. This is known as index substitution.

The objective of the data hiding step is thus to embed a message M made up of m bits b_j(M = b1b2 . . . bm). The embedding factor, in bit/pixel, is given by Eq. (10):

$E_f = m/N$ …….. (10)

The original index image is then partitioned into blocks of size $1/E_f$ pixels. Each block is used to hide only one bit b_j of the message. This partition procedure guarantees that the message is spread homogeneously over the whole image. In order to hide the data of the color palette within the image, m = 3 ×K×8 bits must be embedded in the index image. When K = 256 colors (which is the maximal value), the number of bits to embed is m = 6144 bits and, for an image of 512 × 512 pixels, the size of the blocks is 42 pixels and the embedding factor E_f = 0.0234 bit/pixel. To get an embedded pixel, $index_w(i)$, the selected pixel index(i) is then substituted by one of its two neighbors according to the message bit bj in order to preserve the best quality of the reconstructed image from the data-hidden image, as formalized by Eq. (11):

$index_w(i)$ =

$$\begin{cases} index(i) \; if \; bj = index(i) \bmod 2 \\ argmin \; (k \in [index(i)1, index(i)1] n \neq \{1 \ldots . k\})(palette(index(i) - palette(k))2 \; otherwise \end{cases}$$

……(11)

Thus, the index value index(i) is modified by +1 or −1 gray level when bj index(i) mod 2. The best choice for this modification is then to choose the closest color between palette(index(i) + 1) and palette(index(i) − 1) in order to minimize the distance to the color palette(index(i)). This way of embedding the color palette ensures that each embedding pixel can be modified only by one gray level and at the same time the reconstructed color pixel from the embedding image is very close to the original color value.

2.2. Color to Gray and Back: Color Embedding Into Textured Gray Images

Here approach is to map colors to textures. That is regions of different colors with similar luminance will look different after mapping because they would have different textures .Instead of having a dictionary (or palette) of textures and colors, it produces a continuum of textures that naturally switch between patterns without causing visual artifacts. For that, make use of the discrete wavelet transform (DWT), which decomposes an image into several subbands, each representing different spatial frequency contents. This wavelet-based mapping method works as follows.

2.2.1. Color Embedding

i. Convert image from RGB into YCbCr (or CIELab).

ii. Use a two-level DWT on Y , so that is divided into seven subbands:
Y à (S1,Sh1,Sv1,Sd1,Sh2,Sv2,Sd2)

iii. Reduce Cb and Cr by ½ , construct Cb+, Cb-, Cr+, Cr-, and reduce Cb- further to ¼ of its original size.

iv. Replace subbands
Sd1 ß Cb-; Sh2 ß Cr+; Sv2 ß Cb+; Sd2 ß Cr-

v. Take inverse DWT to obtain the textured gray image, i.e.,
(S1,Sh,Sv,Cb-,Cr+,Cb+,Cr-) à Y’

vi. Image Y’ is the resulting gray image and may be printed, which often includes scaling and halftoning.

2.2.2. Color Recovery

i. Read or scan the gray textured image.

ii. Determine image dimensions.

iii. If necessary, identify corners and carry an affine transform to de-warp the gray image.

iv. Reduce image to the correct resolution.

v. Use a DWT to convert the gray image into subbands
Y’ à (S1,Sh1,Sv1,Sd1,Sh2,Sv2,Sd2)

vi. Interpolate Sd1, doubling its resolution.

vii. Make Cb=|Sv2|-|Sd1|, and Cr=|Sh2|-|Sd2| .

viii. Interpolate Cb and Cr, doubling their resolutions.

ix. Remove the embedded subbands, i.e., set Sd1=Sh2=Sv2=Sd2=0, and take the inverse DWT transform to Y find as

(S1,Sh1,Sv1,0,0,0,0) à Y

x. Convert the Y, Cb, Cr planes back to RGB.

The reason to create positive and negative-valued chrominance planes is to avoid completely the color inversion problem depicted in Fig. 6. If a subband is supposed to have only positive values and we obtained negative ones, then it is a sign of texture inversion. Hence, one can take the absolute value of the subbands and recombine them into Cb and Cr as Cb=|Cb+|-|Cb-| and Cr=|Cr+|-|Cr-|.

2.3. Color Embedding and Recovery Using Wavelet Packet Transform with Pseudo randomized Saturation Code

This article proposes color embedding and recovery using a pseudorandomized saturation code based on a wavelet packet transform to improve the color saturation of the recovered color image and preserve as many details as possible from the original image. In the color-to-gray process, the Y image is divided into 16 subbands using a two-level wavelet packet transform. To minimize the loss of detail, the CbCr color components are then embedded into the two subbands with the minimum amount of energy in the Y image, where the selected combination of subbands is determined by investigating various combinations of eight subbands. Furthermore, to compensate the color saturation, the Cb and Cr components are scaled using the maximum and minimum values of the CbCr components from the original image. These values are embedded into the diagonaldiagonal (DD) subband and transformed into a pseudorandom code while considering the visibility in the resulting gray image. In other words, the pseudorandom code includes the maximum and minimum values of the CbCr components in original image and is expressed using numbers of white pixels. However, to reduce the degradation of details when using the pseudorandom code in the wavelet packet transform, the number of pixels is down sampled in the diagonal-diagonal subband. Finally, the ratio of the original CbCr values to the extracted CbCr values is applied to enhance the saturation of the recovered color image.

The method used to recover the colors from the new gray image with texture is the reverse process of the above color-to-gray algorithm.

2.3.1. Subband Selection for Embedding CbCr

Figure 3 shows the subband locations selected for embedding the CbCr components.

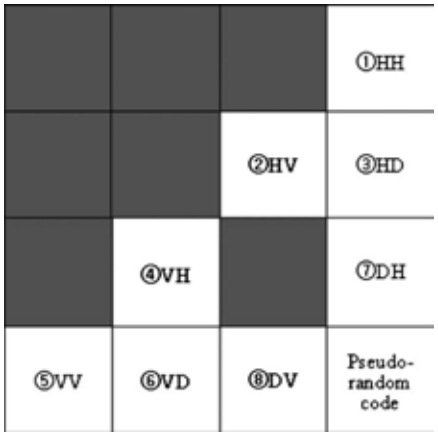

Fig 3: Subband locations for embedding the CbCr components.

Here, eight candidate subbands were selected: the horizontal-horizontal (HH), horizontal-vertical (HV), horizontal-diagonal (HD), verticalhorizontal (VH), vertical-vertical (VV), vertical-diagonal (VD), diagonal-horizontal (DH), and diagonal-vertical (DV) subbands. The seven subbands in the dark region in Fig. 3 were excluded, as they included relatively much more information on the original image than the other subbands. The DD subband was also excluded, as it was used to embed the pseudorandom code to compensate for the color saturation. Thus, the eight candidate subbands yielded 28 possible combinations of two subbands for embedding the CbCr components. The subbands used to embed the Cb and Cr components are selected based on their color difference in CIELAB color space and peak signal-to-noise (PSNR) values. Thus, the color differences in CIELAB color space and PSNR values were calculated as follows:

$$\Delta E^{*}_{ab} = (\Delta L^{*2} + \Delta a^{*2} + \Delta b^{*2})\wedge(\frac{1}{2})$$

where

$$\Delta L^{*} = L2 - L1, \quad \Delta a^{*} = a2 - a1, \quad \Delta b^{*} = b2 - b1$$

$$PSNR_k = 20\ log_{10}\left(\frac{255}{\sqrt{MSE_k}}\right), k = R, G, B$$

Where

$$MSE_k = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}\|O_k(i,j) - R_k(i,j)\|^2$$

The combination of two subbands that resulted in the best performance as regard to the color difference and PSNR value depended on the image. The best color difference and PSNR value were obtained when using combinations among the HV, VH, DH, and DV subbands possibly because they included the minimum information on the original image. Therefore, combinations of two subbands among the HV, VH, DH, and DV subbands produced the best recovered color image, the CbCr components were always embedded into the HV and VH subbands. To reduce the interpolation errors in the gray-to-color process, one-quarter of the CbCr images can be used instead of onesixteenth of the individual CbCr images. The quarter-sized CbCr images are divided into four regions of the same size instead of down sampling to one-sixteenth of the size CbCr images. Each separate region of the Cb image is then embedded into the DH, HH, HV, and HD subbands. Meanwhile, each separate region of the Cr image is embedded into the

DV, VH, VV, and VD subbands, respectively. Next, an inverse wavelet transform is applied to obtain a textured gray image.

2.3.2. Embedding a Pseudorandom Code for Compensation of Saturation

When a textured gray image is printed and scanned, the pixel values (eight bits: 0–255) of the textured gray image are invariably changed by the inherent characteristics of the printer and scanner. This effect leads to a loss of color saturation in the recovered color image as the values of the embedded CbCr components are also changed in the printing and scanning process. Thus, to enhance the color saturation of the recovered color image, the CbCr components were scaled using the maximum and minimum values of the CbCr components of the original image. When using the ratio of the original CbCr values to the extracted CbCr values, the color saturation of the recovered color image can be enhanced. Therefore, this information is transformed into a

pseudorandom code, considering the visibility of the textured patterns on the new gray image, and then embedded into the DD subband.

2.3.3. *Generation of Pseudorandom Code*

The pseudorandom code is expressed by the number of white pixels according to a given code book, and the location of each pixel is chosen pseudorandomly. First, an image is generated that is the same size as each wavelet packet subband. This image is then divided into 16 regions with 4×4 blocks of the same size, and the subband pixel values are set to zero. Next, the pseudorandom code is generated using the maximum and minimum values of the CbCr components. Although the range of CbCr values is generally −128–+127, the range may be changed to −64–+63 to allow more effective representation of the CbCr information by the pseudorandom code. Next, the tens digit is separated into two parts, while the units digit is divided by a factor of 2. As a result, the first row of the pseudorandom code represents the sign information, the second and third rows represent the tens digit information, and the last row represents the units digit information. Meanwhile, the first and second columns of the pseudorandom code are the maximum and minimum Cb values, respectively, while the third and last columns are the maximum and minimum Cr values, respectively.

Registration and geometric distortions are problems addressed in this method. The next method solves this.

2.4. Accurate reversible color-to-gray mapping algorithm without distortion conditions

This paper propose a new color-to-gray mapping algorithm and a color recovery method that preserves the chroma and the spatial resolution of the original image without distortion conditions.

2.4.1. Color-to-gray conversion

This method works as follows:

step E1: Convert images from RGB to YCbCr.

Step E2: One-level discrete wavelet transform on the luminance Y.

Y à (Sl, Sh1, Sv1, Sd1)

Step E3: Reduce Cb and Cr by 1/16, construct Cb+, Cb_, Cr+, and Cr_ where Cb is resolved into two components depending on whether its sign is positive or negative by the following equations:

$$Cb+ = \begin{cases} Cb, & Cb > 0 \\ 0, & Cb \leq 0 \end{cases}$$

$$Cb- = \begin{cases} Cb, & Cb < 0 \\ 0, & Cb \geq 0 \end{cases}$$

The same arrangement is made for Cr.

Step E4: Multiply b(0 < b 6 1) by the chrominance components Cb+, Cb_, Cr+, and Cr_. Hereafter, this process is referred to as a simple scaling so called b-transform.

Step E5: Each subband Sh1, Sv1 and Sd1 is composed of blocks that consist of 2 × 2[pixels]. In the case of the horizontal subband Sh1 and the vertical subband Sv1, one pixel in the block is replaced by the chrominance component of the corresponding position to obtain Sh1' and Sv1', respectively. In the case of the diagonal subband Sd1, two pixels in each 2 ×2 block are replaced by the corresponding chrominance components to obtain Sd1'.

Step E6: Replace subbands

Sh1 ß Sh1'; Sv1 ß Sv1'; Sd1 ß Sd1'

Step E7: Take the inverse discrete wavelet transform to obtain the textured gray image, i.e.,

(Sl, Sh1', Sv1', Sd1') à Y

2.4.2. Recovery step

Step R1: Read the gray textured image.

Step R2: Use a discrete wavelet transform to convert the gray image into subbands:

Y' à (Sl, Sh1', Sv1', Sd1')

Step R3: Obtain Cb-',Cr+',Cb+' and Cr-' from subbands Sh1', Sv1' and Sd1'.

Step R4: Estimate the high-frequency components of the color-embedded pixels in subbands by interpolation. Obtain Sh1" by interpolating the color-embedded pixels in Sh1' in the vertical direction. Obtain Sv1" by interpolating color-embedded pixels in Sv1' for horizontal direction. Make Sd1" by interpolating the color-embedded pixels Sd1' as the mean value of two high-frequency components in a 2 ×2 block.

Step R5: Use an inverse discrete wavelet transform to recover Y"

(Sl, Sh1", Sv1", Sd1" à Y"

Step R6: Multiply 1/b by Cb-'; Cr+'; Cb+', and Cr-'.

Step R7: Obtain Cb" from Cb+' and Cb-', and Cr" from Cr+' and Cr-'. Then Interpolate Cb" and Cr" linearly,by quadrupling their resolutions.

Step R8: Convert the Y" , Cb" , and Cr" planes back to RGB.

This method is constructed on the basis of wavelet transforms and the chrominance information is embedded into the wavelet subbands. The power in the high-frequency subbands Sh1, Sv1 and Sd1 is smaller than that in the low-frequency components. In this algorithm, the chrominance components Cb+, Cb_, Cr+ and Cr_ are spatially distributed and embedded in the above one-level wavelet subbands Sh1, Sv1 and Sd1 effectively. Two chrominance

components are embedded in subband Sd1, because power of Sd1 is generally the smallest among the high-frequency subbands.

III CONCLUSION

In this chapter, we proposed different methods for protecting color information. One palette based approach and three substitution based approaches are discussed. Protecting the color information providing a degraded gray-level image, and a rebuilt color image of good quality is possible. Improvements are possible by mixing the different approaches or with prior knowledge from embedding and extracting side.

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OPTIMIZATION OF THE SOLVENT EXTRACTION RATE AND EXTRACTION EFFICIENCY CONSIDERING FLOW RATE, HEATING RATE, AND SOLVENT CONCENTRATION

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ABSTRACT

Raw cashewnut shell contains around 20 percent oil. When cashewnuts are processed by oil extraction process, about 50 percent oil is extracted. Balance oil (or liquid as it is known) can be further extracted with the help of expellers. This note primarily deals with this kind of processing. Solvent extraction is one of the favored separation techniques because of its simplicity, speed, and wide scope. By utilizing relatively simple equipment and requiring a few times to perform, extraction procedures offer much to the chemists and engineers. Using solvent extraction, important theoretical problems concerning the composition and stability of soluble as well as insoluble complexes can be solved. This paper shows the solvent extraction of cashew nut shell particles using hexane and methanol as solvent. The effect of temperature and solid-liquid ratios had positive influence on extraction rate and extent of extraction which gave the possibility for estimation of initial rate and extent of solid liquid extraction.

Keywords: Cashew Nut Shell Particles, Extraction Rate, Solvent Extractor, Solid-Liquid Ratio, Temperature.

I. INTRODUCTION

As the fossil fuels are depleting day by day, the need for alternate source of energy is atmost concern to our society. As we know that there are various methods for obtaining energy from renewable sources of energy but some of them have found some complications and are economically not feasible for our society. There are many sources of producing energy from renewable sources but it is of great importance to note that biofuels from edible and non edible oils or seeds can be considered as an important source of producing fuels i.e. biofuels which can be converted into biodiesel further and used as fuel in ICengines [3, 5, 7]. Biodiesel from edible oil is not feasible in India because of a big gap between the supply and demand. Plants like Jatropha (*Jatropha curcas*), Mahua (*MadhucaIndica*), Karanja (*Pongamia pinnata*) and Neem *(Azadirachta indica)* contain 30% or more oil in their sees or fruit [9]. Cashew nut (*Anacardium occidentale*) shell liquid (CNSL) is a unique natural source for

unsaturated long-chain phenols .Obtained as a byproduct of the cashew industry, this renewable material has wide applications in the form of brake linings, surface coatings, paints, and varnishes. The main applications of CNSL are in the polymer industry. Compared with conventional phenolic resins, CNSL polymer has improved flexibility (due to the internal plasticization effect of the long chain) and thus betters process ability. The side chain imparts a hydrophobic nature to the polymer, making it water repellant and resistant to weathering. CNSL-based resins possess outstanding resistance to the softening action of mineral oils and high resistance to acids and alkalis. CNSL polymers also have useful characteristics such as heat and electrical resistance, antimicrobial properties, and termite and insect resistance [4]. India being one of the biggest producer and consumer of cashew it becomes very easy for using the cashew nut shell for producing biofuel and biodiesel [6]. CNSL can be extracted by various methods such as hot and cold method [8].

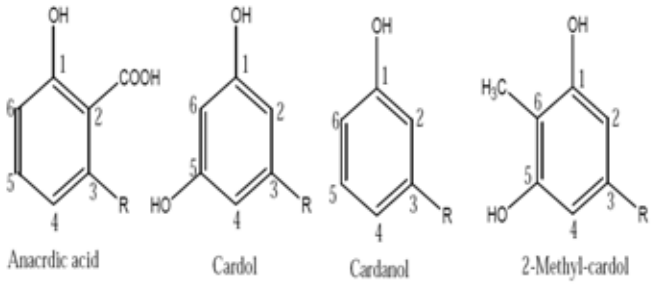

Fig. 1.Structure of main components of CNSL

II. SOLVENT EXTRACTION

This method gives most of CSNL compared to other methods. Extraction solvent may be less dense or denser than water. Hexane and toluene are denser than water and they have a greater tendency to extract oil from the cashew nut shell particles [1]. This method gained its popularity in the recent years as a popular separating technique because of its simplicity, elegance, speed and its wide scope. It has become a very powerful and effective unit of operation in most of the industries. It is a very simple operation apparatus without any sophistication or instrumentation. This unit finds its application in most of the industries such as chemical, metallurgy, nuclear, petrochemical, pharmaceutical as well as in waste management [2].The extraction of CNSL was carried out using a Soxhlet extractor and n-hexane as solvent. Four hundred and fifty milliliters (450ml) of hexane was charged into the round bottom flask of soxhlet apparatus. Subsequently, 60 gram of crushed cashew nut shell was charged into the thimble and fitted into the soxhlet extractor. The apparatus was assembled. The solvent in the set-up was heated to 68^{o}C and the vapor produced was subsequently condensed by water flowing in and out of the extraction set-up. This process of heating and cooling continued until a sufficient quantity of CNSL was obtained. The mixture of hexane and cashew nut shell oil was fed into a vacuum rotary evaporator and the solvent was recovered thus separating the biofuel and solvent. The recovered solvent was used again in the solvent extraction process. The experiment was performed for three hours eight minutes and twenty five siphons were observed so that a sufficient amount of CNSL is extracted. 18 gm of cashew nut shell oil was obtained which is 30percent yield. Similar experiment was also carried out by taking methanol as solvent.

III. EXPERIMENTAL SETUP AND WORKING PRINCIPLE

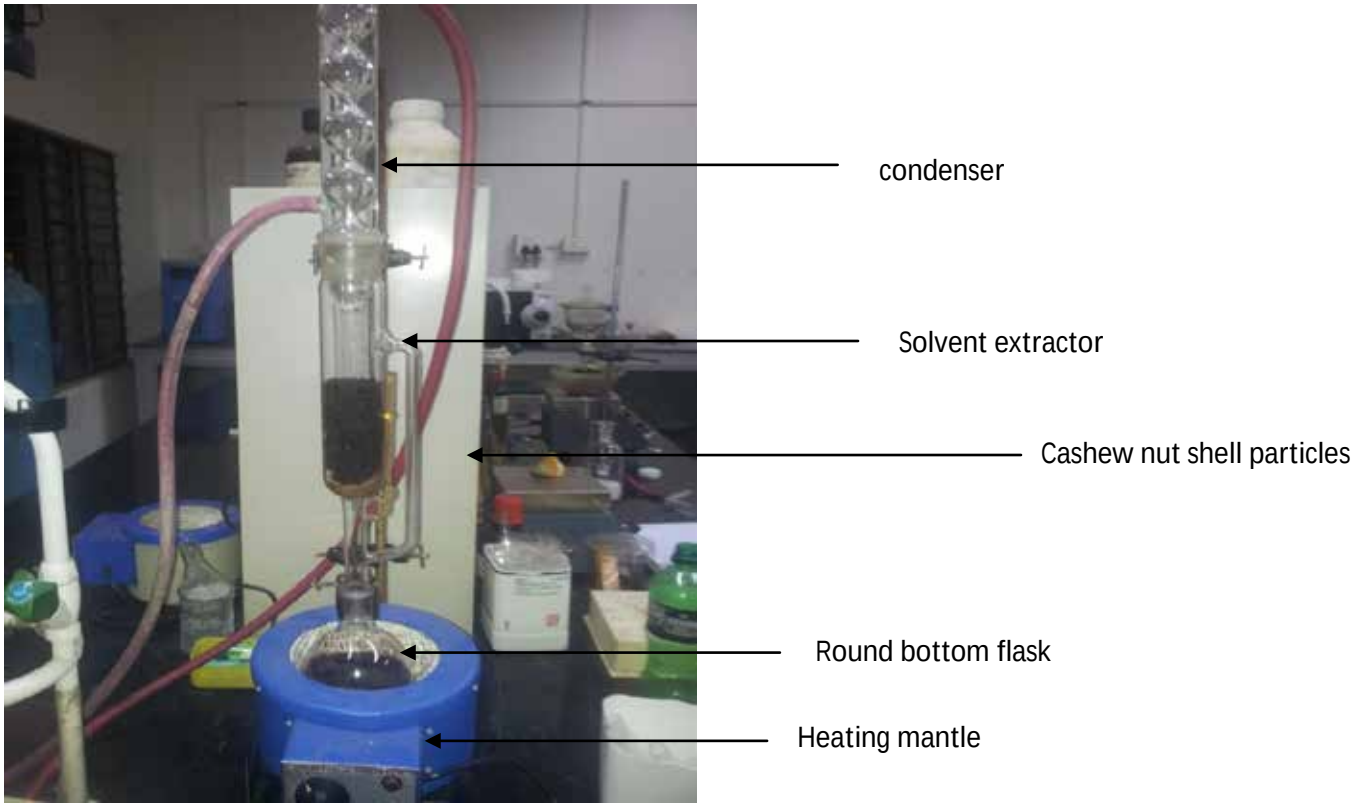

Fig. 2. Components of the solvent extractor

The set up mainly consists of a round bottom flask an extractor and a condenser. The solvent is fed into the round bottom flask and the sample is kept in the extractor which is in the mid position. The round bottom flask is heated by a heating mantle which is connected to the ac supply. When the solvent in the round bottom flask gets heated up to its boiling point then the vapors of the solvent starts rising up and passes through the condenser and condenses the solvent vapor which falls into the sample present in the extractor i.e. the cashew nut particles. When the level of condensed vapor increases then it comes out of a tube which carries the liquid from a higher level and up and over a barrier and down to the round bottom flask. This siphon continues when the level of liquid inside the extractor increases. After sufficient number of siphons the required amount of biofuels is obtained and thus the experiment continues with the same process. After the extraction is over the mixture of the solvent and fuel is fed into a vacuum rotary evaporator for separating the mixture and the solvent is recovered for further use in the solvent extraction process.

3.1 Experimental Results

Amount of n hexane in the round bottom flask	450milliliters

Amount of cashew nut shell particles	60 grams
Amount of biofuel obtained	18 grams
Percentage yield	30 percent
Total time taken for the experiment	3hours and 8 minutes

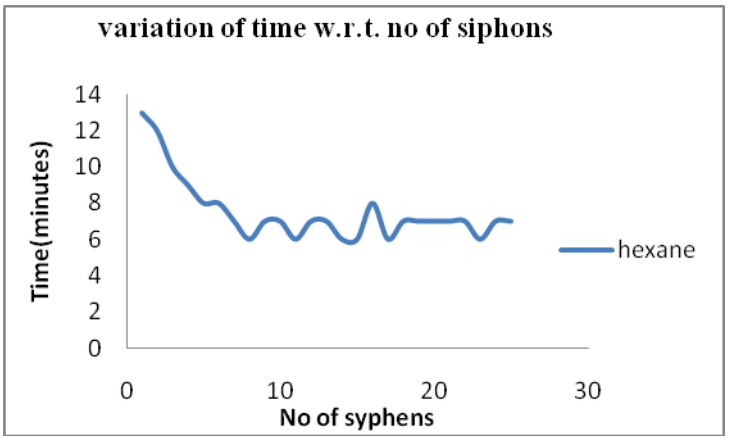

Fig. 3.Variation of time w.r.t. number of siphons using hexane as solvent

Amount of methanol in the round bottom flask	500milliliters
Amount of cashew nut shell particles	70 grams
Amount of biofuel obtained	17.5 grams
Percentage yield	25 percent
Total time taken for the experiment	5 hours 32 minutes

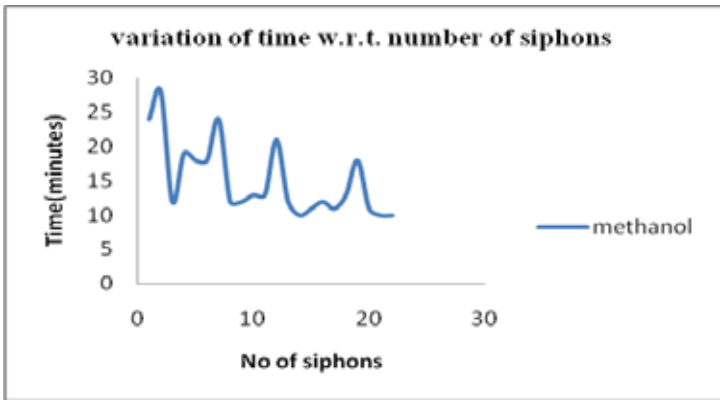

Fig. 4. Variation of time w.r.t. number of siphons using methanol as solvent

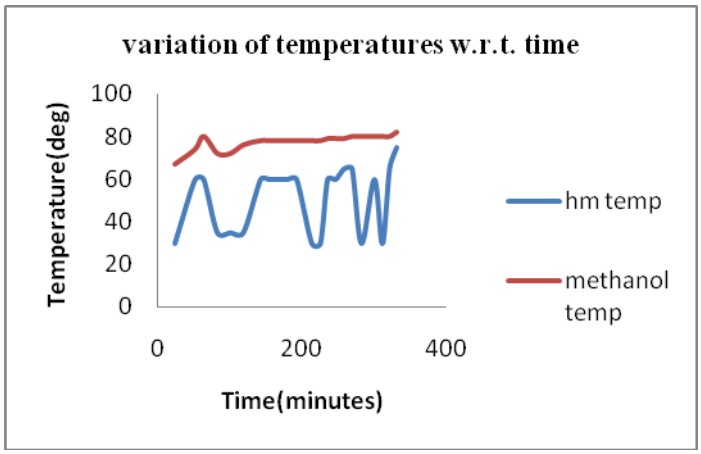

Fig. 5. Variation of methanol temperature and heating mantle temperature w.r.t. time

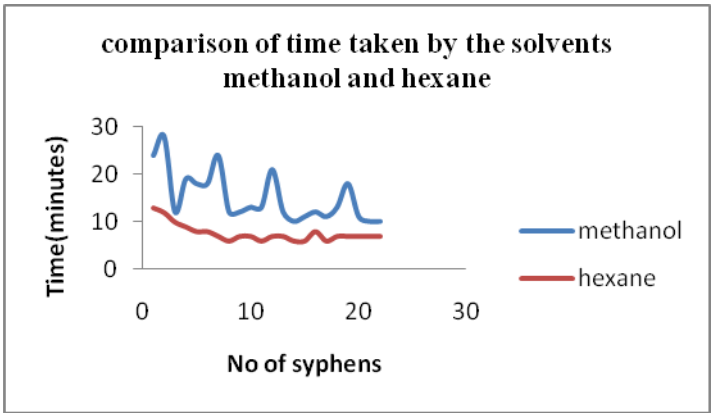

Fig. 6. Comparison of the time taken for both the solvents i.e. hexane and methanol for solvent extraction

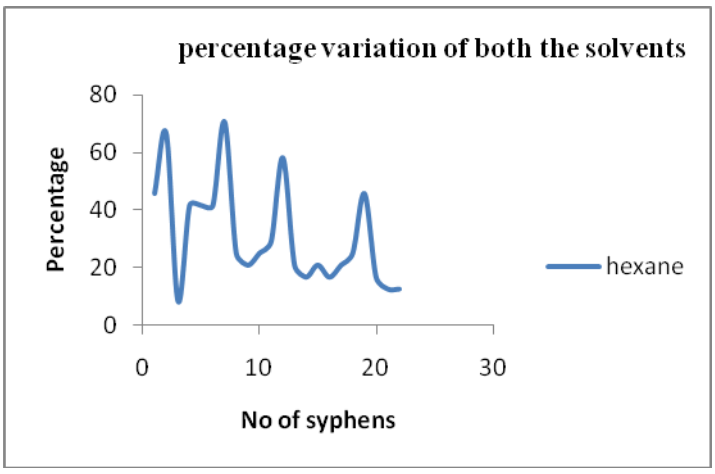

Fig. 7. Percentage variation of the solvent hexane w.r.t. methanol

3.2 Discussion

Fig. 3 shows the time taken by hexane w.r.t. the number of siphons which is less compared to the time taken by methanol as shown in the Fig. 4. Thus we can say that hexane is a better solvent for extraction process and the yield of extraction is also more than that of methanol.Fig. 5 shows the temperature of the heating mantle and the temperature of the solvent methanol. When heating mantle is at a particular temperature the solvent temperature attains some value due to which the boiling of the solvent starts and vapor starts moving upward towards the condenser. At a particular time the temperature attains an equilibrium value for which the heating mantle temperature is slightly maintained at a lower temperature than that of the solvent. There is always a temperature difference between the solvent and the heating mantle. If same temperature is maintained in both the solvent and the heating mantle than the wall of the extractor gets heated up and no siphon occurs. Further the condensed vapors when fall on the cashew shell nut particles the temperature of the liquid falling in the round bottom flask decreases for which an increase in the heating mantle temperature is required. Continuously siphons occur and maximum amount of biofuel is extracted from the sample.Fig. 7 shows the percentage variation of the solvent hexane w.r.t. methanol. It can be clearly seen that the percentage of hexane for the siphon to occur in less amount of time is more than that of methanol. In every siphon it is observed that the solvent hexane requires less amount of time to perform the extraction as compared to methanol thus making hexane a good solvent.

IV. CONCLUSION

The experiments carried out showed that the extraction of oil from the cashew nut using hexane as solvent is much more effective than methanol. Moreover methanol takes much more time in extraction process than hexane and the quantity of biofuel obtain from hexane is 30percent compared to methanol which is 20 to 25 percent. As shown in the Fig. 7 the number of siphons being constant the extraction rate is much more in case of hexane than that of methanol. Solvent extraction by means of soxhlet apparatus has a positive attribute because of the use of limited quantity of solvent more amount of oil can be extracted in a shorter time. This extraction technique is better than the conventional mechanical expeller method as some amount of oil still remains in the cashew nut shell particles after taking out of the mechanical expeller which can be extracted using solvent extraction process.

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STRUCTURAL ANALYSIS OF THE EXHAUST GAS SILENCER FOR THE FLOW THROUGH PERFORATED AND NON-PERFORATED SILENCER

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ABSTRACT

To minimize unwanted noise, the exhaust gas of high pressure and high temperature coming out of internal combustion engine passes through silencer. Various types of silencers like absorptive, reactive and resonating, perforated type are widely implemented in actual practice .perforated reactive mufflers have an effective damping capability. This paper deals with comparative structural analysis of such automobile silencer of both perforated and non-perforated one. Here, geometrical model of perforated and non-perforated silencers has been designed. The analysis of the models for the deformation, stress and strain the were analyzed using ANSYS WORKBENCH 14.0. Boundary Element Method had been adopted for the design analysis for a comprehensive comparative analysis on silencers of perforated and as well as non-perforated type.

Keywords: Deformation, Non-Perforated, Perforated, Silencer, Strain, Stress.

I.INTRODUCTION

The motion of the piston engine and compressor the associated intake and discharge of the gases are responsible the noise vibration and sound pollution and major pollution due to exhaust gases. When this exhaust gases passes through a muffler, then there is large pressure difference between the inlet and outlet of the muffler.If a vehicle which not have a muffler or silencer than it make very much noise due to high level difference of frequencies of sound. This noise is undesirable; and unwanted. To reduce this noise arising out the exhaust from internal combustion engine, mufflers are indispensible device in order to adopt with the stringent environmental regulations. The undesirable noise is known as noise pollution. A pollution is creates more disturbance the environment. Noise is measured in decibel. Audible waves are of frequency ranges from 20 Hz to 20000 Hz. The audible frequency of dog is 15 Hz to 50000 Hz. The aircraft is making more noise. Muffler containing more pressure hence sound is in the pressure waves forms. Because there high difference of pressure in the automobile muffler. Hence there stress, strain, deformation occurs at the silencer body.

Munjal [1] has done a descriptive analysis on design of the mufflers. In his report, he elaborated the main reason noise and vibration generated from of reciprocating engine. His design of muffler has been developed on the basis of experimental trial and error, as well as on the basis of electro-acoustic analysis on passive muffler using impedance mismatch of dissipative or reactive muffler. The main principal of the automobile industries muffler is conservation of acoustic energy into heat by means of highly porous-fibrous linings, called dissipative

automobile muffler. The main purpose of the silencer there passes the high pressure heat, ventilation and air condition system. The automobile is working in vibro-acoustic hoses used in automotive weather control. Automobile main component muffler it creates noise pollution as well as air pollution.

Shital et al. [2] have worked on a practical approach on novel design of automobile muffler with prototype validation. This new area of the muffler and most advances related to the muffler of acoustic filter analysis. The complex design of the muffler it mostly affects the behavior of the acoustic gases like emission, vibration and fuel efficiency of the engine. The muffler play important role to reduction of the noise. They develop a model in modern take analysis in modern tool CAE and optimize the design with respect to requirement refer like noise and back pressure.

Bartlett et al. [3] have worked on modeling and analysis of the variable geometry of the engine exhaust system.In engine exhaust system, gases are generating very high pulsating due to its variation of pressure, temperature and velocity. Hence for their analysis, the variable geometry of the muffler had been taken into consideration.

Na et al. [4] simulated the scattering of acoustic plane waves at a sudden area expansion in the duct without flow, using a linearized Navier Stock equation solver in frequency domain. Their results on acoustic catering were based on wave decomposition techniques with good decision. Their analytical model for flow through the duct of the pipes, proposed the scattering of waves at the different area of discontinuity with the sharp edges. Sound wave of the scattering varies with cross-section. With a cited example Na et al. [4] considered a 3-D duct model having rectangular cross-section with expanding area, and simulated it for the flow of the downstream.

Patekar et al. [5] have theoretically modeled the exhaust silencer of a two wheeler using Finite Element Method (FEM)and experimentally validated using Fast Fourier Transform(FTT) analyses. The modal analysis for the six frequencies and compared with the natural frequency. In accordance with their study, it was noticed that the dynamic performance could be increased with increasing thickness of various parts.

II. THE BOUNDARY CONDITION OF THE MODEL

The silencer has the boundary condition inlet temperature, outlet temperature, inlet pressure, outlet pressure and also includes the fixed supports like holding the silencer.

III GERMETRIC MODEL OF THE SILENCER

In paper here included two types of the geometrics model one is the perforated model as shown in the fig no 1. Second geometric model is the non-perforated model as show in fig no 2.the both geometric model have the same dimension but only the difference perforation.

GEOMETRIC MODEL

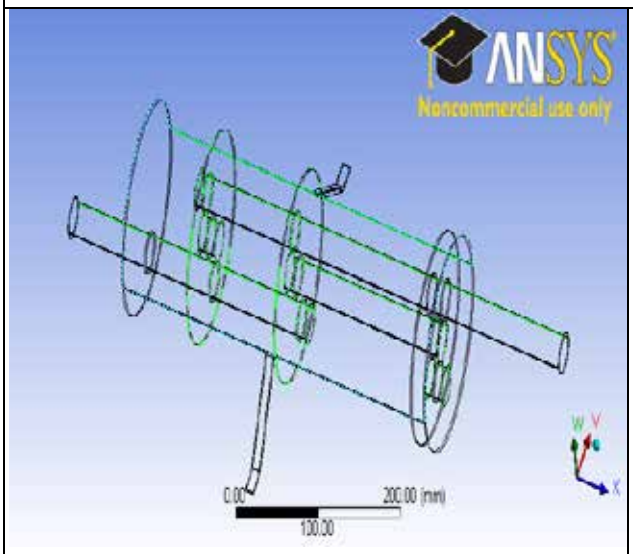

FIG. 1:NON-PERFORATED MODEL

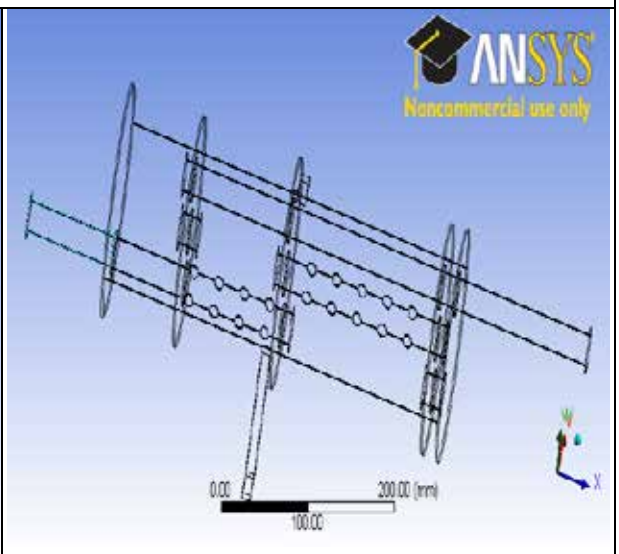

FIG. 2: PERFORATED MODEL

VI. RESULT ANALYSIS

In this paper, it has been discussed about the structural analysis of the both types of the silencer model. In the structural analysis includes the von Mises stress, von Mises strain and the total deformation. The deformation for non-perforated silencer model as show in the fig no.3 and thefor the perforated silencer the total deformation is show in the fig no. 4. The equivalent von Mises stress for the non-perforated silencer model show in the fig. 5 and for the perforated silencer model. The elastic strain is show for the both silencer model fig.7 for the non-perforated and the fig.8 for the perforated silencer.

TOTAL DEFORMATION

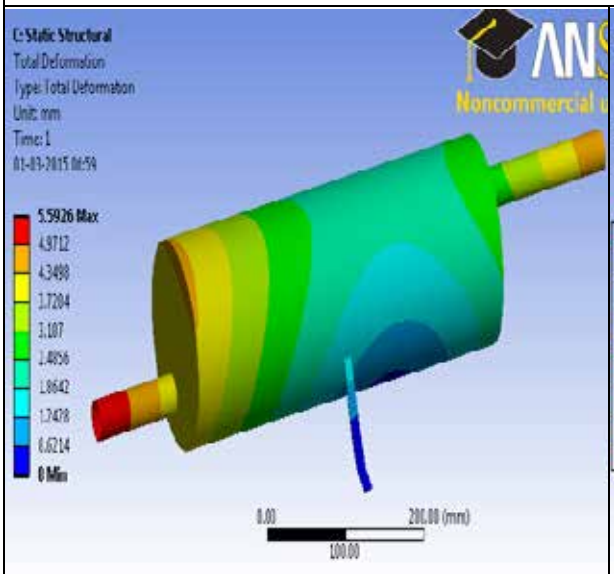

FIG. 3: TOTAL DEFORMATION FOR NON-PERFORATED SILENCER

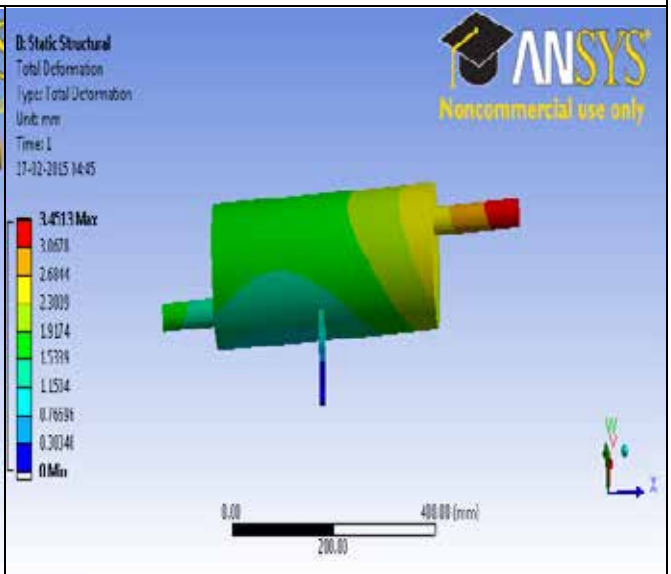

FIG. 4: TOTAL DEFORMATION FOR THE PERFORATED SILENCER

EQUIVAENT (VON-MISES) STRESS

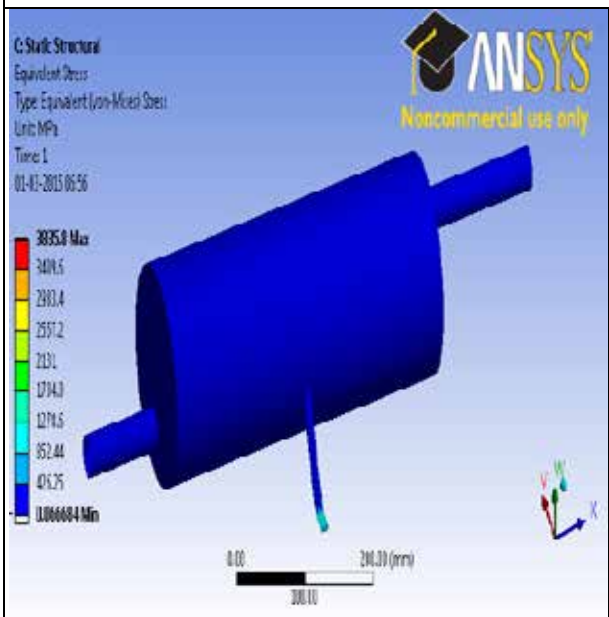

FIG. 5: EQUIVALENT (VON-MISES) STRESS

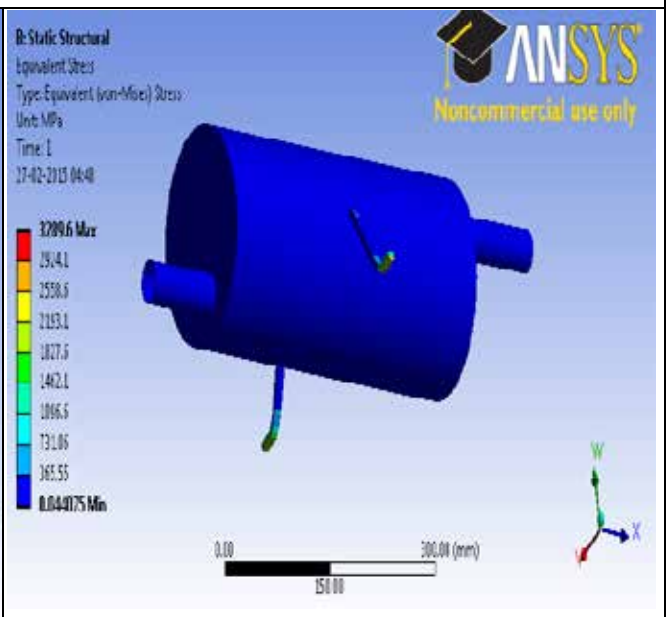

FIG. 6: EQUIVALENT (VON-MISES) STRESS

EQUIVALENT ELASTIC STRAIN

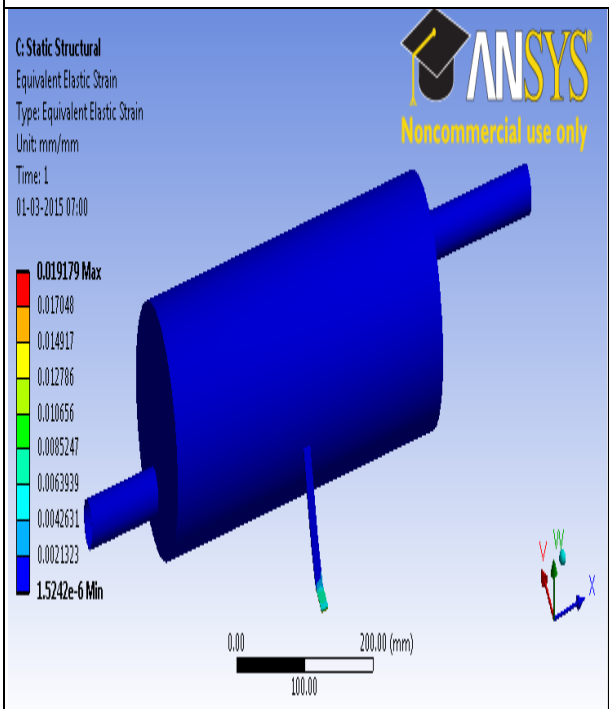

FIG. 7: EQUIVALENT ELASTIC STRAIN

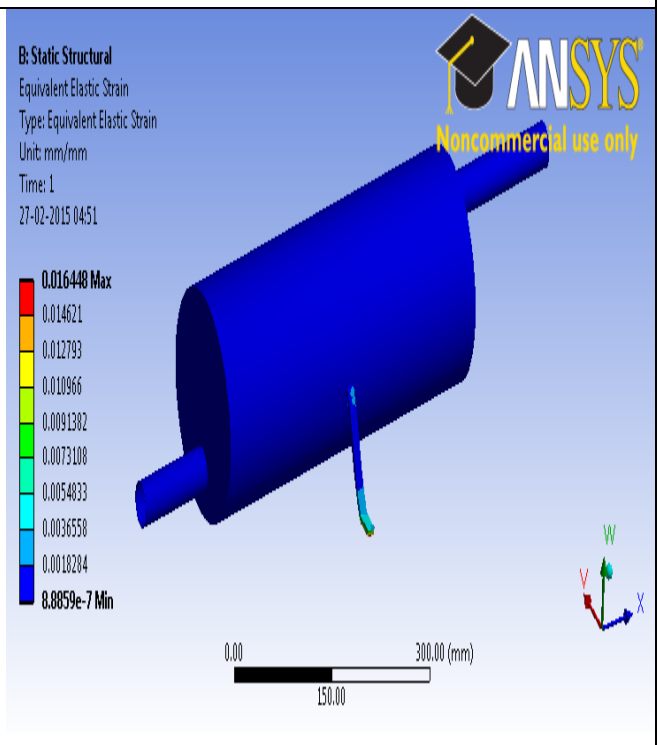

FIG. 8: EQUIVALENT ELASTIC STRAIN

V. CONCLUSION AND FUTURE SCOPE

It has been observed here in structural analysis of both type (perforated and non-perforated) silencer where stress developed at discontinuity. These stresses is not depend only upon inside pressure of exhaust gases but

also extremely affected by temperature of gases. Total deformation is much larger at used pressure and temperature parameter. There were generated different types of stress, strains, and the deformation. The two kinds analysis were disused was structural analysis. The results of the two silencer perforated and non-perforated were analyzed.

FOR THE NON-PERFORATED SILENCER

TABLE NO. 1

S NO.	TYPE OF THE ANALYSIS	MAXIMUM VALUE	MINIMUM VALUE
1.	TOTAL DEFORMATION (mm)	5.5926	0
2.	EQUIVALEN VON-MISES STRESS (MPa)	3835.8	0.066684
3.	EQUIVALENT ELASTIC STRAIN (mm/mm)	0.019179	1.5242×10^{-6}

FOR THE PERFORATED SILENCER

TABLE NO. 2

S NO.	TYPE OF THE ANALYSIS	MAXIMUM VALUE	MINIMUM VALUE
1.	TOTAL DEFORMATION (mm)	3.4513	0
2.	EQUIVALEN VON-MISES STRESS (MPa)	3289.6	0.044075
3.	EQUIVALENT ELASTIC STRAIN (mm/mm)	0.016448	8.8859×10^{-7}

Here noticed that the stress value in non-perforated more than the compared to perforated silencer. Also the similarly the total deformation and the strain compared there maximum deformation, strain were developed in the non-perforated. But in the perforated was getting less. So here clearly justified the perforated silencer much better than the non-perforated silencer.

There is more future scope in modeling of the silencer. The designer of the silencer can change design of the silencer like increase or decrease the length and diameter of the silencer. Here discussed in detail circular type of the silencer. For the future also can change its shape of the silencer like elliptical, tapper, rectangular etc.

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FINITE ELEMENT BASED COMPUTATIONAL STUDY FOR ASSESSMENT OF ELASTIC FOLLOW-UP IN AUTOCLAVE PRESSURE VESSEL

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ABSTRACT

Elastic follow-up is a complex and very influencing phenomenon in pressure vessel and piping system. It affects the performance of some structural components. Quantifying of elastic follow-up value is not that much easy, because it's still not clearly defined in ASME power piping code book. In this paper, elastic follow-up phenomenon in a laboratory based autoclave pressure vessel is shown in detailed analysis manner and brief reviews about previous research paper have been discussed. Geometric modeling of autoclave pressure vessel carried out by Creo2.0 and for analysis purpose Finite element based ANSYS14.0 software is used. Reduced elastic modulus method is used to quantify elastic follow-up. Here a study of elastic follow-up phenomenon taken into consideration at various temperature and pressure with varying elastic modulus but constant geometric parameter. Stress concentration and its effect on elastic follow-up have been described.

Keywords*: *Elastic Follow-up, Finite Element Analysis, Stress concentration.

I. INTRODUCTION

The term follow-up elasticity was first used by Robinson [1] in 1955, later known as elastic follow-up. In fig.1 it can be seen that as creep strain increment exceeds the elastic strain decrease and due to this Elastic follow-up factor is present. Elastic follow-up factor increases as relaxation progresses. Rate of relaxation of residual stresses is found to be proportional to the elastic follow-up factor (Z). It is a concept used to test the importance of possible inelastic strain concentration in a piping system designed primarily using the elastic rules specified in the ASME boiler and pressure vessel code [2]. Elastic follow-up also occur when reduction of modulus (due to stress decreases with increase in strain) is there [3].

Smith et al. [4] carried out experimental work on a bar assembly, which was fixed at both ends and subjected to total load in the central bar. Outer bar remains elastic whereas central bar undergoes perfectly plastic deformation. The load will be redistributed in the central bar and at the same time outer bar EFU action will allow to deform again to the central bar. An initial residual stress doesn't contribute directly to EFU but they promote initiation of plasticity. Teramae, [5], proposed a new method named simplified method which can be used for analysis of Elastic follow-up.In this global and local reference stresses are newly defined and it is found that this method is much better than finite element analysis and flexibility factor method. It requires very less computing time. In this new proposed methodology actual creep properties are used for analysis purpose and

structural analysis other than elastic analysis can be omitted [6].

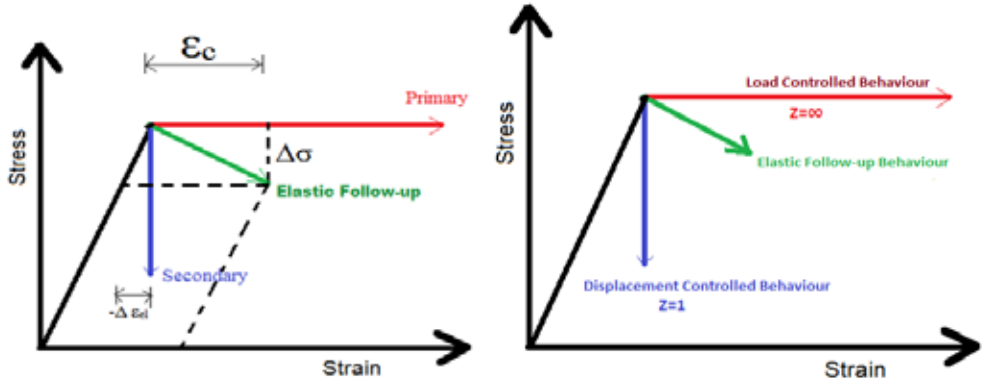


Fig.1: Stress strain relationship with EFU

Fig.2: EFU under Boundary condition [7]

Elastic follow-up is strongly related to creep, which develops in various pipes due to application under high temperature operation for a long time. For example in a superheater, tubes wear when exposed to high temperature and high pressure for a long time. Axisymmetric pipes are subjected to combined primary and secondary stresses with varying magnitude. Secondary stress EFU is affected by the magnitude of the primary stress and primary stress increases elastic follow-up factors [8]. It will help in the design consideration on how EFU is affected due to primary and secondary stresses of any process plant.

It is essential that the system be loaded elastically (plasticity or creep) for any elastic follow-up to occur. If EFU occurs in structure, the elasticity of slightly stressed regions may act as a spring that loads the highly stressed regions [9]. This happens either at low temperature (time-independent phenomenon) or at high temperature (time-dependent phenomenon). In low temperature piping system thermal expansion stress is treated as secondary, but it requires evaluation of local overstrain in that structure.

II. PRESSURE VESSEL

Pressure vessel is very important for any industrial application. It is used in Power plant for boiler drum, deaerator, storage tank, reverse osmosis etc. and in various other applications like industrial autoclave, autoclave for medical field, compressor, gas cylinder, auto stove, petromax, fire safety instrument etc. Pressure vessels are leak proof containers. They may be ofvarious shapes and sizes like cylindrical, spherical, ellipsoids and these are subjected to pressure, temperature, seismic loads etc. Pressure vessel may be subjected to low pressure low temperature or high pressure high temperature according to its application. Depending upon these aspects, pressure vessel can be categorized in two: a) Thick pressure vessel b) Thin pressure vessel; and to standardize these vessel ASME and pressure vessel code have been defined to work in effective manner [10]

III. EQUIVALENT REDUCED ELASTIC MODULUS PROCEDURES

Modulus of elasticity is a measure of stiffness and modulus of elasticity decreases with rise in temperature. We can say that material has high stiffness if deformation in elastic range is relatively small. This property of stiffness is very important in design where deformation must be kept small [7]. Here equivalent reduced elastic modulus procedure has been used in assessment of Elastic follow-up in inelastic structure. This procedure is

mainly used for piping system. It requires less time and low computational costs. Elastic stress is generated in most high stressed structural discontinuity region and corresponding strain will also have to be considered [11]. The simplified procedure to get a percentage of EFU used by Dhalla [2] is based upon the concept that inelastic response of an elbow, being part of a piping system and loaded by a thermal expansion stress, can be simulated by judiciously lowering its elastic modulus.

The elastic stress $\sigma_1$is generated in the most highly stressed structural discontinuity.In the Fig 3, heating of pressure vessel is represented by A. Corresponding to this value strain $\varepsilon_1$will be present. If this structural discontinuity experiences 100% Elastic follow-up, then elastic stress (σ_1) will be constant for various elastic modulus (E_1,E_2) values. For the same, calculated strain will increase from $\varepsilon_{1\ to}\ \varepsilon_2$.

$$\sigma_1 = \sigma_2 \frac{\varepsilon_1}{\varepsilon_2} = \frac{E_1}{E_2}$$

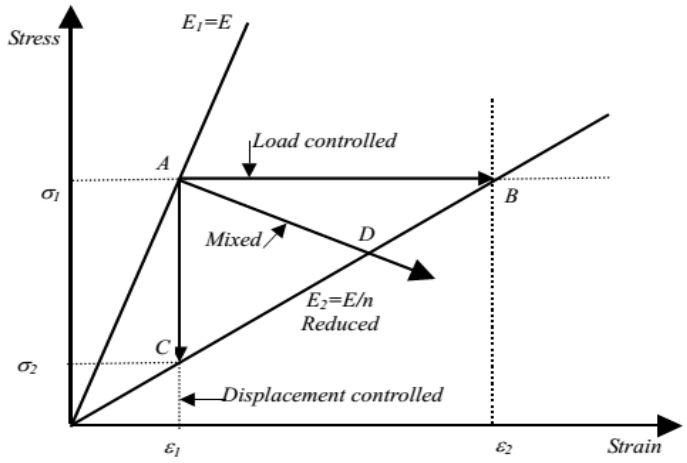


Fig. 3: Idealized load controlled and deformation controlled response [9]

If discontinuity is deformation controlled (0% EFU),the strain will not be changed due to reduced elastic modulus nevertheless stress decreases.

$$\varepsilon_1 = \varepsilon_2 \frac{\sigma_1}{\sigma_2} = \frac{E_1}{E_2}$$

Between both load controlled and deformation controlled, a mixed region is present which is influenced as Elastic follow-up.

Percentage of EFU can be estimated by $\frac{E_1/E_2 - \sigma_1/\sigma_2}{E_1/E_2}$

E_1 =Elastic Modulus

E_2 = Reduced elastic Modulus

σ_1 = Stress level for Uniform elasticity

σ_2 = Stress level for non-uniformity

IV. AUTOCLAVE PRESSURE VESSEL ANALYSIS

Bacteria can be destroyed by using super-heated steam in an autoclave. Its primary objective is to sterilize materials and pieces of equipment before being used in laboratories or other facilities. Sterilization process means a complete destruction of all forms of microbial life, including bacterial spores through physical or chemical methods. In steam sterilization, microorganisms are killed thorough saturated steam under pressure. Pressure gauges and thermometers are used to regulate desired pressure and temperature. The manufacturing of high-performance components from advanced composites often requires autoclave processing. Autoclave pressure vessel is generally constructed using mild steel and its inner surface is stainless steel coated. This coating will secure the autoclave from wear due to extreme condition. So here it is assumed that autoclave vessel is completely made of mild steel ASME SA516 Grade 70. As per 2004 with 2005 Addenda, ASME SA-516 is specification for pressure vessel plates, carbon steel, for moderate and lower-temperature service.

Total height = 540mm**Mechanical Properties**
Inner radius = 175mmDensity= 7833.41 kg/m^3
Outer Radius = 178.5mmPoisson's Ratio = 0.3
Uniform thickness = 3.5mmTensile Strength = 485-620 MPa
Lid height from Centre end = 45mm

TABLE I. ELASTIC PROPERTY FOR ASME SA-516 GRADE 70

No.	Temperature °C	Pressure (MPa)	Young's Modulus (GPa)	Thermal Expansion (/°C)	Thermal Conductivity W/m-K
1	37.7	0.0015	202.01	11.7×10^{-6}	46.1
2	65.5	0.0029	200.64	11.88×10^{-6}	45.3
3	93.33	0.0034	198.57	12.06×10^{-6}	44.7
4	104	0.015	198.56	12.09×10^{-6}	43.8
5	108	0.0345	198.89	12.14×10^{-6}	43.5
6	115	0.103	197.01	12.24×10^{-6}	42.9
7	121.1	0.0689	197.19	12.24×10^{-6}	43.8
8	130	0.138	195.01	12.36×10^{-6}	42.7

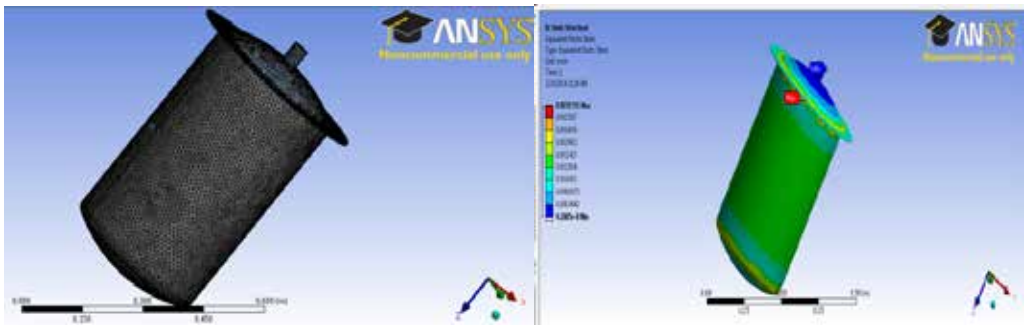
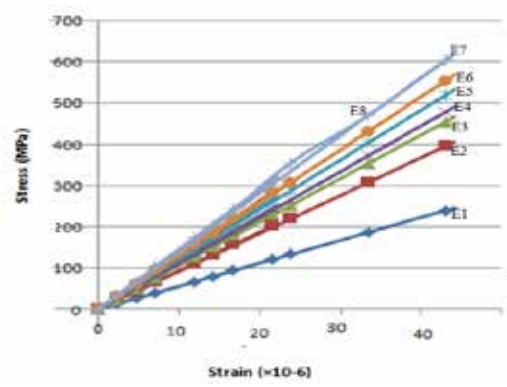


Fig.4: Meshed Autoclave Pressure vessel

Fig.5: Von-Mises Strain for maximum temperature



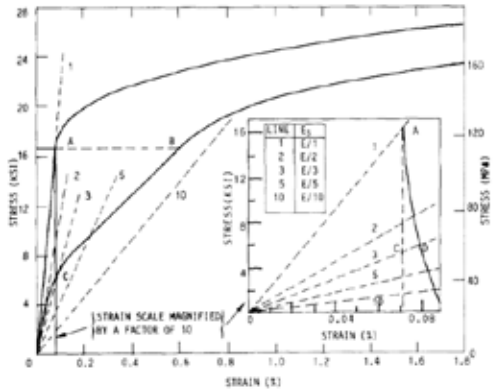


Fig.6: Isochronous stress strain curve for different moduli

Fig.7: Isochronous stress strain curve for different moduli [9]

TABLE II. RESULT FOUND OUT BY ANALYSIS

Elastic Moduli	E1	E2	E3	E4	E5	E6	E7	E8
Temperature °C	37.7	65.5	93.33	104	108	115	121.1	130
Pressure (MPa)	0.0015	0.0029	0.0034	0.015	0.0345	0.103	0.0689	0.138
% EFU	0	64.45	78.64	81.47	82.83	83.82	84.86	86.26

V.CONCLUSION

The influence of pressure and temperature on the mechanical behavior of the autoclave has been observed. Also the percentage of Elastic follow-up for this autoclave analysis has been found out. The maximum stress which is found to be at the structural discontinuity of the autoclave is well within the material yield strength. Maximum deformations will occur resulting from numerical simulations at increasing temperatures and pressures. Stress value increases highly with an increase in temperature. It is also observed that when the pressure is increased stress value will also increase at upper top discontinuity region as a result. If this stress value exceeds more than 250 MPa (which is the yield stress of the corresponding material) then possibility of collapse in the operation may occur.

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EFFECTIVE UTILIZATION OF ELECTRICITY AND AN ALTERNATIVE APPROACH TO MEET THE POWER DEMAND

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ABSTRACT

In recent years, power demand is increased and we have to be needed to meet a lot of power cut problems. Electrical power is a form of energy and we have come to depend on that in many automated product line business cannot tolerate its loss for even a few tens of milli seconds. In order to avoid that power cut problems and to provide continuous power supply a new technique is introduced in this paper. For that frequently used ,most important low power consumption devices are considered as primary loads and less priority high power consumption devices are considered as secondary loads. When the power usage by the customers is within the allowable limit, both primary loads and secondary loads are made in ON condition. When power demand is detected, only primary loads are in ON condition and secondary loads are made to turn off. By making the primary loads are in turned on condition for all time, we can fulfill the basic needs of residential in all situations. In this manner, power demand is identified automatically and loads are continuously distributed to all the customers. The proposed system is successfully verified through simulation using Lab view software.

Key Words*: *Lab View, Power Availability, Power Demand, Primary Loads, Secondary Loads

I. INTRODUCTION

Our recent technological world has become deeply dependent upon the continuous availability of electrical power [7]. In general commercial power is made available via grids. The grid must supply basic needs of residential, lighting, heating, refrigeration, air condition and transportation as well as critical supply to governmental, industrial, financial, commercial, medical, and communication communities[5],[6], [7],[10],[11].Increasing power demand leads to a lot of power cut problems.

Availability of power is one of the biggest inputs necessary for the sustained growth of any economy [6].This becomes even more important for a state like tamil nadu, which is one of the most industrialized and urbanized states in india. Over the last few years, tamil nadu has been facing massive power deficits. On an average, 3-4 hours of power cuts are being experienced by consumers in the state [1],[2],[3],[4]. The reason for the huge deficits in Tamil Nadu is due to the lack of power availability. Anticipating a huge increase in demand, driven by economic growth, states such as Maharashtra, Gujarat and Andhra Pradesh put in added efforts to increase the availability of power. This was done both by increasing own capacity and by encouraging private investment

in power generation [6].To satisfy the energy needs of state, we have needed to choose any one of the following options: (i) Increase the installed capacity by capacity additions. (ii)Based on the availability of power, use the generated electric power in efficient manner. Due to lack of capacity additions, especially in Tamil nadu the second option is the best approach to reduce the massive power cut problems. Chapter 2 describes about the basic methodology, flow chart used in this paper. The advantaage of Lab view and results of this work is discussed in chapter 3. Conclusion and future work of this paper are explained in Chapter 4.

II. BASIC METHODOLOGY

As per a statistical report, especially in Tamil nadu the percentage of power deficit has been increasing rapidly from 2003 to till date. in the year 2013, TANGEDCO issued a statement such that restriction in power usage for commercial customers between 6-10 pm and all industries in subjected to one day power holiday in a week to compensate energy gap and the generated power is not enough to satisfy the minimum power requirement of customers due to power deficit problem. The basic concepts followed in this paper are explained below. Energy is one of the most fundamental parts of our universe. Energy has come to be known as a `strategic commodity' and any uncertainty about its supply can threaten the functioning of the economy, particularly in developing economies. Achieving energy security in this strategic sense is of fundamental importance not only to India's economic growth but also for the human development objectives that aim at alleviation of poverty and unemployment and meeting the Millennium Development Goals (MDGs). Holistic planning for achieving these objectives requires quality energy statistics that is able to address the issues related to energy demand, energy poverty and environmental effects of energy growth[15].

2.1 Current Load Shedding Method

Electrical generation and transmission systems may not always meet peak demand requirements. The greatest amount of electricity required by all utility customers within a given region. In these situations, overall demand must be lowered, either by turning off service to some devices or cutting back the supply voltage (brownouts), in order to prevent uncontrolled service disruptions such as power outages (widespread blackouts) or equipment damage. Utilities may impose load shedding on service areas via rolling blackouts or by agreements with specific high-use industrial consumers to turn off equipment at times of system-wide peak demand.

According to TNEB report, on November 15, 2013total availability from internal generation, share from central generating station and other sources is only 9130 MW. But the requirement is 10515MW.In order to reduce this energy gap, TNEB has decided to cut down the power for at least 4-6 hours to all areas in cyclic manner. During this outage time, we can't use any appliances.

2.2 Power Supply Position

The annual report 2013-2014 gives power supply position in overall India such that though electricity generation in India registered tremendous growth in the past six decades, country continues to face peak and energy shortages. TABLE 1 shows how the peak and energy shortfalls have narrowed down in 2013-14 as compared to the power supply position in 2001-02[18]. Fig.1 shows the estimation of energy requirement and peak loads in india [17].

Table 1 Power Supply Position

Period	Energy(BU)			Peak (MU)		
	Requirement	Availability	Shortage(%)	Demand	Met	Shorts(%)
2001-02 (1)	522.54	483.35	35.19 (7.5)	78441	69189	9252 (11.8)
2006-07 (2)	690.59	624.50	66.09 (9.6)	100715	86818	13897(13.8)
2011-12 (3)	937.20	857.89	79.31 (8.5)	130006	116191	13815(10.6)
2012-13	998.11	911.21	86.90 (8.7)	135453	123294	12189 (9.0)
2013-14	512.14	487.72	24.42 (4.8)	135561	129269	62926)
(1)- End of 9th plan , (2)- End of 10th plan and , (3)- End of 11th plan						

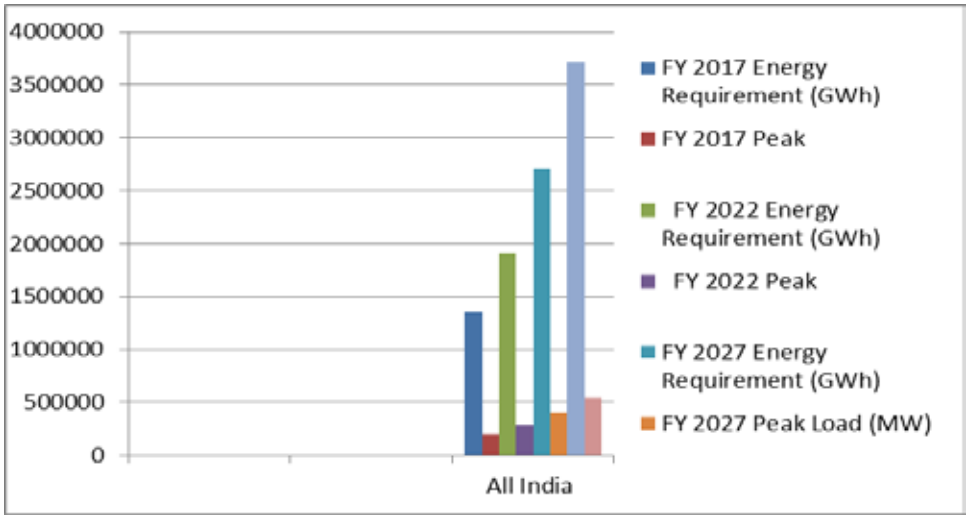

Figure 1 Energy Requirement And Peak Load Forecast By India

2.3 Primary loads & secondary loads

In automatic detection and control of control of power demand, all loads are grouped such as primary loads and secondary loads. For example tubes light, fan, CFL are taken as primary loads. These loads are fulfilling the minimum requirement of customers. Air conditioner, washing machines are taken as secondary loads. Fig.2 shows the flow chart for the proposed system. TABLE 3 represents the list of possible primary loads and secondary loads with their power consumption (for home appliances).

2.4 Automatic Detection & Control

At every time, voltage and current are sensed with the help of suitable sensors to calculate the total power consumed (P_{act}) by both primary loads and secondary loads are calculated and is compared with the allowable limit (P_{set}). Conditions to be followed for controlling the power demand in shown in TABLE 2.

Table 2 Status of Primary Loads & Secondary Loads for Different Power Levels

Separation of Loads	Home Appliances		Power Consumption in Watts
Primary Loads	Incandescent lamp		40-100
	Ceiling fan		10-50
	Compact Fluorescent lamp		10-30
	TV(19 " color)		70
	Mobile charger		3
Secondary Loads	Air conditioner		1000
	Refrigerator(20 cubic feet)		540
	Washing machine	Automatic	500
		Manual	300
	All other home appliances		-
*In industries, based on the priority Electronic machines may be separated as Primary Loads & Secondary Loads.			

Table 3 List Of Possible Primary Loads & Secondary Loads

Different power levels	Primary Loads	Secondary Loads
$P_{act} = P_{set}$	ON	ON
$P_{act} < P_{set}$	ON	ON
$P_{act} > P_{set}$	ON	OFF

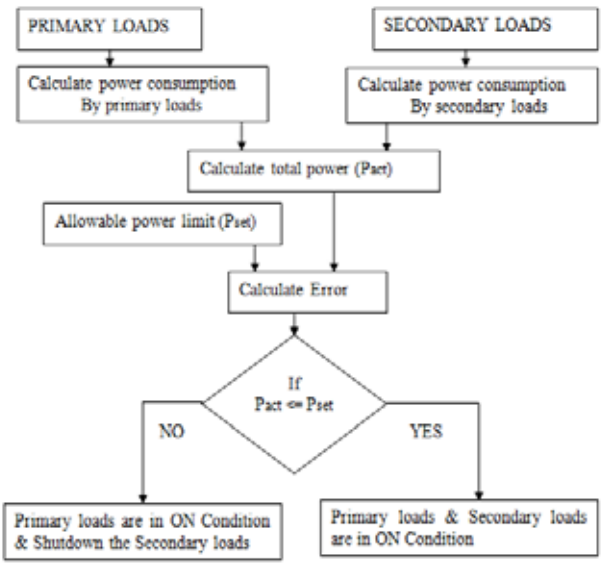

Figure 2: Flow Chart of the Proposed System

Figure 3 Status Of Primary Loads And Secondary Loads When $P_{act} = P_{set}$

Figure 4: Status Of Primary Loads And Secondary Loads When $P_{act} < P_{set}$

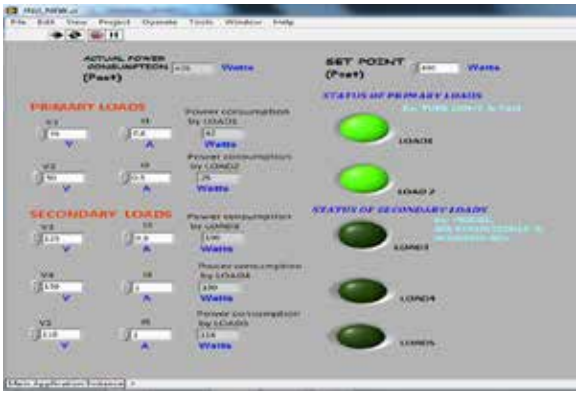

Figure 5 Status Of Primary Loads And Secondary Loads When $P_{act} > P_{set}$

III. SIMULATION RESULTS

3.1 Lab View Software

Lab view contains a comprehensive set of tool for acquiring, analyzing, displaying and storing data. In Lab view, we can build a user interface or front panel with controls and indicators. This paper use LEDs to indicate the status of primary loads and secondary loads at different power levels. The advantage of Lab view is, it requires less hardware component to implement specific real time applications.

3.2 Simulated Results

Front panel representation in Lab view for the various conditions of power levels are explained below. In simulation, two loads are considered as primary loads and two loads are considered as secondary loads. Fig.3 shows the front panel diagram in Lab view when calculated power (P_{act}) is equal to the allowable power limit (P_{set}).If $P_{act}= P_{set}$, all the LEDs are in ON condition. (ie. both primary loads and secondary loads are in ON condition) Fig.4 shows the front panel diagram in Lab view when calculated power (P_{act}) is less than the allowable power limit (P_{set}). If $P_{act}< P_{set}$, all the LEDs are also in ON condition (ie., both primary loads and secondary loads are in ON condition). Fig.5 shows the front panel diagram in Lab view when calculated power (P_{act}) is greater than the allowable power limit (P_{set}). If $P_{act}>P_{set}$, LEDs which represents as primary loads are in ON condition and LEDs which represents as secondary loads are in OFF condition.

3.3 Advantages

The main advantages of this concepts are includes,

- Issues of power cut problems reduced considerably.
- Cost Effective
- Uninterrupted power supply to all customers
- To satisfy the minimum power requirement of customers particularly for residential even in peak hour

IV. CONCLUSION

In this paper, a new method for utilizing the available electric power was verified using lab view software. If this technique is implemented for real time application in future, it would be very helpful to improve the economic growth of India. Even though in real time implementation, the initial installation cost is high, by using this automated system the generated electric power from power generating station will be used effectively and minimum power is distributed to all the customers to fulfill their basic needs of power for all time. We are trying to implement this concept in hardware also and our intension of this work is to establish a flexible, economical and easy configurable system which can solve our problem of power demand.

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DECISION STUDY ON USING CONSTRUCTION EQUIPMENTS FOR STAKEHOLDERS

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ABSTRACT

Consumer is using or choosing construction equipment based upon their maximum possible uses, initial cost, maintenance cost, depreciation cost and idle cost which are the factors responsible for the profit margin. By identifying the key factors and cost influence in equipment utilization in terms of rental basis rather than owning it, cost analysis is carried out with respect to productivity of the equipment. For which the questionnaire survey is conducted on engineers and contractors practicing the equipment management system in their construction projects. Accordingly the response from the respondents are analyzed by relative importance index method and the objectives are established with respect to real time requirements on equipment utilization. The evaluation strategies are carried out with various modes of acquisition. Such a way that profit margin chart is framed specifying right time to own the equipment for profit maximization of the construction firm.

Keywords : Equipment; Rent; Buy; Lease; Custom Hire; Net Present Value; Cost Analysis.

I.INTRODUCTION

The activities involved in construction projects where the magnitude of the work is on a big scale, timely completion and nature of work with quality control are very vital. The mechanization of work has to be done, where construction equipments play a pivotal role. Proper use of appropriate equipment contributes to budget, safety, quality, speed and on time completion of the project. Construction process performs with importance construction equipments. The contractor may not able to desire to own each and every type of construction equipment required for the project. On consideration of various features of the specific equipment, the contractor has to sparingly justify whether to purchase the equipment or to hire it. The amount capitalized in the owning of equipment should be recovered during the useful period of such equipment.

1.1 Scope of the Project

1. This research will optimize the investment on equipment's of a construction firm.
2. Thereby it increases the profit margin of the construction firm.
3. It creates value & support to the construction firm.

1.2 Objective of the Project

1. To carry out the study review on prevailing mixer, material handling equipment, screening equipment, vibrator, handling & compacting equipment.
2. To study the factors affecting like initial and maintenance cost, depreciation cost, idle cost and overheads involved in usage at various types of construction work.
3. To disparate and equate the performance of the equipment's under the influence of study focusing cost aspects

II. LITERATURE REVIEW

The major cost consequences in construction operations are mostly due to the machineries and equipment expenses of the project. The typical method of obtaining the machineries for the construction operation may be achieved by personal financing or through loans at permissible interest rates or leasing the equipment [1]. Thus the contractors or engineers preferring the option of acquiring due to increased equipment cost, maintenance cost, obsolescence of owned equipment and limited sources of outside capital. These options includes leasing, renting, purchasing equipment, and obtaining machinery service from custom operators.

2.1 Equipment Acquistion

The major issues faced by the contractor and engineer in running their companies to a successful turnover depends on the mode of acquisition of equipment for their construction projects [2]. This consideration mostly lies on the contractors and engineers undertaking CLASS II, III, IV, V works in case of government projects and some significant private contracts. They doesn't know the right time to acquire the equipment as owned and to replace the equipment. Because the timely owning and replacement of equipment will definitely increases the profit margin of the construction firm. There are various factors to be considered before going for the acquisition of equipment. The factors are both financial and non-financial factors that influence the equipment acquisition methods [2].

2.2 Equipment Cost

Equipment cost may in the range of 10% to 40% of overall construction cost [9]. The equipment cost is considered as a major problem before and after acquiring it. The costs included in the equipment are tangible and intangible [3]. By which the tangible cost of the equipment can easily be recorded and estimated using cost accounting methods. Where the equipment cost management lies between the capital cost and operating inferiority.

The substantial portion of the equipment production includes its ownership and operating cost. Hence the equipment cost make up a significant part of fixed and variable cost of construction operation [4]. The fixed cost generally include depreciation, interest, shelter and taxes, insurance. And operating cost includes fuel, lubrication, labor, repairs.

2.3 Equipment Maintenance

Profitability of construction projects depends on the effective equipment maintenance, because the equipment is one of the key factor for improving contractor's capability in performing their work more effectively and

efficiently [5]. The economic production of construction machineries depends on keeping the equipment in good condition. Construction firm faces finance loses due to improper maintenance, equipment failure and breakdown.

2.4 Decision Options

Decision to acquire the equipment makes the value and profit to the construction firm. There are other options and conditions reviewed during decision making. The general thumb rule is that percentage contribution of equipment less than 60% should go for renting [6]. This consideration favors purchasing the equipment with cost significant cost consequences. The decision making also goes with consideration of taxes, incentives, capital investment, interest rates, depreciation and resale value also influence the decision making process.

Consumer going for equipment acquisition need to know the elements involved in the life cycle of equipment and its estimated time period to be used with its frequency in that period [7]. Other sensible factors during decision making are reliable service for long time, down payment, tax benefits, and depreciation dispose of [8]. The condition in lease contract is that leases are structured to last at least a year. Canceling the lease contract prior to the contract period may end up with penalty.

There are some immeasurable factors like flexibility, ease of use, repetitions, which are responsible for the decision making on equipment acquisition. The measurable factors includes tax advantages, depreciation, maintenance cost and repair cost [9].

2.5 Evaluation of Decision Options

Cost benefit analysis is used to determine the appropriate contracting method. Cost benefit analysis includes two various methods such as Present Value Method & Net Present Value Method [7]. The method of estimating machinery cost over multiple time periods is in order to compare the options of leasing, renting, purchasing, custom hire [1]. The net present value analysis is used to evaluate the decision option in equipment acquisition. The DIRTI formula which is used to calculate the annual depreciation, interest, repairs, taxes and insurance [1]. The discounted after tax rate can also be analyzed by NPV method. The analysis is made worthwhile under the consideration of equipment productive hours and its useful life [9].

This research focuses on construction contractor and engineer practicing equipment management in Erode district, especially in Mettur canal division, Bhavani, Gobi, Erode, to identify the factors considered in equipment acquisition and evaluate the various decision modes of equipment acquisition on cost benefit analysis method.

III. RESEARCH METHODOLOGY

A detailed literature review was carried out to collect the information about the objectives of this study by considering construction practitioners in various locations. Through the literature review helped to establish the research topic in detail and general.The construction equipments considered for this research includes seven categories or eleven no. of machineries includes concreting equipments, concrete handling equipment, screening equipment, compaction equipment, handling equipment, bar bending equipment, earth compactor.

The resources from various literature of this study are international and national conference papers. Documents, internet, journal articles, magazines, books, etc. These are collectively named as secondary data sources, used to identify the financial factors affecting on construction equipment acquiring method [2].

3.1 Establishing Objectives

The design of questionnaire meant for surveying with contractors and engineers are literally achieved through various literatures. The primary data that are obtained from the sources of contractors and engineers with open ended questions. This survey is used for identification of factors affecting on construction equipments acquisition methods.

3.2 Data Collection & Evaluation

With those identification through the survey from contractors and engineers, the objectives of this study is established. Such that secondary process of research is proceeded with data collection regarding equipment purchase data, rental data, lease data and customers hire option.

The purchase data includes its down payment, interest rate, tax deductions, loan length and annual payment, salvage value, etc. The rental data includes equipment rental rate, rental inflation rate and twelve monthly use. The lease data found parallel to rental data replacing the terms as lease purchase having additional data about its lease length. The custom hire option includes user defined options on hiring the equipment includes custom hire base charge, custom hire unit and its inflation rate. Some of the common data includes annual insurance, housing, repairs, labours, lubricant, etc.

The data collected are evaluated by means of cost benefit analysis method. Evaluated data is consolidated and put-up in the form of profit margin chart providing the right time to own the construction equipment rather than renting or leasing as shown in figure 1.

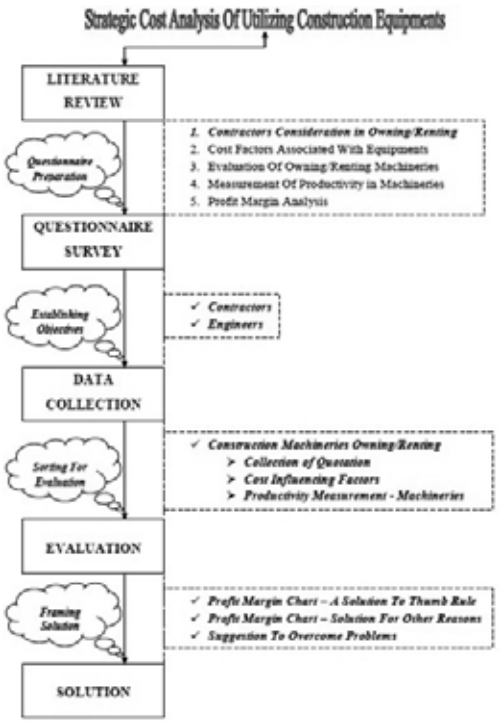
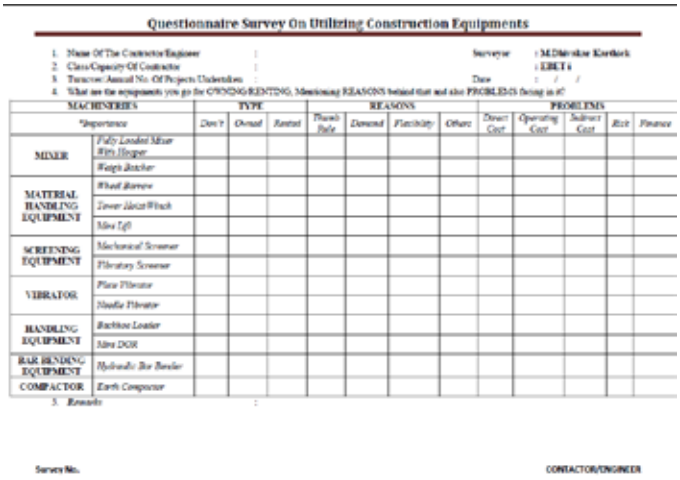


Figure 1 - Methodology

IV. QUESTIONNAIRE SURVEY

The data were obtained through the use of Investigatory Survey Research Approach Method (ISRAM), a well-structured questionnaire administrated on various constructors as in table 1.



Questionnaire Survey On Utilizing Construction Equipments

1. Name Of The Contractor/Engineer :
2. Class/Capacity Of Contractor :
3. Turnover/ Annual No. Of Projects Undertaken :
4. What are the equipments you go for OWNING/RENTING, Mentioning REASONS behind that and also PROBLEMS facing in it?

Surveyor : M.Dhivahar Karthick
: EBET 6
Date : / /

MACHINERIES		TYPE			REASONS				PROBLEMS				
*Importance		Don't	Owned	Rented	Thumb Rule	Demand	Flexibility	Others	Direct Cost	Operating Cost	Indirect Cost	Risk	Finance
MIXER	Fully Loaded Mixer With Hopper												
	Weigh Batcher												
MATERIAL HANDLING EQUIPMENT	Wheel Barrow												
	Tower Hoist/Winch												
	Mini Tyll												
SCREENING EQUIPMENT	Mechanical Screener												
	Vibratory Screener												
VIBRATOR	Plate Vibrator												
	Needle Vibrator												
HANDLING EQUIPMENT	Backhoe Loader												
	Mini DOR												
BAR BENDING EQUIPMENT	Hydraulic Bar Bender												
COMPACTOR	Earth Compactor												

5. Remarks :

Survey No. CONTACTOR/ENGINEER

Table 1 Questionnaire Survey on Constructors

4.1 Contractors

The survey is triggered with contractors practicing equipment management system in public projects. Contractors so identified are from sources of tamilnadu public works department in mettur lower canal division followed up by the sub division's ammapettai, bhavani, komarapalayam. The group so surveyed focused on CLASS I – V contractors, where priority is given to lower class contractors. This is because of logical reason that the premium class contractor's holds maximum assets and so equipment management may not be major problem in acquisition. The survey is conducted through in-person interview with them respectively.

4.2 Engineers

The equipment management system other than public works covers private contracts such as residential building construction, commercial construction and other civil works. Here engineers are involved in large proportions. Hence the survey made effective with in-person interview with engineers performing private contracts. Survey with engineers are achieved through civil engineers association situated in gobi, and erode.

4.3 Consoildation

The overall survey with contractors and engineers are consolidated for evaluation of research objectives as below as in table 2,

Table 2 Consolidated Survey Results

Machineries	***Acquisition***			***Reasons***				***Problems***			
Factors Evaluation	***D***	***O***	***R***	***T***	***D***	***F***	***O***	***D***	***O***	***R***	***F***
Fully Loaded Mixer	0	23	17	28	0	12	0	0	27	0	13
Weigh Batcher	34	3	3	7	0	0	33	0	10	10	20
Wheel Barrow	4	20	16	26	1	9	4	0	23	0	17
Tower Hoist/Winch	7	13	20	25	2	7	6	0	18	7	13

Mini Lift	11	12	17	21	1	5	13	5	12	6	15
Mechanical Screener	15	10	15	21	1	4	14	0	14	0	26
Vibratory Screener	38	2	0	2	1	1	36	0	0	16	24
Plate Vibrator	40	0	0	0	0	1	39	12	8	11	9
Needle Vibrator	2	20	18	26	3	9	2	0	18	4	13
Backhoe Loader	8	9	23	21	3	10	6	16	13	3	4
Mini DOR	9	13	18	25	1	7	7	11	16	5	2
Hydraulic Bar Bender	40	0	0	0	0	0	40	21	7	9	3
Earth Compactor	22	8	10	14	2	3	21	0	18	7	13

V. DATA COLLECTION

The data collection is done for equipment acquisition options evaluation. Data are classified based on its mode of acquisition such as purchase data, rental data and lease data. There are some common forms of data's that are common to above modes of classification are annual insurance and housing, annual repairs, annual labours, annual fuel and oil, marginal tax rate and after tax discount rates. Out of which the custom hire option holds the combination of data obtained in purchase data and rental data.

5.1 Purchase Data

The purchase data of any equipment holds the following contents necessary for evaluation show in table 3,

Table 3 Purchase Data

Purchase Price	Down Payment	Interest Rate	Loan Length	Annual Payment	Salvage Value

5.2 Rental Data

The rental data of any equipment holds the following contents necessary for evaluation as show in table 4,

Table 4 Rental Data

Rental Price	Annual Use	Rental Inflation Rate	Rental Length

5.3 Lease Data

The lease data of any equipment holds the following contents necessary for evaluation as show in table 5,

Table 5 Lease Data

Lease Price	Lease Units	Lease Inflation Rate	Lease Length	Lease Terms

VI. EVALUATION

6.1 Relative Importance Index

The survey evaluation was done using Relative Important Index (RII) method and found the bottom most factors leading to affect the labour productivity at construction site. The following formula is used to calculate the relative importance index.

Formula used for Relative Important Index

$$RII = \frac{\Sigma (Xi * Y_i)}{(Zi * 5)}$$

Where,

RII = Relative Importance Index

X_i= number of responses to the factors

Y_i = the value of rating

Z_i = total number of responses to the factors

Table 6 Survey Evaluation

Machineries **Factors Evaluation**	***Acquisition***	***Reasons***	***Problems***
	RII		
Fully Loaded Mixer With Hooper	0.808333	0.85	0.935
Weigh Batcher	0.408333	0.79375	0.8
Wheel Barrow	0.766667	0.84375	0.915
Tower Hoist/Winch	0.775	0.8375	0.815
Mini Lift	0.716667	0.8375	0.715
Mechanical Screener	0.666667	0.84375	0.87
Vibratory Screener	0.45	0.74375	0.72
Plate Vibrator	0.433333	0.74375	0.605
Needle Vibrator	0.8	0.81875	0.82
Backhoe Loader	0.791667	0.78125	0.57
Mini DOR	0.741667	0.85	0.63
Hydraulic Bar Bender	0.433333	0.75	0.475
Earth Compactor	0.566667	0.79375	0.815

6.2 Depreciation Analysis

Depreciation can be calculated more than a few ways, the simplest is the straight-line method. The depreciation is constant for annual basis, reducing the equipment value yearly.

- Depreciation in Any Period = ((Cost - Salvage) / Life)

Partial year depreciation, when the first year has M months is taken as:

- First year depreciation = (M / 12) * ((Cost - Salvage) / Life)
- Last year depreciation = ((12 - M) / 12) * ((Cost - Salvage) / Life)

6.3 Residual Value Analysis

Residual value is another name for salvage value, the residual value of an asset after it has been fully depreciated. The estimated value that an asset will realize upon its sale at the end of its convenient life. The cost is used in accounting to determine depreciation amounts and in the tax system to determine deductions. The rate can be a best guess of the end rate or can be determined by a regulatory body such as the IRS.

The residual value derives its calculation from a base rate, calculated after reduction. Salvage values are calculated using a number of factors, generally a vehicles market worth for the term and mileage required is the start point of the calculation, followed by seasonality, once a month adjustment, and lifecycle and clearance performance. The leasing company setting the residual values (RVs) will use their own historical information to insert the adjustment factors within the calculation to set the end value being the residual value.

6.4 Net Present Value Analysis

When comparing leasing and purchasing alternatives, the future monetary value you would expend in a lease or lease-purchase contract must be converted to its value in present monetary value in order to compare the real costs of each option. Calculating Present Value can be used as an intermediate step to calculating Net Present Value (NPV) [7].

Net present value analysis involves four simple steps.

- The first phase is to forecast the benefits and costs in each year.
- The second phase is to determine a discount rate.
- The third phase is to use a formula to calculate the net present value.
- The final phase is to compare the net present values of the alternatives.

Analysts should follow five common rules when forecasting costs and benefits:

- Forecast paybacks and expenses in today's monetary value amount.
- Do not comprise sunk costs.
- Embrace opportunity costs.
- Use probable value to estimate uncertain benefits and costs.
- Overlook non-monetary costs and benefits.

$$\mathrm{NPV}(i,N) = \sum_{t=0}^{N} \frac{R_t}{(1+i)^t}$$

Where,

t = time of cash flow

i = discount rate

R_t= net cash flow

i.e., net cash flow = cash inflow –cash outflow

NPV is an indicator of how much value an investment or project increases to the firm. With a particular project, if R_t is a positive rate, the project is in the status of progressive cash inflow in the time of t. If R_t is a negative rate, the project is in the status of reduced cash outflow in the time of t. Suitably, risked projects with a positive NPV

could be accepted. This does not certainly mean that they should be undertaken since NPV at the cost of capital may not description for opportunity cost, i.e., comparison with other available reserves. In financial concept, if there is a choice between two equally special substitutes, the one yielding the higher NPV should be selected as shown in table 7.

Table 7 Decision Conditions

What If?	Means	Then
NPV > 0	Investment worth adding	Equipment should be accepted on its mode of acquisition
NPV < 0	Investment doesn't worth adding	Equipment should be rejected on its mode of acquisition
NPV = 0	Investment may or may not considered	Equipment may be accepted on its mode of acquisition

VII. DISCUSSION

Effective equipment acquisition is sustained through evaluation of decision options. Relative importance index method and graphical method are used to evaluate importance scale of equipments. The importance scale of equipments addressed by constructors so evaluated from questionnaire survey is clearly understood by table 8,

Table 8 Importance scale by constructors

Machineries Factors Evaluation	***Importance Scale by Constructors***
Fully Loaded Mixer With Hooper	Most important & essential
Needle Vibrator	
Backhoe Loader	
Tower Hoist/Winch	
Wheel Barrow	
Mini DOR	
Mini Lift	Likely necessary but not important
Mechanical Screener	
Earth Compactor	
Weigh Batcher	
Vibratory Screener	Not necessary and not important
Plate Vibrator	
Hydraulic Bar Bender	

VIII.SUMMARY

Present study outlines the major equipment acquisition modes for profit maximization of construction firms. Based on literature study and from interview of experts, importance of equipments were identified under 3 major groups. Further methodology has suggested to work out with the data extracted from available modes of

acquisition by three methods; depreciation analysis, residual value analysis and net present value method as a function of framing profit margin chart. Data collection pattern is prepared based on these methods. It is proposed to carry out evaluation of equipment acquisition from net present value method.

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EFFICIENT LAYOUT OF FREDKIN GATE WITH MINIMIZED AREA

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ABSTRACT

Quantum cellular automata (QCA) is a new technology in nanometre scale (<18nm) to support nano technology. QCA is very effective in terms of high space density and power dissipation and will be playing a major role in the development of the Quantum computer with low power consumption and high speed. This paper describes the design and layout of a fredkin gate based on quantum-dot cellular automata (QCA) using the QCADesigner design tool. The fredkin design is based on combinational circuits which reduces the required hard-ware complexity and allows for reasonable simulation times. The paper aims to provide evidence that QCA has potential applications in future Quantum computers, provided that the underlying technology is made feasible. Design has been made using certain combinational circuits by using Majority gate, AND, OR, NOT in QCA. The QCA is a novel tool to realize Nano level digital devices and study and analyze their various parameters.

Keywords: Fredkin Gate, Nano-Technology, QCA

I. INTRODUCTION

Quantum Dot cellular automata (QCA) is an emerging technology that takes advantage of quantumeffects, which become increasingly apparent at the scale of a few nanometers. Previous work has shown that QCA has several novel features not available with conventional FET-based circuits [1]. Although the design cost function is different from FETbased technologies [2], a significant effort has already been started into exploring alternative arithmetic architectures that are portable to QCA, such as systolic arrays and bit-serial circuits. Recently, several successful studies into computer arithmetic and memory structures have provided further motivation for research into the realization of QCA technology [2-8]The QCA cell [9] consists of a system of four quantum dots charged with only two free electrons. Electrostatic repulsion between these electrons force them to occupy only the diagonal sites creating a so called “polarization” used to encode binary information, as seen in Figure 1. Interactions between neighboring cells allow for the layout of functional circuits, where the objective is to layout the cells in such a way that the ground state polarization of the output cells represents the correct output of a function to a given set of input vectors. The software simulation tool used for the realization of this technology is QCADesigner [15] by Walus group at university of British Colombia.

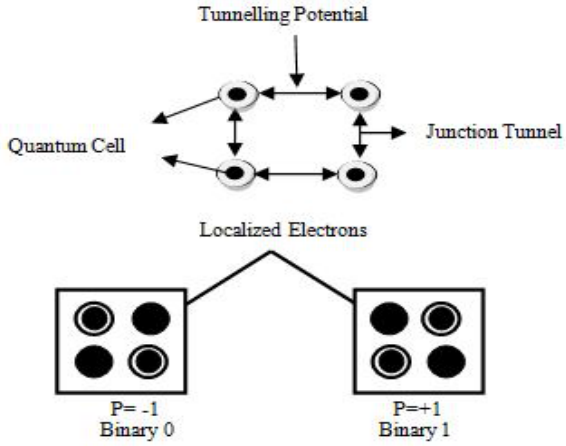


Fig:1 QCA Cell Polarization

To date, proof of concept QCA cells have been experimentally verified using a device which exploits the Coulomb blockade phenomenon [10], although the originally proposed cell is still beyond present fabrication capabilities. As a result, investigators are currently looking at creating QCA cells using single molecules [11].At first, it may appear premature to begin in depth investigation into the design of large circuits such as the one proposed here prior to the realization of a final technology. However, due to the capabilities of today's computers, the cost of such investigations is relatively low when compared to experimental studies. Such investigations provide a feedback mechanism in the development loop that can fairly rapidly include or exclude new device implementation concepts based on their potential application in these larger circuits. Using simulations we have, for example, identified a fundamental requirement for multilayer capability in complex circuits, previously believe unnecessary [12]. The physical interactions between cells may be used to realize elementary Boolean logic functions. The basic logic gates in QCA are the Majority logic function and the Inverter. The Majority logic function can be realized by only 5 QCA cells. The logic AND function can be implemented from a Majority logic function by setting one input permanently to 0 and the logic OR function can be Implemented from a Majority logic function by setting one input permanently to 1.Each gate is made to perform each performance Based on the mutual interaction between cells, basic logic components including an inverter and a three-input majority gate can be built in QCA. An inverter is made by positioning cells diagonally from one another to achieve the inversion functionality. A majority gate consists of five QCA cells that realize the following function:

$M(a,b,c)=ab+bc+ca$---------- à (a)

Majority gates can be easily converted to AND or OR gates by using a fixed value for one of the

inputs. For example, a two-input AND gate is realized by fixing one of the majority gate inputs to "0":

$AND(a,b)=M(a,b,0)=ab$---------- à (b)

Similarly, an OR gate is realized by fixing one input to "1":

$OR(a,b)=M(a,b,1)=a+b$---------- à ©

In combination with inverters, these two logic components can be used to implement any logic function.

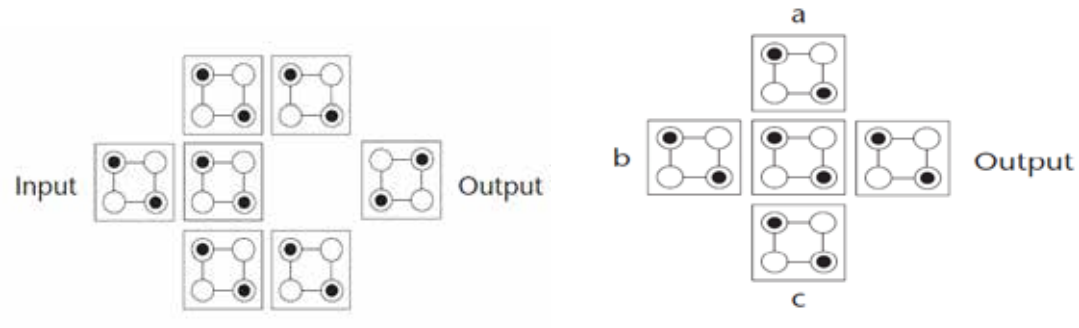


Fig 2QCA basic gates:(a) inverter, (b) majority gate.

II. CONSERVATIVE REVERSIBLE FREDKIN GATE

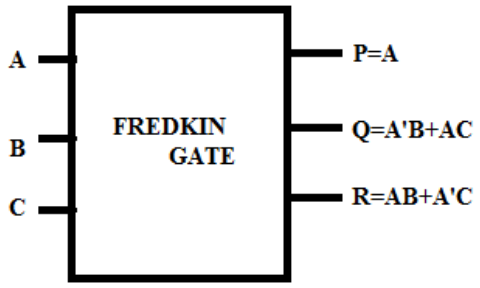


Fig 3 Fredkin gate

In fredkin gate we can perform different logic functions such as buffer,NOT,AND andOR.Along with fredkin gate many researchers invented the toffli gate and feymanngate.But as a result and conclusion from the three gate,the fredkin gate contains the minimum garbage outputs.Following figures and description is discussing about Fredkin gate and its benefitThe above fig 3 shows the block diagram of fredkin gate,the inputs are A,B,C and outputs are P,Q,R..It contains two OR gate and four AND gate.Inexisiting method[1] they used to implement the fredkin gate with cross wires,more majority gates and long array wires

III. BACKGROUND AND RELATED WORK

A number of different implementations to realize the bistable and local interaction required by the QCA paradigm have been proposed. Both electrostatic interaction-based QCA implementations (metal-dot, semiconductor, and molecular) and magnetic QCAs have been investigated.

Metal-Island QCA

The metal-island QCA cell was implemented with relatively large metal islands (about 1 micrometer in dimension) to demonstrate the concept of QCA [13, 16]. The dots are made of aluminum with aluminum oxide tunnel junctions between them. In this metal-island QCA cell, electrons can tunnel between dots via the tunnel junctions. These two pairs of dots are coupled to each other by capacitors. Two mobile electrons in the cell tend to occupy antipodal dots due to electrostatic repulsion.

Semiconductor QCA

A semiconductor QCA cell is composed of four quantum dots manufactured from standard semi conductive materials [20–22]. A device was fabricated in [23] using a GaAs/AlGaAs hetero structure with a high-mobility

two-dimensional electron gas below the surface. Four dots are defined by means of metallic surface gates. The cell consists of two double Quantum-Dot systems (half cells).Half cells are capacitively coupled. The charge position is used to represent binary information

Molecular QCA

A molecular QCA cell [25–28] is built out of a single molecule, in which charge is localized on specific sites and can tunnel between those sites. In the molecule shown in [29], the free electrons are induced to switch between four ferrocene groups that act as quantum dots due to electrostatic interactions, and a cobalt group in the center of the square provides a bridging ligand that acts as a tunneling path.

Magnetic QCA

A magnetic QCA cell is an elongated nanomagnet with a length of around 100 nm and a thickness of 10 nm. The shape of the nanomagnet varies for different schemes. The binary information in magnetic QCA cells is based on their single domain magnetic dipolemoments. The usage of magnetic interaction inherently minimizes the energy.

3.1 Related Work

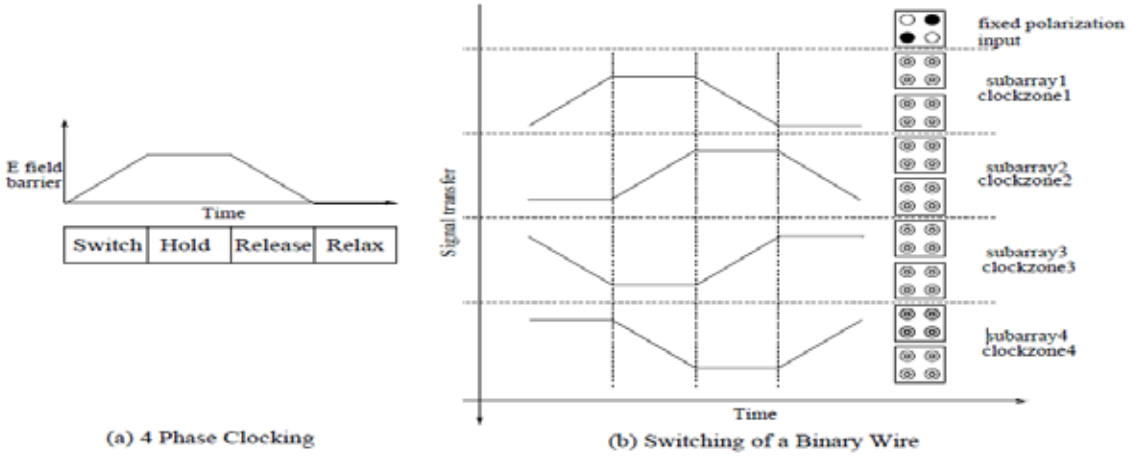
The testing of QCA was addressed for the first time in a seminal work reported in [4], where the defect characterization of QCA devices was investigated, and it was shown how the testing of QCA was different from conventional CMOS. The modeling of QCA defects at molecular level was done for combinational circuits in [11]. Fault characterization was done for single missing/additional cell defect on different QCA devices such asMV, INV, fan-out, crosswire, and L-shape wire. The test generation framework for QCA was presented in [10]. It was shown that additional test vectors can be generated for detecting QCA defects that remain undetected by the stuck-at fault model. Bridging fault on QCA wires was also addressed.

Clocking

In VLSI systems, timing is controlled through a reference signal (i.e., a clock) and is mostly required for sequential circuits. Timing in QCA is accomplished by clocking in four distinct and periodic phases and is needed for both combinational and sequential circuits. Clocking provides not only control of information flow but also true power gain in QCA. Signal energy lost to the environment is restored by the clock.

Two Types Of Switching Methods: Abrupt switching and adiabatic switching. In abrupt switching, the inputs to the QCA circuit change suddenly and the circuit can be in some excited state; subsequently, the QCA circuit is relaxed to ground state by dissipating energy to the

environment. This inelastic relaxation is uncontrolled and the QCA circuit may enter a metastable state that is determined by a local, rather than a global energy ground state. Therefore, adiabatic switching is usually preferred; in adiabatic switching, the system is always kept in its instantaneous ground state. A clock signal is introduced to ensure adiabatic switching.



(a) 4 Phase Clocking (b) Switching of a Binary Wire

For QCA, the clock signals are generated through an electric field, which is applied to the cells to either raise or lower the tunneling barrier between dots within a QCA cell. This electric field can be supplied by CMOS wires, or CNTs buried under the QCA circuitry. When the barrier is low, the cells are in a non-polarized state; when the barrier is high, the cells are not allowed to change state. Adiabatic switching is achieved by lowering the barrier, removing the previous input, applying the current input and then raising the barrier. If transitions are gradual, the QCA system will remain close to the ground state.

The clocked QCA circuit utilizes the tri-state six-dot cells, as shown in Fig 5. The clock signal is applied to either push the electrons to the four corner dots or pull them into the two middle dots. When the electrons are in the middle dots, the cell is in the “null” state. When the electrons are in the four corner dots, the cell is in an active state. The charge configuration of the cell in active state represents binary “0” and “1” as shown previously in Figure 1. A molecule with three quantum-dot hole sites is shown in Figure 2. Two such molecules form a six-dot QCA cell

This Clocking Scheme Consists Of Four Phases

Switch, Hold, Release and Relax, as shown in Figure 4.. The QCA circuit is partitioned into so-called clocking zones, such that all cells in a zone are controlled by the same clock signal. Cells in each zone perform a specific calculation. During the Relax phase, the electrons are pulled into the middle dots, so the cell is in “null” state. During the Switch phase, the inter dot barrier is slowly raised and pushes the electrons into the corner dots, so the cell attains a definitive polarity under the influence of its neighbors (which are in the Hold phase). In the Hold phase, barriers are high and a cell retains its polarity and acts as input to the neighboring cells.

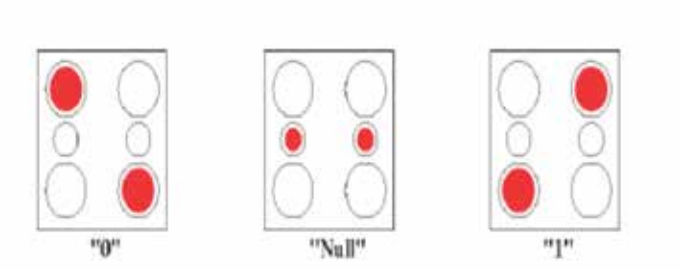


Fig 5 Schematic Diagram of a Six-dot QCA Cell

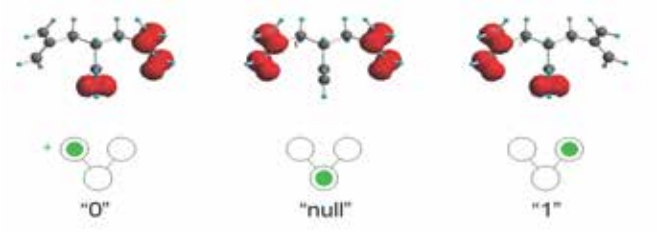


Fig 6Tri-state Quantum-dot Molecule

Finally in the Release phase, barriers are lowered and the electrons are pulled into the middle dots so the cell loses its polarity. Here switching is adiabatic, i.e. the system remains very close to the energy ground state during transition, and the stationary state of each cell can be obtained by solving the time-independent Schrodinger equation. Clocking zones of a QCA circuit or system are arranged in this periodic fashion, such that zones in the Hold phase are followed by zones in the Switch, Release and Relax phases. A signal is effectively "latched" when one clocking zone goes into the Hold phase and acts as input to the subsequent zone.In a clocked QCA circuit, information is transferred and processed in a pipelined fashion and allows multi-bit information transfer for QCA through signal latching. All cells within the same zone are allowed to switch simultaneously, while cells in different zones are isolated. initially, subarray1 switches according to the fixed input, and subarray2 shows no definite polarization at this time. Then, subarray1 enters the Hold phase; at this time subarray2 starts switching. As subarray3 is in the relaxed state, it will not influence the computational state of subarray2. Next, subarray1 is moved to a Release phase; subarray2 is in the Hold state and serves as the input to subarray3 (which is in the switch phase). The signal is "latched" when subarray1 enters the Hold phase and acts as input to subarray2.In the adiabatic switching schemes, fluctuations in operating temperature T may excite QCA cells above their ground state and produce erroneous results at the output. An analysis of these thermal effects on a line of N QCA cells is provided in . It has been shown in [1] that for reliable kink-free computation, within a single clocking zone, N is bound by e EkkBT . Large QCA circuits are therefore partitioned into smaller sub circuits, each of which resides in its own clocking zone. The clock signal is commonly generated by CMOS wires buried under the QCA circuitry. Fig 6 depicts the schematic diagram for clocking a 3-dot molecular QCA array [28]. QCA molecules are located in the xz plane and clock wires are placed in the z direction, thus inducing an electrical field in the y direction. One of the limiting factors for high density of QCA systems is the wiring requirements for the generation of the electrical field. The use of single walled carbon nanotubes (SWNTs) and a new clock wire layout is recommended in [31].

It has been shown that metallic SWNTs are excellent conductors [34] and can be used to generate a clocking field that smoothly propagates the QCA signals. The layout method of [35] consists of a series of clocking wires perpendicular to the QCA signal direction.In this method, the direction of the perpendicular clocking wires must be changed with turns in the QCA signals. The approach proposed in [31] allocates clocking wires at a 45o angle .hence, only two clocking directions are needed to allow QCA signal propagating along the two axes.

IV.QCA SIMULATORS

Several QCA simulators are currently available, They are mAQUINAS and QCADesigner are physics-based and solve quantum equations for Quantum-Dot Cellular Automata cell interactions. mAQUINAS assumes a continuous clocking scheme envisioned for the molecular QCA systems. Adiabatic switching is assumed where the system is kept close to the ground state. At each time step, the time independent Schrodinger equation is solved for each cell. The process continues until a self consistent solution is found for the entire system. QCADesigner [27] has been used to produce results presented in the book, and will be discussed in more detail next. However, quantum simulation is computation intensive and are not suitable for large circuits. QBert is another simulator developed for digital logic simulation for QCA which can be run much faster. A new model based on a SPICE model has been proposed and experimentally verified.

V.SIMULATIONS AND RESULTS

In existing fredkin gate they used to design the fredkin gate with Binary wires,cross wires and 6 Majority Voters.But in this paper describes about Fredkin gate implement with minimum area that contain only Binary wires and 4 Majority voters. Existing paper produced fredkin gate using 246 cells in QCA Designer tool.In this paper the fredkin gate implemented using 133 cells only,so the implementation area will be minimizes.

Fig 7 Proposed layout of fredkin gate

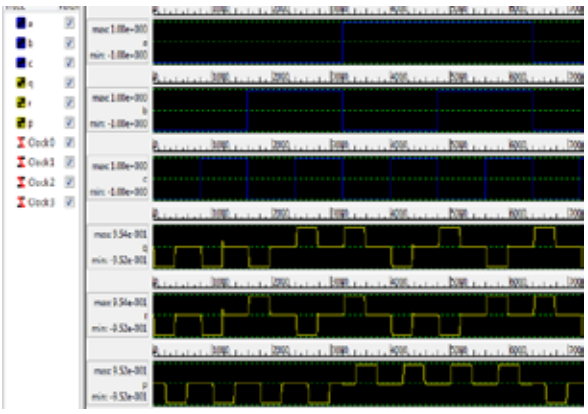


Fig 8 Output waveform

Table1Truthtable

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Existing fredkin gate	246	4s
Modified fredkin gate	133	1s

Table 2 Comparison Table of fredkin

S.no	GATES NAME	NO.OF.CELLS	KINK ENERGY	POLARIZATION	SIMULATION TIME
1	INV	11	$14.44*10^{-21}$	P_{001} ±9.54	0
2	OR	5	$22.09*10^{-21}$	P_{001} ±9.54	0
3	AND	5	$19.43*10^{-21}$	P_{001} ±9.54	0
4	MODIFIED FREDKIN	133	$150.78*10^{-21}$	P_{001} ±9.54	1s

gate7 shows the existing and proposed fredkin gate layout.Abovetable prescribes the truth table for fredkin gate.The inputs are A,B,C and Outputs are P,Q,R.The output of P displays the input of A,Hence we can understood that fredkin gate implement as buffershows the output waveform of fredkin gate, and it was simulated in bistableengine.The option parameters for fredkin gate of bistable engine is given below.

5.1 Equation

- Electrostatics interactions between the electrons in QCA is

$$E=\frac{Q1\,Q2}{4\pi\varepsilon_0\varepsilon_r r}$$

The interaction is determines the kinetic energy between two cells, thus the kinetic energy is

$$E_{kink}=E_{opp.pol}-E_{same\ pol}$$

From this equation we can calculate the kink energy of fredkin gate and others.The table for kink energy is shown below.In table 3 contains the calculation result from kink energy equation.Table2 contain the comparison between the existing and Proposed fredkin gate layout

VI.CONCLUSION

Each gate is made to perform each performance,But in fredkin gate we can perform different logic functions such as buffer,NOT,AND and OR. Along with fredkin gate many researchers invented the toffli gate and feymanngate.But as a result and conclusion from the three gate,the fredkin gate contains the minimum garbage outputs. In existing fredkin gate they used to design the fredkin gate with Binary wires,cross wires and 6 Majority Voters.But in this paper describes about Fredkin gate implement with minimum area that contain only Binary wires and 4 Majority voters. Existing paper produced fredkin gate using 246 cells in QCADesignertool.In this paper the fredkin gate implemented using 133 cells only,so the implementation area will be minimizes.Here I conclude that my fredkin gate design consumes low power dissipation,Area and delay.

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