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DESIGNS OF CARRY LOOK AHEAD BCD SUBTRACTOR FOR REVERSIBLE LOGIC APPLICATIONS.

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ABSTRACT

BCD subtractor paves an important role in various applications such as quantum computing, Nanotechnology and optical computing .It is widely used because of its reversible logic implementation. BCD subtractor comprises of carry look ahead subtractor and carry skip subtractor .The operation of carry look ahead BCD subtractor is implemented by using nine's complement method with proposed CLA BCD adder. A carry look ahead adder is a fast adder used to compute addition with less propagation delay. It reduces the amount of time required to determine carry bits by improving the speed. The overall performance of BCD subtractor is efficiently improved using proposed CLA BCD adder. The propagation delay of proposed method is reduced from 14.58ns to 7.45ns

Keywords: Modified full adder (MFA), Proposed BCD CLA adder, 9's Complement method and Fast adders.

I. INTRODUCTION

In electronics, a subtractor can be designed using the same approach as that of adder. Subtractors are usually implemented within a binary adder for small cost. The important role of implementing BCD arithmetic is to enhance its speed as much as possible. Addition of signed BCD numbers can be performed by using 9's or 10's complement methods. A negative BCD number can also be expressed by taking the 9's or 10's complement. BCD subtractors are a part of the core of an arithmetic logic unit (ALU). The control unit decides which operations an ALU should perform (based on the op code being executed) and sets the ALU operation include more functions. Carry look ahead adder is designed to eliminate the ripple carry delay and to overcome the latency introduced by the rippling effects of the carry bits. This method based on the carry generating a carry propagating function of the full adder. This adder is based on the principle of looking at the lower bits of the augends and addend. The adder helps to reduce the carry delay in which the propagation of carry signal happens by reducing the usage of number of gates when higher order is generated.

II. RELATED WORK

2.1 BCD Subtractor

BCD subtraction can be performed by using nine's complement. In nine's complement, the minuend is added with the subtrahend. The nine's complement performed by nine minus the number in which nine's complement is to be computed. For example, consider the number 7 whose nine's complement will be 2(9-7=2), which is represented in terms of BCD is 0010.There are two possibilities i.e., [8]: [1] in BCD subtraction using nine's complement. The output of the sum will be positive in this performance. In 9's complement subtraction when 9's complement of smaller number is added to the larger number, carry is generated. This carry value is again added with resulting value. This method is called an end-around carry. When larger number is subtracted from smaller one, there is no carry, and the result is in 9's complement form and negative. This is illustrated in following examples:

EXAMPLES:

Δ REGULAR SUBTRACTION:

8-2=6

BCD SUBTRACTION:+7(9's complement)= 15

Here, 1 is carry added with 5: 5+1=6

Δ REGULAR SUBTRACTION:

1-2=-1

BCD SUBTRACTION:

1+7(9's complement) =8

9's complement of 8=1

We have realized that XOR gates are not in need of nine's complement for complementing. NOT gate is performing better than xor because it can able to reduce the complexity of the circuit in CMOS as well as reversible logic implementation. The design of nine's complement is shown in fig 1

2.2 Related Diagrams

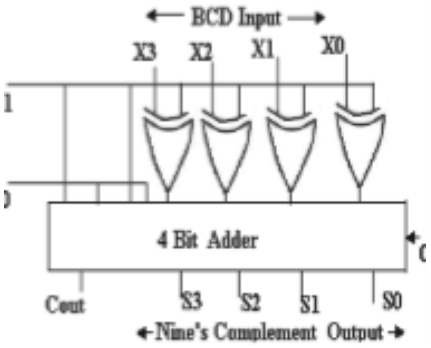

Fig:1 Nine's Complement

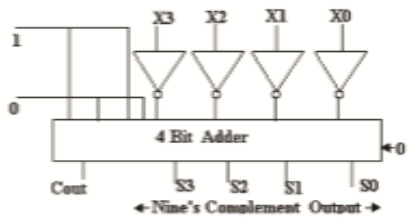

Fig:2 Proposed Nine's Complement

2.3 Proposed Carry Look Ahead Subtractor

BCD subtractor is done by integral the NINE'S COMPLEMENTER, BCD adder and 4-bit adder. The NINE'S COMPLEMENTER, the BCD adder and the 4-bit adder are replaced by their carry look ahead counterparts. This replacement helps us to design a BCD subtractor with faster and more efficient.

2.4 CARRY LOOK AHEAD BCD ADDER

A carry look ahead BCD adder is proposed which is a modification over the architecture proposed in [9, 10] and is especially improved for making it suitable for CMOS and reversible logic implementation. In the proposed CLA BCD adder, OR gates used in the and replaced by XOR gates. One cannot replace the OR gates in the equations in [9, 10] randomly. Hence, a rigorous study has been done and OR gates in the equations in [9, 10] have been replaced in certain places. The proposed CLA BCD adder is verified by using Verilog HDL simulator. The useful purpose of Verilog is given below

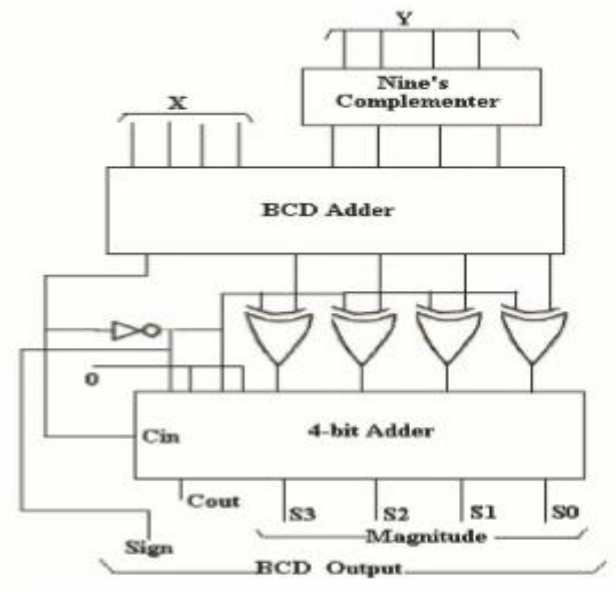

FIG:3 Modified Conventional BCD Subtractor

1. In the conventional CMOS logic, compare with OR gate, the XOR gate can be constructed with a few number of transistors.

2.The multi-input OR gate is compared with one less carbage output of XOR gate and less number of reversible gates will be used in XOR gate. For example, the equation x y can be realized with only one (2x2 reversible gate) and two garbage output compared to x which can be realized with one 3x3 reversible gate and two

garbage output, or two 2x2 reversible gates with two garbage output. Thus, in reversible logic it is easy to realize equations as XOR functions compare than OR functions. This is one of the major advantages of XOR gate.

Consider two BCD numbers x and y of 4 bits each, using the proposed approach, the modified functions used to generate the carry look-ahead BCD adder are as follows

// 1st Part g[j] = x[j] • y[j] 0 j 3 "generate" p[j] = x[j] + y[j] 0 j 3 "propagate" h[j] = x[j] y[j] 0 j 3 "half-adder"

//2nd Part M = g[3] (p[3] • p[2]) + (p[3] • p[1]) (g[2] • p[1]) N= p[3] (g[2] + (p[2] • g[1])) (Here M and N are the carry generate and propagate functions of the first three bits of the decimal number x and y (x[3]x[2]x[1] and y[3]y[2]y[1]), respectively).

2.4. Carry Look Ahead Binary Adder

Figs.2 and 3 represents the design of the NINE'S COMPLEMENTER and the modified conventional BCD subtractor respectively, the proposal 4-bit adder is the key requirement to increase their efficiency. The carry look-ahead counterparts are proposed to replace the 4 bit adder blocks. A modified carry look-ahead adder (abbreviated as MCLA) is similar to CLA (carry look-ahead adder). The drawback of MCLA is that, In spite of faster speed, MCLA requires large area coverage because of the usage of the excessive number of NAND gates for faster carry propagation. When we use MCLA for designing the CLA, this problem will occurs highly. The MCLA uses the modified full adder (MFA) as shown in Fig.4.The replacement of 4th MFA in the MCLA by a full adder to reduce the number of gates without affecting the speed improvement. Fig.5 shows that verification i.e., there will be a reduction in the number of gates to generate the final carry. The proposed 4-bit CLA can be cascaded to design an expanded width CLA in series form in order to obtain the less number of usages of gates.

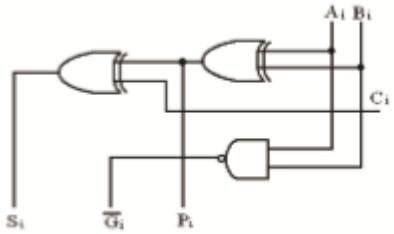

FIG: 4 Modified Full Adder

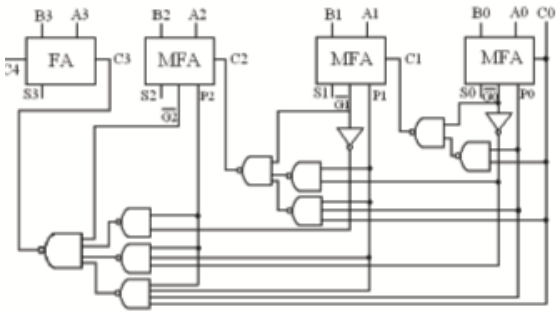

FIG: 5 PROPOSED 4-BIT CARRY LOOK AHEAD ADDER

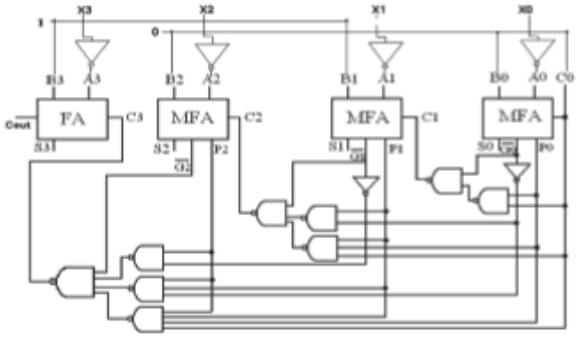

FIG: 6 CLA'S NINE'S COMPLEMENT

Figure 6 shows the proposed NINE'S COMPLEMENTER using the proposed carry look ahead adder and using the proposed concept of using NOT gates for complement- ting (rather than XOR gates). The proposed NINE'S COMPLEMENTER performs fast speed and it satisfies the requirements of the carry look-ahead approach and it requires less area.

2.6 Carry Look Ahead BCD Subtractor

BCD adder, 4-bit adder and NINE'S COMPLEMENTER are the components required to designed in carry look-ahead fashion, the carry look-ahead BCD subtractor can be designed by integrating the components. Figure 7 shows the design of the proposed carry look-ahead BCD subtractor and The emphasis on improving the individual modules of the BCD subtractor, is the significant purpose to improve the efficiency of BCD subtractor and make it is more suitable for reversible logic implementation.

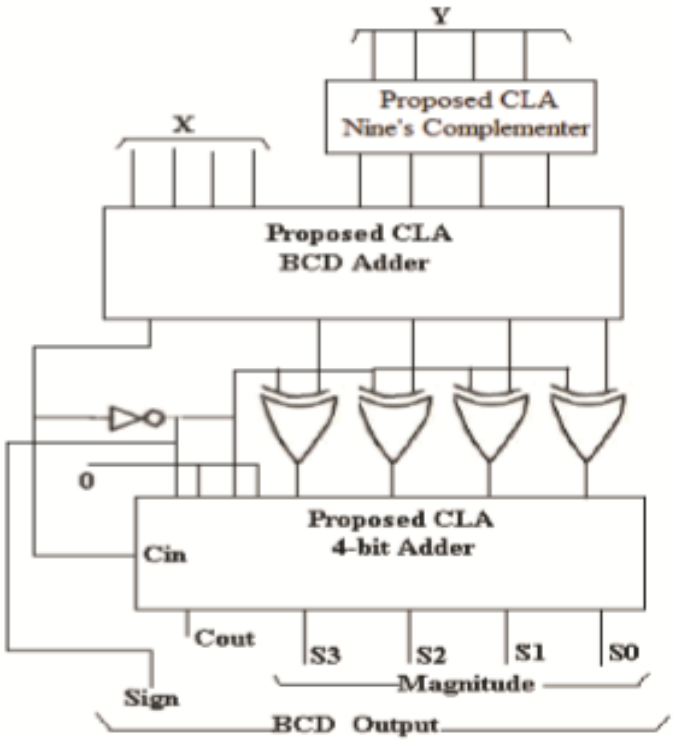

FIG: 7 Proposed Carry Look Ahead Bcd Subtractor

	Conventional BCD subtractor	CLA BCD subtractor	Proposed BCD subtractor
Delay	17.23ns	14.58ns	7.45ns

Table1: comparison of conventional BCD subtractor with proposed method

III. SIMULATION OUTPUT

OUTPUT WAVEFORM

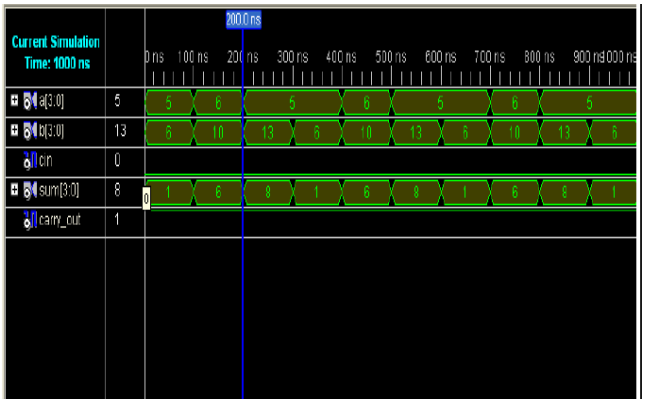

FIG8: CARRY LOOK AHEAD SUBTRACTOR

IV. CONCLUSION

The operation of adding/subtractor two binary numbers is one of the fundamental tasks performed by a digital computer. BCD subtractor can be used for designing large reversible systems, which is can be used in ultralow power digital circuits and quantum computers. This paper explained that the performance of carry look ahead BCD subtractor design by different logic diagrams with least time delay. It reduces the amount of time required to determine carry bits by improving the speed. The BCD subtractor is used mostly in low-power CMOS, Nano-technology and optical computing. The Xilinx ISE Design suite 14.5 HDL simulator is used to measure the overall efficiency of proposed BCD subtractor. It is estimated that the propagation delay reduced to 7.45 ns.

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