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Design and Implementation of Three Fish Cipher Algorithm Blocks Using FPGA

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ABSTRACT

Every organization sees the secure communication is the prime requirement. In today's world the security has became the major aspect of life. It can be achieved by various techniques such as password, cryptography and biometrics. In this work, to study various encryption algorithms, data encryption standard used for data security and implement Three-Fish Cipher algorithm in order to achieve security with minimum number of overheads then compare the proposed work with test bench and then compile, simulate the test bench with the help of Xilinx ISE software.

***Key Index:* Secure communication, Three-Fish Cipher algorithm, Xilinx ISE software.**

I. INTRODUCTION

Data Encryption Standard (DES) is the most well-known cryptographic mechanism in history [1]. It begins with the work of Feistel at IBM in the early 1970s. Ruth M. Davis [3] provides a hardware-implementable algorithm for enciphering data, which has been adopted as a Federal standard to provide a high level of cryptographic protection against various attacks. Whitfleld Diffie et. al [4] describes cryptographic technology, which examines the forces driving public development of cryptography. Ingrid Verbauwhede [5] described Security and Performance Optimization of a New DES Data Encryption Chip. James E. Katz [6] provides Social Aspects of Telecommunications Security Policy for privacy and of society for security. H. Bonnenbergt [7] described the VLSI implementation of a new block cipher. K.H. Mundt [8] presented superscript ASIC get 100Mbits/ s encryption speed on silicon applying 1 micron design rules. C. Boyd [9] provides the modern data encryption in which proposed standard for digital signatures based on RSA were introduced. R. Zimmermann et. al. [10] provides a 177 Mb/s VLSI implementation of the International Data Encryption Algorithm. Stefan Wolter [11] provides the implementation of the IDEA architecture that includes a concurrent self-test based on a mod3 residue code self-checking system. Seung-Jo Han [12] describes the improved DES algorithm in which a 96-bit data block is divided into three 32-bit sub-blocks. Hassina Guendouz et. al. [13] describes rapid prototype of a fast data encryption standard with integrity processing for cryptographic applications. K. Wong [14] performed transform domain analysis of DES algorithm by using tool. M.P. Leong [15] described a bit-serial implementation of the International Data Encryption Algorithm (IDEA). R. G. Sixel et. al. [16] describes a high level language implementation of the DES and bit-slice architecture. Teo Pock Chueng [17] provides implementation of pipelined DES using Alter CPLD. Toby Schaffer et. al. [19] describes an integrated design of

Advanced Encryption Standard (AES). Cameron Patterson [20] provides high performance DES encryption using Vertex FPGA. Jbits. Pui-Lam Siu et. al. [22] presented about the A Fault Attack on pairing based Cryptography Current fault attacks against public key cryptography focus on traditional schemes.

II. NEED OF WORK

After the study of various encryption algorithms, the concept of keys has been successfully observed from the observation it has been seen that better secured system can be achieved by increasing the key length. Longer key lengths consume more power and dissipate more heat. Basically it is a tradeoff, between security and overheads. In order to achieve more secured system continuous efforts are required. An efficient encryption algorithm should consist of two factors – fast response and reduced complexity. By keeping the utility of encryption algorithm in secure communication it is desirable to optimize and/or improve the encryption techniques, so security overheads remains under control.

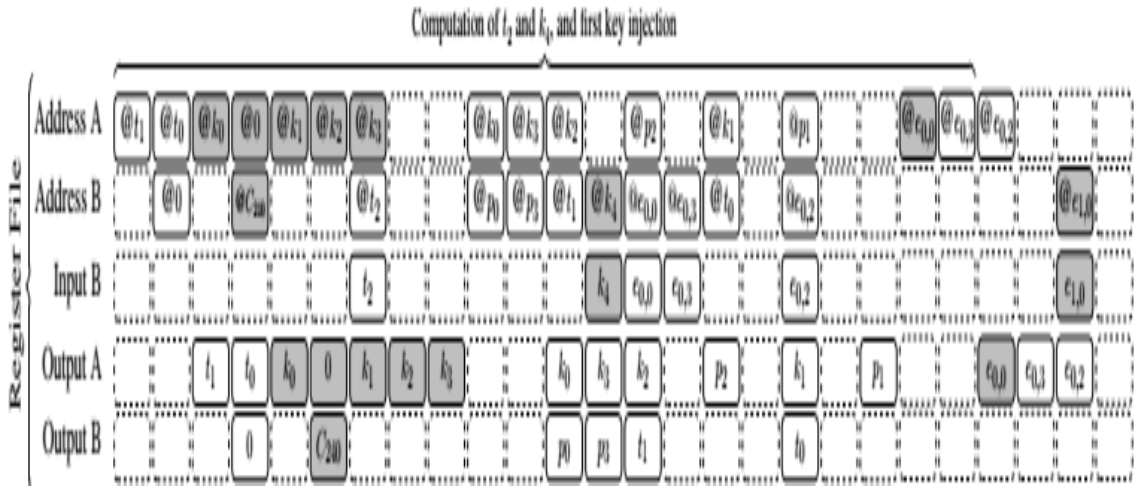
III. THREE FISH CIPHER ALGORITHM

This report discusses the three fish cipher algorithm with the help of key scheduling how the encryption does and decryption algorithms are defined by applying the plain text to encryption block and generation of cipher text as output. By applying cipher text to the decryption block and key has been scheduled in a way that deciphered text has been found.

Block Size	Number of Words (Nw)	Number of rounds (Nr)
256	4	72
512	8	72
1024	16	18

Table.1. Block size and Number of rounds

IV. KEY INJECTION SCHEDULING



V. RESULTS AND CONCLUSION

CIPHER OUT PUTS Following are simulated results of three fish block cipher algorithm implemented in virtex-5 kit with the help of Xilinx ISE 12.1.

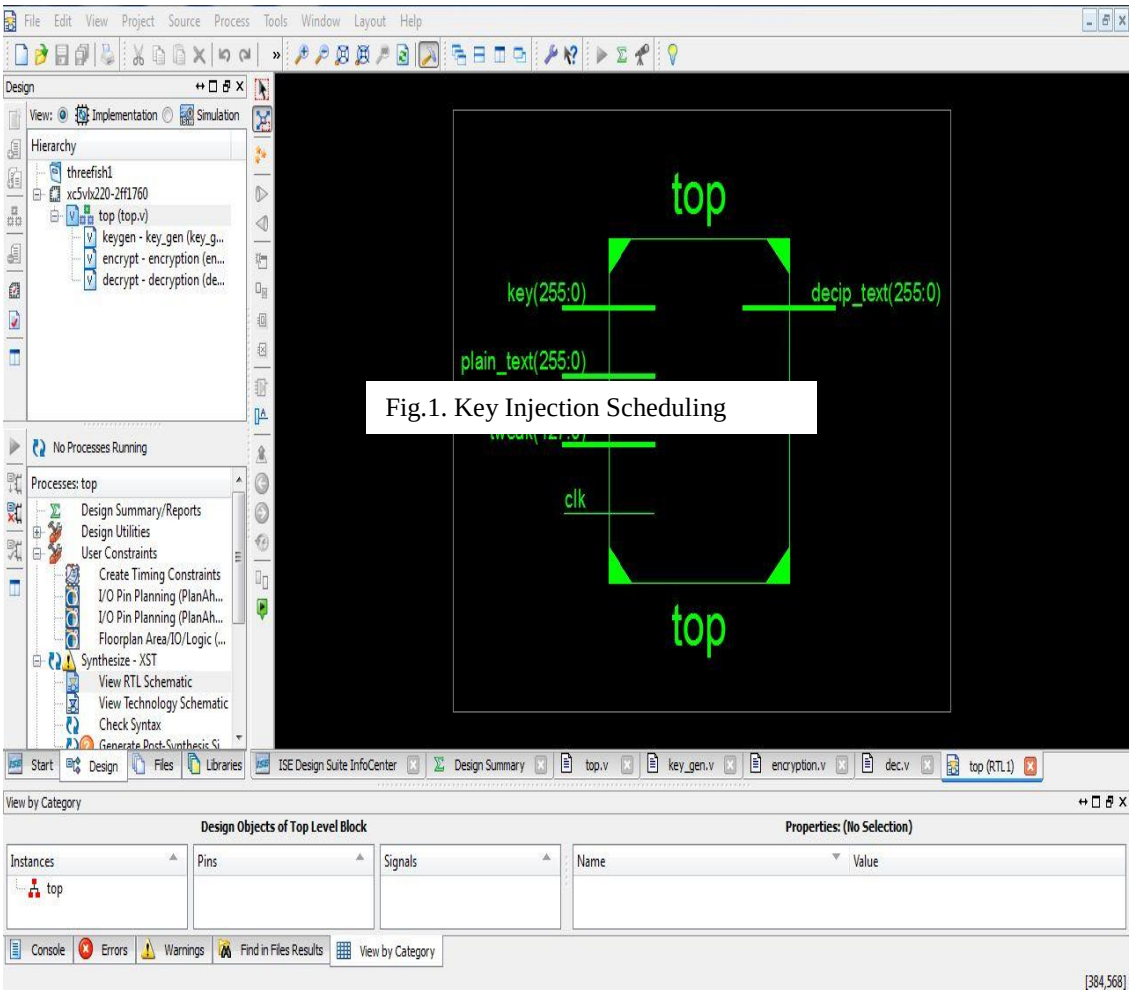


Fig.1. Key Injection Scheduling

CIPHERED OUT PUTS

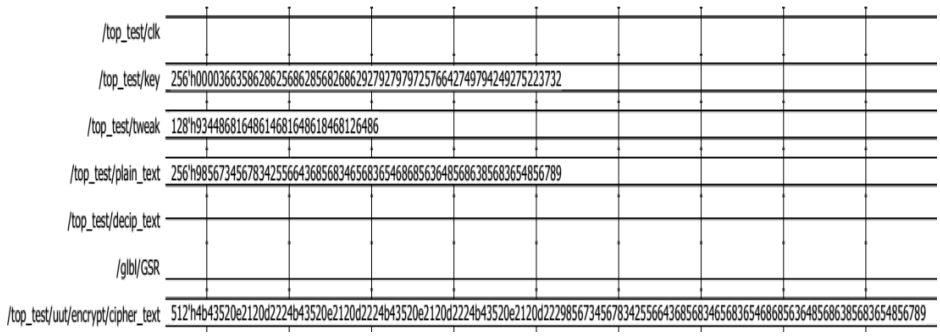


Fig.3. a) .Ciphered output

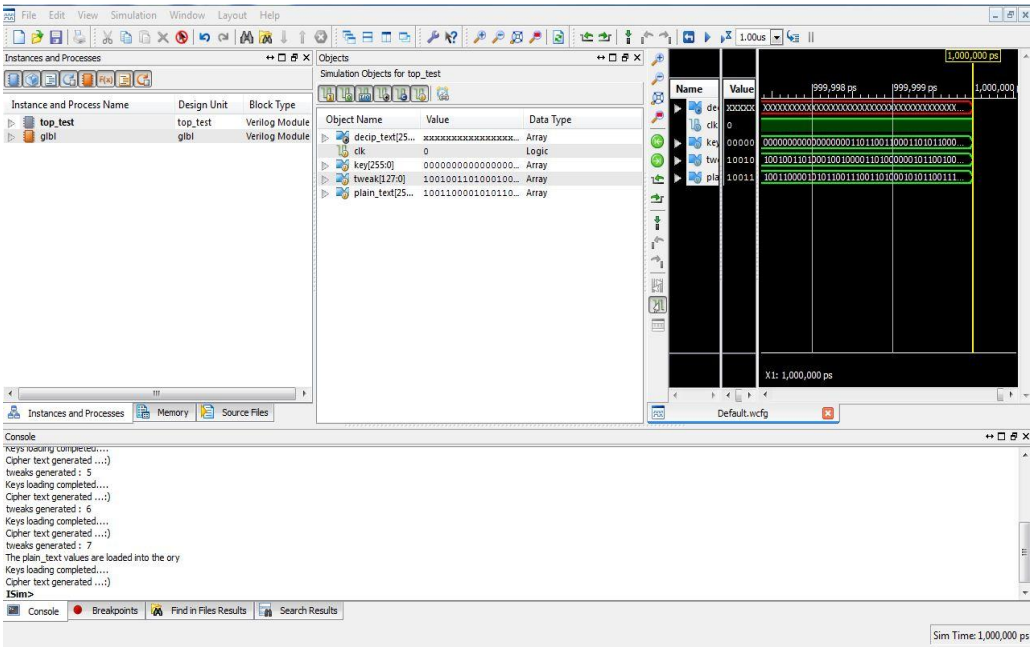


Fig. 3. b). Ciphered output

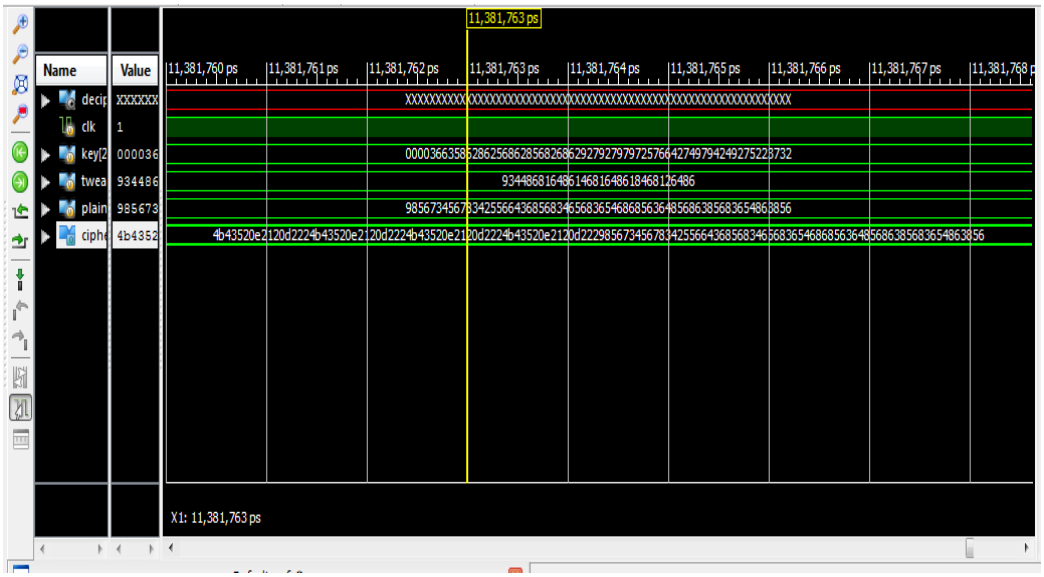


Fig. 3. c). Ciphered output

VI. CONCLUSION

- It has been noted that 14.2ns for 256 bits of input data and is very low compared to 128 bits AES encryption standard.
- The improvement has been observed to be 45.78% as compared to classical DES technique.
- The key length can be reduced, keeping the same security, in order to optimize the utilization of resources.
- The few gaps have been covered but still a lot of work can be done for the increase in security of the data along with the optimization of resources.

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