2nd International Conference on Science, Technology and Management
University of Delhi (DU), Conference Centre, New Delhi (India)
27 September 2015, www.conferenceworld.in, www.icstmdu.com
978-81-931039-6-8

DESIGN AND IMPLEMENTATION OF 8X8 DRAM MEMORY ARRAY USING 45nm TECHNOLOGY

S.Raju[1], K.Jeevan Reddy[2] (Associate Professor)

Digital Systems & Computer Electronics (DSCE),
Sreenidhi Institute of Science & Technology, Hyderabad, (India)

ABSTRACT

Process variation like threshold voltage variation, gate length variation will greatly impact the scalability, reliability, power consumption and performance of future microprocessors. All these variations are harmful to 6T SRAM structures and will become critical with continued technology scaling. A memory architecture using 3T1D DRAM cells in the L1 data cache tolerates wide process variations with little performance degradation, making it promising choice for on-chip cache structures for next generation microprocessors. The proposed memory array is designed using 3T1D DRAM cells in 45nm technology. The average power consumption, write access time, read access time and retention time of 3T1D DRAM cell have been analyzed. In this paper an effort is made to design 8x8 DRAM memory array. The 8x8 DRAM memory has been designed, implemented & analyzed in gpdk045 technology library using cadence tool.

Keywords*: *3T1D DRAM Cell, Access Times, Power Consumption, DRAM, Cadence, gpdk045.

I. INTRODUCTION

Memories are the circuits that store digital information in large quantities. Semiconductor memories are classified on the basis of functionality, nature of storage mechanism and their access patterns. For data storage and data transmission soc designs require a great amount of embedded memory devices. Two types of memories used in the modern day architecture are Read only memory (ROM) and Random access memory (RAM). Random access memories are two types namely SRAM and DRAM.SRAM is static in nature-it is a non volatile memory. SRAM is faster compared to DRAM. 70% of the chip area in soc is occupied by SRAM memory because SRAM memory cell requires 6 transistors to store a single bit of data. These are mostly used as L1-data cache memories .DRAM stores data in a capacitor in the form of charge. Capacitor leaks charge over time, the information eventually fades unless the capacitor charge is refreshed periodically.

Because of this refresh requirement it is a dynamic memory. They require less number of transistors to store a single bit of data. These are mostly, used as main memories. The process variation deviates the size of the transistor from the specified size causing device mismatches.

Mismatches reduce the reliability. Process variation limits 6T SRAM performance scalability by causing variation in the operating speed of individual cell and memory lines. An alternative design that can replace 6T cell is that of the 3T1D DRAM cell, which promises operating speeds comparable to that of SRAM without the destructive reads of the standard 1T DRAM [1]. Cadence tool is used to design DRAM. The technology file attached is gpdk045. DRAM array is constructed using the basic 3T1D DRAM cell. The paper aims to propose

978-81-931039-6-8

the design for 8bytes (64 bits) memory using schematic editor virtuoso. Peripheral circuits like pre-charge circuit, write and read control circuit, sense amplifier, column and row decoders are to be designed and implemented. The project aims to implement the memory array and perform successful write and read operations.

II. BACKGROUND

The paper on "capacitor less dram cell design for high performance embedded system" discuss about the memory cell and its performance [2]. The increasing demand for large data storage has driven the fabrication technology and memory development toward more complex design rules. The amount of memory required for system depends on the type of application. The memory capacity has reached 1 GB. The trend towards higher storage capacity will continue to push the leading edge of digital system design. Section 3 discuss about the DRAM architecture, section 4 about its implementation. Section 5, 6 describes the experimental results and conclusion respectively.

III. DRAM ARCHITECTURE

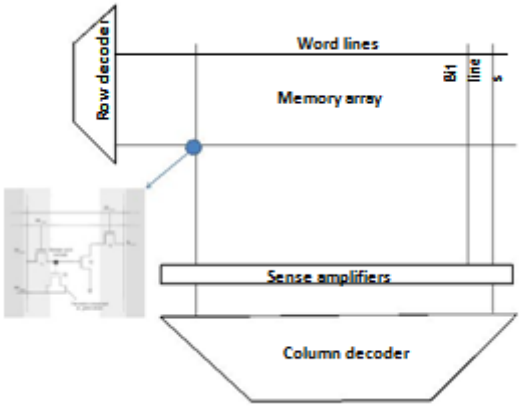


Fig 3.1 Typical DRAM Block Diagram

DRAMs can be organized as bit oriented or word oriented fashion. In bit orientation each address accesses a single bit. In word orientation each address accesses a word of n bits. A DRAM cell must be designed in such a way that it provides a non-destructive read operation and a reliable write operation. the main building blocks of DRAM memory array are as follows

1. DRAM cell
2. Pre-charge circuit
3. Read and write control circuit
4. Sense amplifier
5. Row and column decoder.

IV. DESIGN AND IMPLEMENTATION

4.1 The DRAM Cell

3T1D DRAM uses a gated diode instead of a capacitor to store the data value. The gated diode acts as a storage node, a voltage controlled capacitor and an amplifier for the cell voltage [3]. The absence of capacitor reduces the power consumption as compared to the other DRAM cell designs.

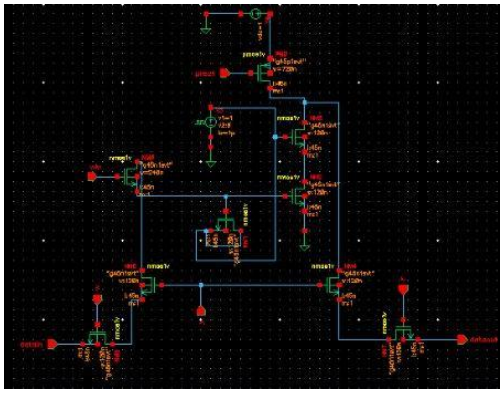


Fig 4.1 3T1D Memory Cell

The above fig sows the memory cell. The gated diode is connected to a read bit line BLW via a write device (w_g) forming a write path. The read select device (r_s) and read device (r_g) are connected in series between the read bit line (BLR) and ground forming a write path. Write word line (wlw) select the cell for writing and read word line (wlr) select the cell for reading. '0'V for 0-data and "VDD-V_{TH}" for 1 data is written into the storage node from bit line write via 'w_g', by raising wlw high and holding wlr low. In order to read the cell the read bit line BLR has to be pre-charged at V_{DD} level. For read wlr is pulsed from low to high. For read 1 the gated diode capacitance is large as the channel is on, the storage node voltage is boosted high and turns 'r_g' on. For read 0, Cgs is small as the channel is off and 'V_c' is almost at ground and rg remains off. During read bit line read drops towards ground via 'rs' and 'rg' for 1, and holds at V_{dd} for 0-data and the difference is detected by a gated diode sense amplifier. At the end of the read 'wlr' returns to ground.

4.2. The Pre-Charge Circuit

Pre-charge circuit is one of the essential components in the DRAM memory array for non-destructive read operation.

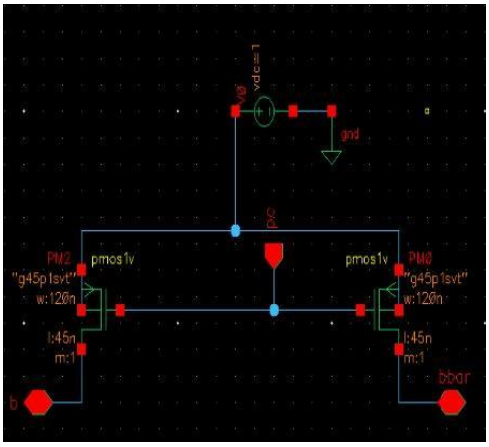


Fig 4.2 Pre-Charge Circuit

978-81-931039-6-8

The primary function of the pre-charge circuit is to charge the bit and bit bar lines to Vdd. Bit and bit bar lines are charged to Vdd before every write and read operation. The width required for PMOS is min 120 nm and length is fixed to 45 nm. For each column one pre-charge circuit is used.

4.3. Write and Read Control Circuit

Fig 4.3 Write and Read Control Circuit

The column is selected prior to the write and read control signals are enabled. Data input is passed on to the write bit line by enabling the write signal. Output data is collected from the read bit line after enabling the read signal.

4.4. Sense Amplifier

Sense amplifier is an important component in the memory array design. Here we are using voltage based sense amplifier circuit. It amplifies the small differential voltage.

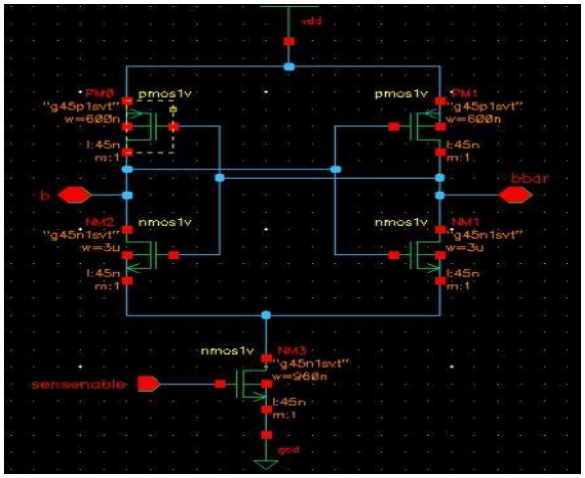


Fig 4.4 Sense Amplifier Circuit

The primary function of the sense amplifier is to amplify a small differential voltage developed on the bit lines to full swing digital signal thus reducing the time required for a read operation.

978-81-931039-6-8

4.5. Row Decoder and Column Decode

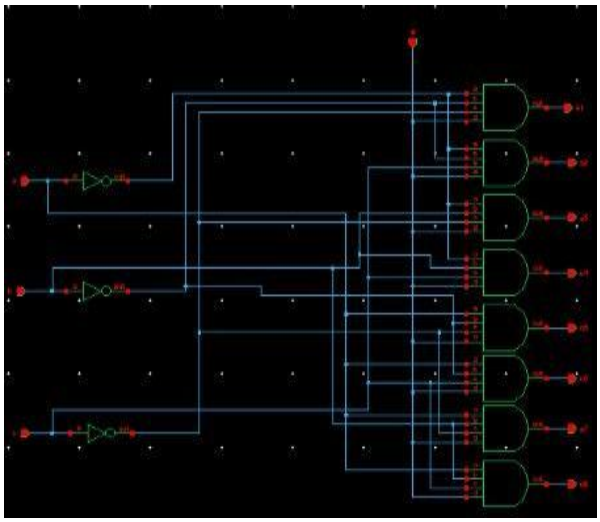


Fig 4.5 Row and Column Decoder Circuit

The schematic shows AND gate based 3 to 8 decoder with one enable input.

The function of the row decoder is to select a particular row or word line depending on the inputs A, B, C and E(enable). The output of the row decoder acts as a word line to each row. For example consider A=B=C=E= '1' then 8th word line will be selected and data will be written in to that selected cell. Column decoder is used to select a particular column for write and read operation.

Simulation of 3T1D cell is carried out for 0-200ns. During this interval write '1',read '1',write '0',and read '0' are executed, average power consumption is calculated and listed below.

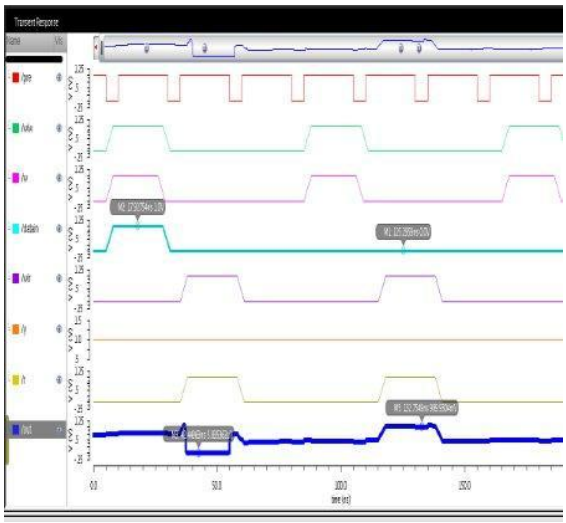
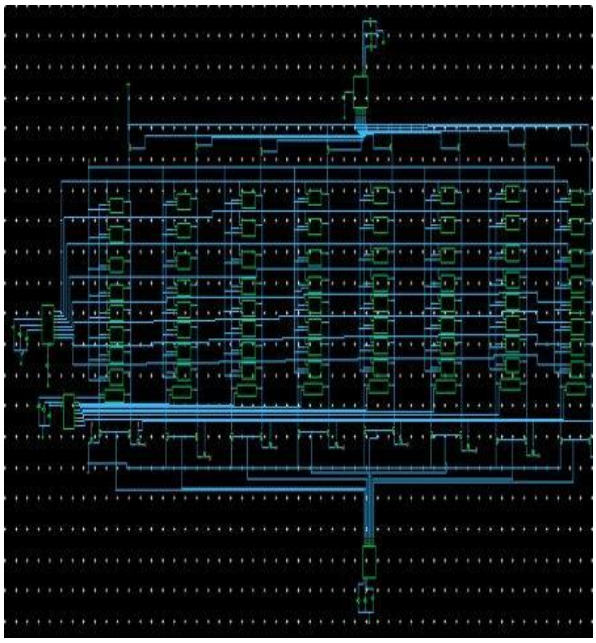


Fig1.Simulation Waveform of the 3T1D Memory Cell

Schematic of 8x8 DRAM memory is shown below.

978-81-931039-6-8



The 8x8 memory array is capable of storing 64 bits. it consists of 64 bit cells ,8 sense amplifiers, and 8 pre-charge circuits. Here first we pre-charge the bit lines to VDD before each write and read. Before reading the data sense enable signal goes high to '1' this will sense the difference between two bit lines and then gives the output. If we have written '1' into the memory cell, we will read it as '0' at the output.

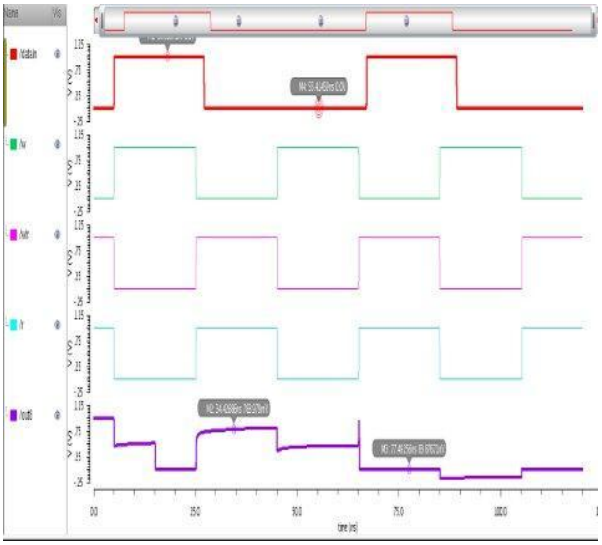
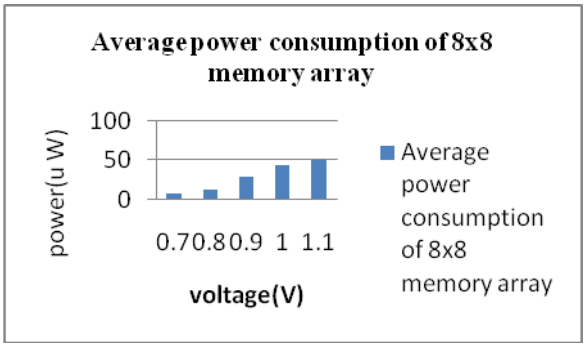


Fig2.Simulation Waveform of the 8x8 Memory Array

Table 1: Average Power Consumption of the 8x8 Memory Array.

SUPPLY VOLTAGE(V)	AVERAGE POWER CONSUMPTION OF 8X8 MEMORY ARRAY (u Watt)
0.7	8.851
0.8	13.29
0.9	36.06
1	44.86
1.1	50.33



V. PERFORMANCE ANALYSIS

Average power consumption of single 3T1D memory cell and 8x8 memory array are carried out. The average power consumption values are calculated with varying the supply voltage from 1.1V to 0.7V. read access time, write access time and retention time of 3T1D memory cell are also calculated with varying supply voltage from 1V to 0.7V.

Table 2 Average Power Consumption of the 3T1D Memory Cell

SUPPLY VOLTAGE (volt)	AVERAGE POWER CONSUMPTION OF 3T1D MEMORY CELL (n watt)
0.7	138.6
0.8	166.6
1	228.3
1.1	262.4

978-81-931039-6-8

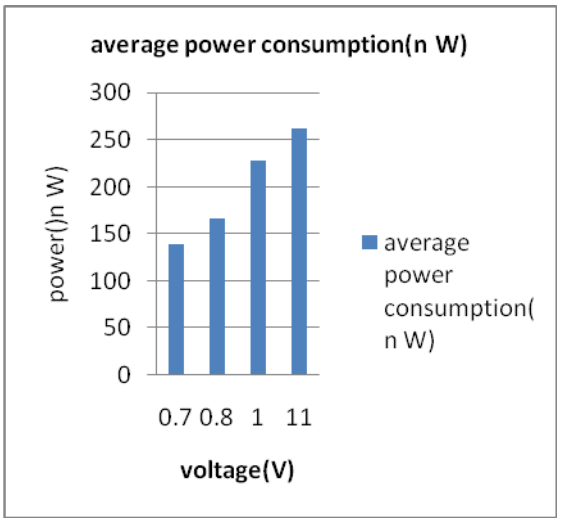
Table 3. Read Access Time with Supply Voltage

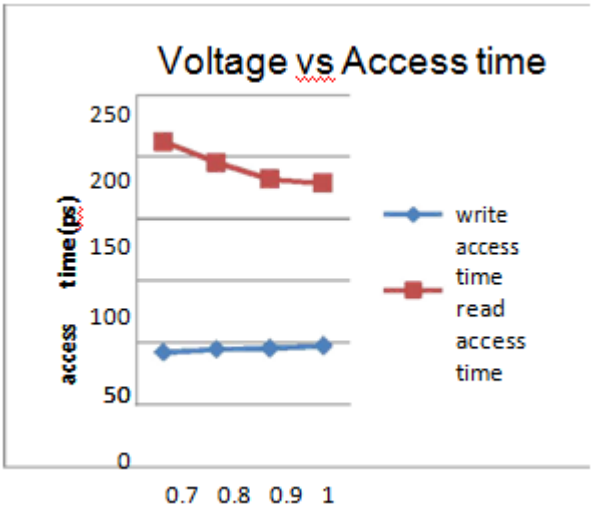
SUPPLY VOLTAGE (volt)	READ ACCESS TIME OF 3T1D CELL (p secs)
0.7	212.4
0.8	195.3
0.9	182.1
1	178.7

\

Table 4.Write Access Time with Supply Voltage

SUPPLY VOLTAGE(V)	WRITE ACCESS TIME OF 3T1D CELL(P sec)
0.7	42.3
0.8	44.8
0.9	45.6
1	47.7





VI. CONCLUSION

Analysis of 3T1D memory cell for average power consumption, read access time, write access time and retention time is carried out by varying supply voltage from 0.7V to 1.1V. The schematic is designed to store 64 bits i.e. 8x8 memory array. The array includes memory bit cell, pre-charge circuit, write read control circuit and sense amplifier are designed and integrated. This integrated array is capable of storing 64 bits. This proposed array consumes 50.33uW power to write and read 1&0 at 1.1V power supply and gradually decreases with decreasing power supply. The dram array is designed and implemented in standard gpdk045nm technology using cadence tool for schematic.

REFERENCES

[1]. [1].Yogesh N. Thakre, Shubhada S. Thakre, Devendra S. Chaudhari "An effect of process variation on 3T1D DRAM" in International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July-2013 ISSN 2229-5518

[2]. [2].Prateek Asthana and Sangeeta Mangesh "Capacitor less DRAM cell design for high performance embedded design" in international conference on advances in computing, communications and informatics (ICACCI)978-1-4799-3080-7/14/$31.00_c 2014 IEEE.

[3]. [3] W. Luk, J. Cai, R. Dennard, M. Immediato, and S. Kosonocky, "A 3- transistor dram cell with gated diode for enhanced speed and retention time," in VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on, 2006,

[4]. 184–185.

[5]. S. G. R. C. Nivard Asymerich, "Impact of positive bias temperature instability (pbti) on 3t1d-dram cells." in VLSI Journal, vol. 45. Elsevier, 2011, pp. 246–252.

[6]. K. Lovin, B. Lee, X. Liang, D. Brooks, and G.-Y. Wei, "Empirical performance models for 3t1d memories," in Computer Design,2009. ICCD 2009. IEEE International Conference on, Oct 2009, pp. 398–403.

[7]. E. Amat, "Strategies to enhance 3t1d dram cell variability robustness," pp. 1–6, 2013.

[8]. Arpit Yadav, Prof. Aruna Tete "design of process variation 3T1D based DRAM using cadence" in International Journal of Emerging Technology and Advanced Engineering ISSN 2250-2459, Volume 2, Issue 6, June 2012.