DESIGN AND SIMULATION OF 0.18 MM CMOS LNA
FOR UWB SYSTEM

Arun Sharma¹, Jaikaran Singh², Mukesh Tiwari³

¹,²,³Department of Electronics & Communication Engineering, SSSIST, Sehore, Bhopal(M.P.) (India)

ABSTRACT
In this paper, 0.18 µm CMOS LNA for UWB systems has been simulated. The resistive-capacitive feedback is used to increase the stability of the circuit. The value of $S_{21}$ is 26.577dB at 8.894GHz. The noise figure of the simulated circuit is 1.235dB at 3.1GHz. The $S_{11}$ is -27.590dB and the value of $S_{22}$ is -29.092dB which shows good impedance matching at input and output port. The proposed circuit has cascade and cascode connection of transistors.

Keywords: LNA; Mixer; Noise Figure; SNR; UWB

I. INTRODUCTION
In RF receiver systems, Low Noise Amplifier (LNA) is very essential block which is used to increase the power of signal as well as to decrease the noise figure [1]. The S parameters are used to judge the performance of LNA. The $S_{21}$ gives the value of gain for LNA, $S_{11}$ tells about the matching at the input port, $S_{22}$ gives the information about the matching at the output port and $S_{12}$ is used to measure the reverse isolation. The noise figure is the ratio of SNR at input port to the SNR at the output port. For a good LNA, $S_{21}$ should be as high as possible and $S_{11}$ should be negative (in db) so that no power get reflect at the input port. For the maximum power at the output port, the $S_{22}$ should also be negative (in dB) [3]. For high SNR at the output, low noise figure is preferable.
CMOS LNA is on today's focus because of its low cost, small size & low power consumption. The block diagram of RF receiver systems is shown in Fig. 1. The block next to LNA is mixer which translates the RF signal into the IF signal. The amplifier is connected next to mixer whose function is to amplify the signal at last stage. The performance of the mixer and amplifier circuits depends on the LNA performance [3].

![Fig. 1 RF Receiver System](image)

Federal communication commission has allocated the frequency 3.1GHz to 10.6GHz in the unlicensed band which is known as Ultra Wide Band (UWB). For the local area network, UWB provides the high data rate. The speed of
100Mbps can be achieved and the bandwidth of greater than 500MHZ. The FCC has put the limitation on the power of UWB signal so that unlicensed frequency signal should not interfere with the licensed frequency signals. The various topologies are used in designing the LNA. Source degeneration is used for input impedance matching. Cascade topology helps in increasing the gain, cascode topology enhances the bandwidth of the circuit and R-C feedback provides the stability to the circuit but the gain gets decreases[1]. There is a tradeoff between the various parameters of LNA. The input and output impedance matching can also be done by connecting the matching circuit at input & output respectively.

II. CIRCUIT DESIGN

The designed CMOS LNA circuit for UWB systems is shown in Fig. 2. The various components are connected in the circuits which helps in improving the performance of LNA. Inductor L2 is used for source degeneration technique so that input of M1 seems to be resistive which is given by

$$Z_n = Z_s + \frac{1}{sC_{gs}} + \frac{2g_m}{sC_{gs}}$$

where $Z_s$ is the parallel combination of $L_2 || C_{gs}$. By adjusting the value of frequency & $L_s$, the impedance can be made resistive. $L_1$ and $C_1$ are used for the impedance matching at the input port for low value of $S_{11}$ or for transferring the maximum power. The cascode topology has been used to reduce the reverse isolation means to reduce the load effect on the input impedance. Transistors M2 and M6 are connected in cascode with M1 as shown in Fig. 2. Shunt feedback topology has been used for increasing the stability of the circuit. By using the R1 as shunt feedback, the gain of the circuit gets decreases so transistor M6 is connected in cascaded with M3 to provide the better gain. The parallel combination of $L_5$ and $C_2$ is used to provide the filtering. Parallel connection of $L_6$ and $C_3$ is used for output filtering. M4 is used as biased current. The noise figure for an LNA circuit is given by

$$NF = 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L}$$

where

$\gamma = $ Constant

$\alpha = $ Constant

$R_S = $ Source Resistance

$R_L = $ Load Resistance
Fig. 2. The Proposed Circuit

At input side the shunt feedback resistance is approximately equal to the \( \frac{R_1}{1-A_v} \) resistance.

The dependent current source will be equal to the MOFET transconductance with the \( v_{gs} \) i.e. \( g_m v_{gs} \). The transconductance of MOSFET is given by

\[
g_m = \frac{2I_D}{V_{OV}} \quad (3)
\]

\& \quad V_{OV} = (V_{GS} - V_t) \quad (4)

III. SIMULATION RESULTS

The simulation results are shown in following figures. The simulation result for gain of LNA i.e. \( S_{21} \) is shown in Fig. 3.

Fig. 3. Simulation Result for \( S_{21} \) versus RF Frequency
The maximum value of gain is 26.577 dB at 8.894 GHz. In the whole frequency range, the $S_{21}$ is somewhat constant.

The noise figure simulation is shown in Fig. 4.

![Fig. 4. Simulation Result for Noise Figure versus RF Frequency](image)

The minimum noise figure is 1.235 dB which tells good behaviour of LNA.

The $S_{11}$ simulation result is shown in Fig. 5.

![Fig. 5. Simulation Result for $S_{11}$ versus RF Frequency](image)
The $S_{22}$ simulation result is shown in Fig. 6

![Graph showing $S_{22}$ simulation result]

**Fig. 6. Simulation Result for $S_{22}$ versus RF Frequency**

**IV. CONCLUSION**

The CMOS LNA is proposed with 0.18 $\mu$m technology. The maximum value of gain is 26.577dB at 8.894GHz. The reflection at the input port is -27.590dB and the reflection at the output port is 29.092dB. The minimum value of noise figure is 1.235dB at 3.1GHz. The proposed circuit has cascade and cascode connection of transistors.

**REFERENCES**


