

AN EFFICIENT ADIABATIC FULL ADDER DESIGN APPROACH FOR LOW POWER

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ABSTRACT

In this paper authors are going to compare the full adder using TG with full adder using energy recovery logic PFAL. Even though transmission logic is very efficient in power consumption but adiabatic technique PFAL is also an energy reused method. By adiabatic technology, charge stored on node capacitance can be recycled back and used as power clock. The full adder designed with positive feedback adiabatic logic has better performance than previous design and all results were verified with Tanner V.7. Various types of parameters such as power dissipation, transistor count and power supply were compared of both methods on T-Spice tool.

Keywords: *Adiabatic Logic, Full adder using TG and PFAL, PFAL, TG, T-SPICE.*

I. INTRODUCTION

As in designing of conventional static and dynamic CMOS logic, the circuit performance is necessary in parameters of logic levels, input supply but not in the case of power consumed by the conventional circuits. To obtain less power consumption, the best technique is implemented like reduce the supply voltage, factor .consequently; the design gives us degraded performance [1]. To overcome this problem, the method is introduced works on energy recovery principle known as adiabatic logic. Adiabatic circuits are those circuits in which energy is recycled back to threshold voltage and no energy is wasted [2]. In this paper, author have designed full adder by using adiabatic technique and compare with existing TG design. Before this, I have studied various approaches that are used to minimize the power dissipation of various electronic circuits. Full adder is a circuit which adds three bits and gives the two binary outputs, sum and carry. It is widely used in applications like digital signal processing (DSP), and microprocessor. Different types of full adder were discussed in various papers over the past decades. The one of the main adders are ripple carry adder, carry look ahead adder and parallel binary adder. In the present paper, the performance analysis of full adder has done with TG logic and adiabatic logic PFAL. In transmission gate logic, the PMOSFET and NMOSFET switches are connected in parallel form and consecutively works as transmission gate. It is observed that high number of internal nodes can increase parasitic capacitances and ultimately circuit complexity becomes increase. So, power consumption of the circuit enhance in many large arithmetic circuits. The circuit design with TG logic is very complicated and takes more delay for logical operation during transition [3].

The rest paper describes as: section 2 gives the basics of full adder and logic design styles. Section 3 shows the simulation results of TG and adiabatic PFAL. Section 4 demonstrates the conclusion. At last, References have

II. LOGIC DESIGN STYLES

2.1 Full Adder

Full adder is a combinational circuit that performs the addition of 3 binary digits. The input variables are represented by A, B, C_{in} . A and B represent the 2-input variables and C_{in} represents the carry from the previous lower significant position. In the full adder, whenever we add two binary numbers, each having two or more binary bits, the least significant bits can be added using half adder. The logic symbol of full adder is shown in "Fig. 2".

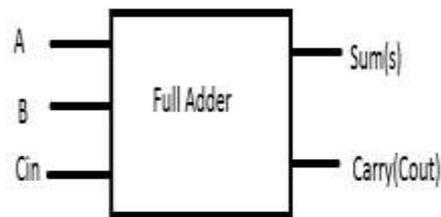


Figure 2 Logic Symbol For Full Adder[7].

Full adder basically accepts 3 inputs and produces 2 outputs sum and carry. As compared to half adder, full adder takes the value of carry input to handle the additional input carries.

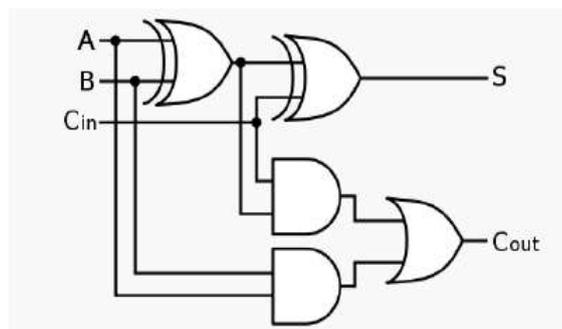


Figure 2.1 Logic Diagram for Full Adder [7].

From the Fig 2.1, it is clear that sum(S) is the XOR of A, B and C_{in} and carry is designed with the combination of AND and OR gate. The output of first exor gate is the input of AND gate and another input C_{in} is also applied. Similarly, the inputs A and B also applied to the AND gate .As a result, the OR gate gives the result of Carry output [7].

2.2 TG Based Full Adder

The implementation by TG uses 14 transistors so power consumption and area is larger in TG circuit. The transistor count is more so the area for circuit is also more.

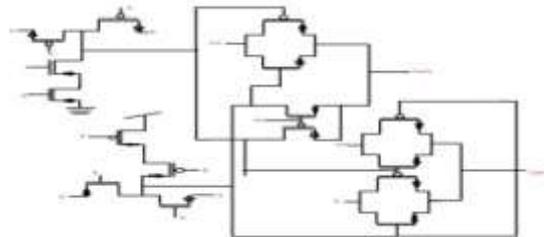


Figure 2.2 TG Based Full Adder [8] .

Two TG based ports are used to realize the function of full adder. One is used to implement the sum expression and other for carry [8].

2.3 PFAL Based Full Adder Sum

The PFAL logic consists of a two cross coupled inverters and two functional blocks F and F/. These functional blocks are used for logic operation. The pull up network is designed with combination of NMOS and PMOS. When the inputs a, b and c are at logic 001 and V_{DD} move up from lower position to higher position of constant supply then F-array sum store data one. Sum/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then sum/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded. When the inputs a, b and c are at logic 010 and V_{DD} move up from lower position to higher position of constant supply then F-array sum store data one. Sum/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then sum/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded. When the inputs a, b and c are at logic 100 and V_{DD} move up from lower position to higher position of constant supply then F-array sum store data one. Sum/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then sum/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded. When the inputs a, b and c are at logic 111 and V_{DD} move up from lower position to higher position of constant supply then F-array sum store data one. Sum/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then sum/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded.

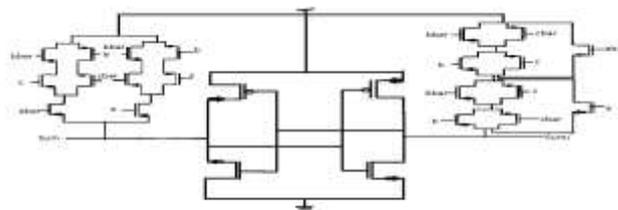


Figure 2.3 PFAL Based Full Adder Sum.

2.4 PFAL Based Full Adder Carry

The PFAL logic consists of a two cross coupled inverters and two functional blocks F and F/. These functional blocks are used for logic operation. The pull up network is designed with combination of NMOS and PMOS. When the inputs a, b and c are at logic 011 and V_{DD} move up from lower position to higher position of

constant supply then F-array carry store data one. Carry/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then carry/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded. When the inputs a, b and c are at logic 101 and V_{DD} move up from lower position to higher position of constant supply then F-array carry store data one. Carry/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then carry/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded. When the inputs a, b and c are at logic 111 and V_{DD} move up from lower position to higher position of constant supply then F-array carry store data one. Carry/ charge the capacitor up to the threshold level. Now V_{DD} fall from higher position to lower position then carry/ gives its energy back to V_{DD} , no energy of V_{DD} is grounded.

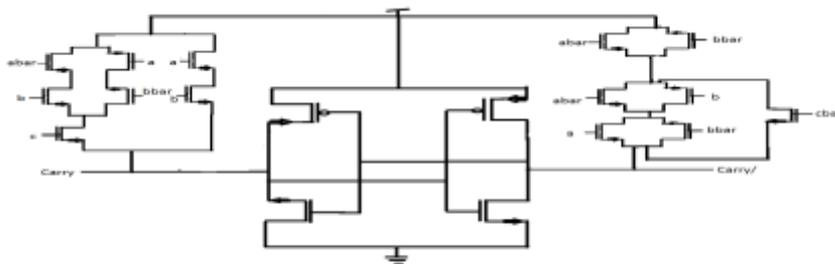


Figure 2.4 PFAL Based Full Adder Carry.

III. SIMULATION RESULTS

In this paper different logic styles, TG and PFAL logic were used to design full adder. This full adder was implementing using T-spice of TANNER tool on 0.18um technology. The graphical representation of two styles is shown below.



Figure3 Simulation results of full adder using TG.

Fig. 3 describes the graphical waveform of full adder with TG logic. The bottom one line is the output signal and top four are input signals.

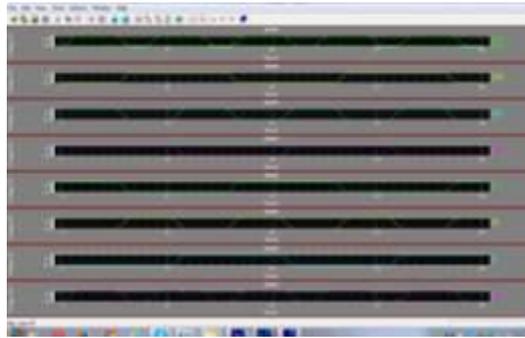


Figure 3.1 Simulation results of full adder sum using PFAL.

Fig. 3.1 describes the graphical waveform of full adder with PFAL logic. The bottom two lines are the output signals and top seven are input signals.

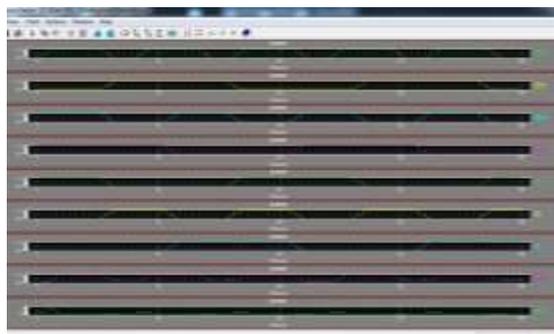


Figure 3.2 Simulation results of Full Adder Carry using PFAL.

Fig. 3.2 describes the graphical waveform of full adder with PFAL logic. The bottom two lines are the output signals and top seven are input signals.

3.1 Comparison of Proposed With Existing Design

The comparison between the TG and PFAL based full adder has done in various terms such as power supply, transistor count and power dissipation. The transistor count is higher in PFAL but it dissipates least energy as heat at node capacitance. In Fig.3.3 the TG and PFAL logics are compared as TG has average power of $16.7\mu\text{w}$ with proposed design power of only $15.38\mu\text{w}$.

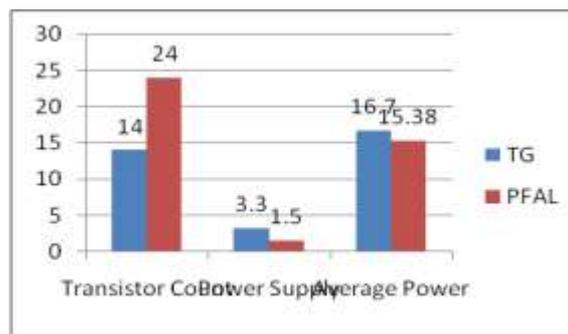


Figure 3.3 Comparison of proposed and existing design with different parameters.

Table1. Table shows the Comparison between Existing and Proposed Full Adder

Parameters	TG(Transmission Gate)	Proposed
Function	Full Adder	Full Adder
Technology (nm)	250	180
Supply Voltage (V)	3.3	1.5
Power dissipation(μ w)	16.7	15.38

IV. CONCLUSION

The full adder using adiabatic logic such as PFAL compared with the TG (transmission gate) against the parameter variation. The result verified that the adiabatic full adder shows the better power result against all the parametric variation as compare to TG full adder. At high frequency the PFAL based full adder shows better power saving as compare to TG. The full adder has wide range of application like ALU, DSPs etc; adiabatic full adder can be used in any application.

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