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PERFORMANCE COMPARISON OF GNRFET BASED 6T SRAM CELL WITH CMOS, FINFET AND CNTFET TECHNOLOGY

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ABSTRACT

In the world of micro and nano IC era, Complementary Metal-Oxide-Semiconductor (CMOS) technology has lost its performance credentiality during scaling down beyond 32nm. Scaling causes severe performance degradation including Short Channel Effects (SCE) which are difficult to suppress. As a result of such effects, many alternate devices have been identified. Some of the major contestants include Multi Gate Field Effect Transistor (MuGFET) like FinFET, Carbon Nano tubes, Graphene Nano Ribbon, silicon Nano wires etc. Among these, Graphene Nanoribbon plays a vital role in modern electronic VLSI design. In this paper, the CMOS transistors present in the 1 bit SRAM memory cell is replaced by GNRFETs. The performance of SRAM memory cell built by 32nm GNRFET technology is compared with CMOS, FinFET and CNTFET technology using HSPICE simulation tool.

Keywords: Carbon Nanotube, CMOS, Finfet, Graphene Nanoribbon, Power Dissipation, SRAM.

I. INTRODUCTION

Semiconductor memories are considered as the most important microelectronic components of digital logic system design, such as computers based application. Semiconductor memory arrays are capable of storing large quantities of digital information which are essential for all digital systems. The amount of memory required in a particular system depends on the type of application, but the number of transistors required for storage function is larger than for logic operations and other applications. The ever increasing demand for large storage capacity has driven the fabrication technology and memory development towards higher data storage densities. On-chip memory arrays have become widely used subsystems in VLSI circuits and commercially available single chip read/write memory capacity has reached 1 GB.

The semiconductor memory is generally classified according to the type of data storage and data access. Read/write memory or Random access Memory (RAM) must permit the change of data bits stored in the memory array, as well as their retrieval demand. The stored data is volatile.

SRAM is mainly used for cache memory in microprocessor, mainframe computers, engineering workstations and memory in handled devices due to high speed and low power consumption. Memory cells are constructed

using transistors. The number of transistors used in a single chip may increase drastically for every years based on Moore's law, [1]. Even though they provide high speed of operation, lower leakage and reduced transistor count, they become less efficient when the area decreases below 32nm. International technology Roadmap for semiconductors (ITRS) provides information about recent trends and advancement in semiconductor technology, [2].

In this paper, the CMOS transistors used in the conventional SRAM cells are replaced by Graphene Nanoribbon, to reduce power consumption and the simulation is done by using HSPICE tool. The simulation results of GNRFET-SRAM are compared with the simulation results of CMOS SRAM on the basis of power dissipation.

II. CMOS ALTERNATIVES

Many researches are being carried out in the field of SRAM. Newer technologies are coming to existence. Moore's law states that the number of transistors per square inch in an integrated circuits doubles every eighteen months but now the law is facing certain discrepancies, [1]. In the existing system, SRAM memory cells are designed using CMOS technology. It has various advantages like the circuit is very simple, consumes little power in a fixed state and also has high input impedance. Though it has these advantages, it fails when it is scaled beyond 32nm, [3], [4]. It undergoes Short Channel Effect which is an effect whereby a MOSFET in which the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction, behaves differently from other MOSFETs. As a result of this short channel effects, the power dissipated by CMOS SRAM circuit becomes very high below 32nm. The read stability and write ability are major concerns in nanoscale. Therefore, inorder to reduce the performance degradation and short channel effects, the alternate devices such as FinFET, CNTFET, GNRFET, Silicon nanowire etc have been studied experimentally,[5], [6].

2.1 FinFET

Fin-type field-effect transistors (FinFETs) are leading promising substitutes for CMOS device at the nanoscale. FinFETs are double-gate devices. The two gates of a FinFET can either be shorted for higher perfomance or independently controlled for lower leakage or reduced transistor count, [3], [7].

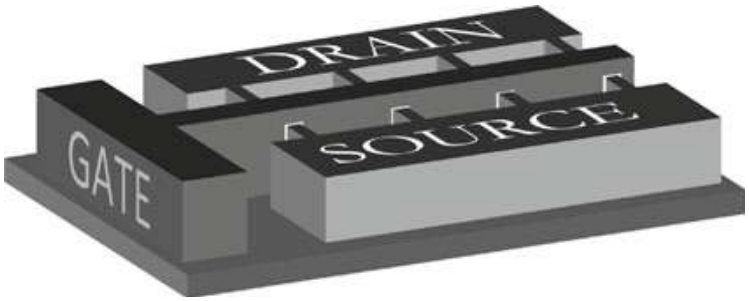

Fig. 1 Multi-fin FinFET

The FinFET device consists of a thin silicon body, wrapped by gate electrodes. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The

effective gate width of a FinFET is 2nh, where n is the number of fins and h is the fin height. Thus, wider transistors with higher on-currents are obtained by using multiple fins.

2.2 Carbon Nanotubes

Carbon Nanotubes are tubular cylinders of carbon atoms that have extraordinary mechanical, electrical, thermal, optical and chemical properties. They are of two types of nanotubes, which are single walled and multi walled Carbon Nanotubes. CNTFET (Carbon Nanotube Field Effect Transistor) utilizes a single carbon Nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure, [8], [9],[10].

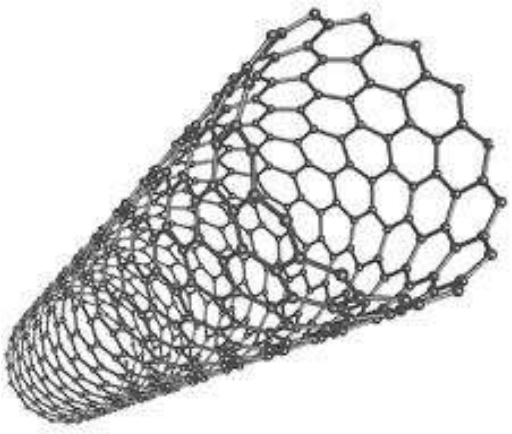

Fig.2 Carbon Nanotube Structure

Based on their folding angle and diameter, these nanotubes can be metallic or semiconductive. The band gap of semiconducting nanotubes decreases with increase in diameter. Electronic structure of carbon nanotubes makes then ideal candidates for novel molecular devices. This can also be used as an alternative for CMOS technology beyond 32nm in order to overcome its short comings .

2.3 Graphene Nanoribbon

Graphene Nanoribbon is also called as nano-graphite ribbons, are strips of graphene with ultra-thin width (<50nm). Graphene ribbons were introduced as a theoretical model by Mitsutaka Fujita and co-authors to examine the edge and nanoscale size effect in grapheme. Careful patterning of graphene laterally confined in ribbon like structure gives rise to Graphene Nanoribbons (GNRs), [11], [12],[13].

They are of two types- armchair and zigzag. In Zigzag, each segment is of opposite angle to the previous. In armchair type, each pair of segments is a 120/-120 degree rotation of the prior pair. Zigzag edges provide the edge localized state with non-bonding molecular orbitals near the Fermi energy. They are expected to have large changes in optical and electronic properties from quantization.

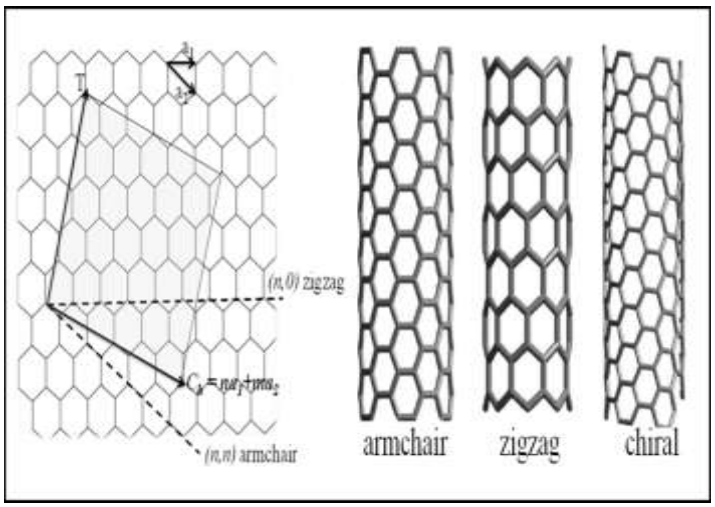

Fig.3 Graphene Nanoribbon

Calculations based on tight binding theory predict that zigzag GNRs are always metallic while armchairs can be either metallic or semiconducting, depending on their width. Density Function Theory (DFT) calculations show that armchair nanoribbon are semiconducting with an energy gap scaling with the inverse of the width of Graphene Nanoribbon. Experiments verified that energy gaps increase with decreasing GNR width.

Graphene Nanoribbons possess excellent semiconductive properties and may be used as an alternative for silicon semiconductor. Their 2D structure along with certain properties like high electrical and thermal conductivity makes GNR an alternative to copper for Intergrated circuits interconnect.

III. SRAM CELL

SRAM stands Static Random Access Memory. It finds application in CPU Cache, Personal Computers, workstations, routers, hard disk buffers and router buffers. The advantage of SRAM is that it does not require periodic refreshment unlike DRAM. It is also volatile i.e. the data is lost once the power is turned off. The construction of a 6T SRAM cell consists of 2 PMOS and 4 NMOS transistors.

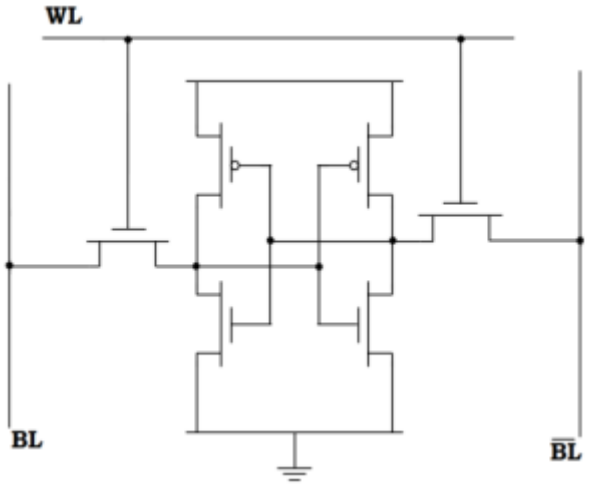

Fig. 4 6T SRAM Cell

The operation of SRAM cell is explained by considering 6T SRAM cell as an example. From the figure 3 we can understand the circuit diagram of 6T SRAM cell. The operation of SRAM can be divided into three states: read, write and hold state. During write operation, the voltage of WL is increased and Bit lines BL and BL' are raised to Vdd or with necessary values. The new bit line value overpowers the existing value. During read operation, the WL voltage is raised high, the memory cell discharges either BL or BL' depending on the stored date on the nodes Q and Q'. During Hold state, the voltage in WL is held low and the BLs are left floating or driven to Vdd. Each bit in an SRAM is stored on four transistors that form two cross-coupled. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors control the access to storage cell during read and write operation.

IV. SIMULATION RESULTS

Hailey's Simulation Program with Intergrated Circuit Emphasis (HSPICE) is software that supports the simulation of SRAM cell using Graphene Nanoribbon. Simulations are carried out to measure the power dissipated by CMOS and GNRFET (Graphene Nanoribbon Field Effect Transistor). Along with this, the power dissipated by FinFET and CNTFET is also estimated and results are tabulated to find the technology that has minimum power dissipation below 32nm, [13], [14], [15], [16].

The simulation result of 6T SRAM cell is shown below and the same is obtained for various technologies used. The first waveform represents the word line, the second waveform represents the bit line and third waveform represents the output depending on whether it is read or write operation, [17,[18].

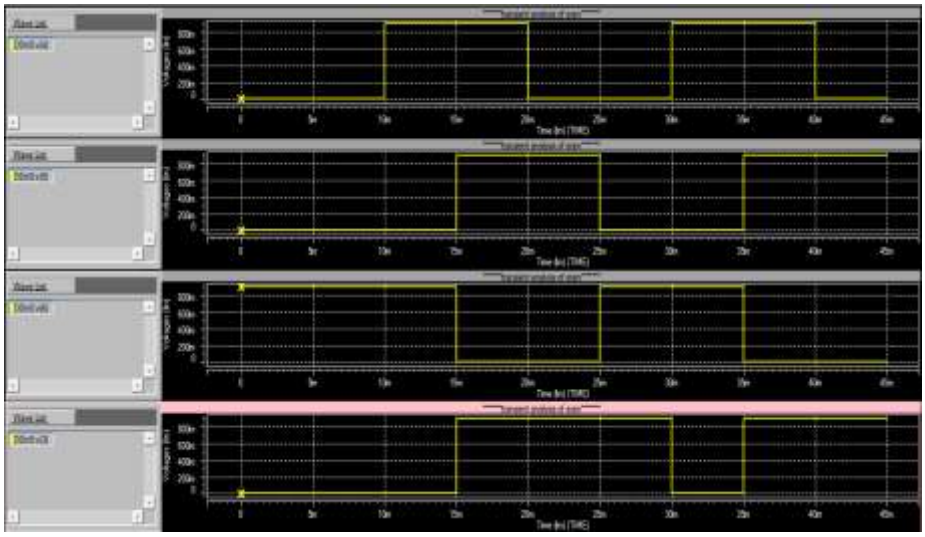

Fig. 5 Simulation Waveform of 6T SRAM cell

In the above figure, the first waveform v(4) shows bitline (BL), the second waveform v(5) shows bitline bar (BLB) and the third waveform v(6) shows wordline (WL). Finally, the last waveform shows data stored in the node 2.

These simulation is done by using model files obtained from resources available in PTM, Stanford and nanohub websites, [19],[20],[21].

V. PERFORMANCE COMPARISON

The performance of Graphene Nanoribbon based design is determined by comparing with CMOS, FinFET, and CNTFET based design. The performance are compared based on the parameters such as power consumption, total power dissipation, average delay and leakage current.

The following table shows the performance comparison of GNRFET based SRAM cell with CMOS, FinFET and CNTFET based SRAM cell design.

Parameters	**6T-SRAM Cell**			
Technology used	**CMOS based design**	**FinFET based design**	**CNTFET based design**	**GNRFET based Design**
Average power consumption	16.605nW	10.23nW	6.211 nW	8.23 nW
Total voltage source power dissipation	5.5079 nW	34.1 nW	32.90 pW	0.401nW
Average delay	0.2964 us	4.65ns	2.5049 ns	3.75ns

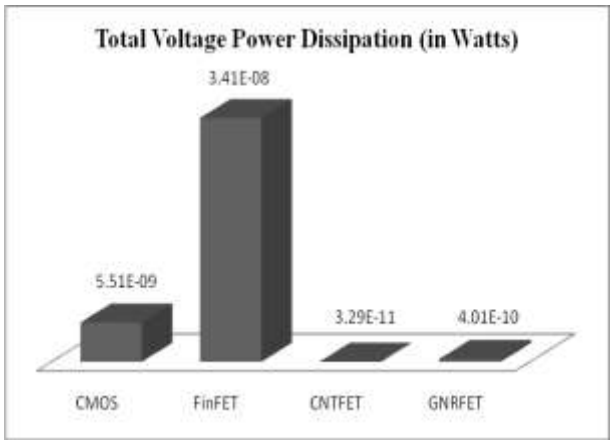

Fig. 6 Performance comparison

VI. CONCLUSION

From this it can be concluded that, though CMOS is irreplaceable, the power dissipated by GNRFET is comparatively less than CMOS. The power dissipated by CNTFET is also less than CMOS beyond 32nm. The circuit designed using GNRFET is more efficient than CMOS technology beyond 32nm. The scope of Graphene

Nanoribbon in the field of VLSI proves to be promising and paves way for a new revolution in MOSFET technology. Graphene Nanoribbon can thus be used as an alternative for CMOS beyond 32nm.

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