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INTEGRATION OF MATCHED MICROSTRIP LINE WITH CMOS LOW NOISE AMPLIFIER FOR WIRELESS APPLICATIONS

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ABSTRACT

In this work, Integration of matched microstrip line with CMOS LNA amplifier for wireless application is proposed. A novel thought of CMOS low noise amplifier achieves higher gain, low noise and best return loss. A 50Ω micro-strip transmission line as a matching network is adopted in Low noise amplifier for enhancement of wide impedance bandwidth. The circuit is simulated using 90nm TSMC CMOS technology in ADS tool. The simulation results offer impedance bandwidth of 6.3 from ranging of 12.8GHz to 18.5GHz. The highest forward gain of 15.3dB is achieved. A noise figure is around to be 2dB at 16GHz is also achieved.

Keywords: Microstrip line, Millimeter wave (MMW), CMOS Low noise amplifier (LNA)

I INTRODUCTION

Recently, fastest growth of CMOS devices in microwave based industries is establishing a big new market opportunity. Good researchers are founding continuously new solutions which would be implemented into the existing wireless system networks to provide the wider bandwidth, the high quality and new added services. A millimeter wave (MMW) frequency band is the most promising technology for providing broadband wireless communications [1]. The extensive progress of CMOS technology has enabled its application in microwave and millimeter wave technologies. Presently, the CMOS technology has became one of the most attractive choices in implementing transceiver due to its low cost and high level of integration [2]. Despite of the advantages of CMOS technology, the design of CMOS transceiver in millimeter wave applications exhibits several challenges and difficulties that the designers must overcome. In addition, Kinetic performances of active devices with LNAtch antenna have been improved, where MMW designs can be considered [3].

Low noise amplifier (LNA) is an important unit of the wireless transceiver, so designing a high performance LNA is the key to improve performance of wireless receivers [4]. However, the designing and implementation of CMOS LNA is very difficult. Demands in different aspects of the LNA require designers to consider comprehensively how indicators can compromise between one another. Today, several authors are designing a Low noise amplifier using LC matching networks and to achieve maximum LNA of 50%. In [5], two LNA is designed for 3G applications and achieves LNAE of 50%. In this work, Class AB LNA is selected as it displays

higher Low noise efficiency as well as linearity. Single-ended two-stage amplification form is used in this design. In order to achieve more efficient match, micro-strip line is adopted. This design has demonstrated a simple structure, but with high stability, as well as superior overall performance, which can be used as a transmitter for millimeter and microwave applications. The basic geometry of RF transmitter system are shown in Fig.1

II LOW NOISE AMPLIFIER

Low noise amplifiers involve a balancing of many different LNA parameters, including Low noise added efficiency (LNAE), maximum output Low noise, linearity, maximum stable gain, Low noise, stability, input/output matching, and breakdown voltage. As with many RF component designs, these requirements are often in conflict with one another. As the fulfill these requirements of LNA design, different topologies like common source (CS), Common Gate (CG) etc. are available which are briefly discuss below.

A. CMOS Topology

The common source (CS) and common gate (CG) topologies are two popular architecture choices which are widely used for LNA design. Common source structure is used in this circuit. Meanwhile, in order to achieve the gain of more than 20 dB, Low noise amplifier use single-ended two-stage amplification form. Single-ended topology can be avoided application of the balanced-unbalanced transformer [6], which could simplify the integration process and improve the cost efficiency per unit of LNA. For matching using LC networks as input and output achieves LNAE up to 50% but if adopted 50Ω transmission line like micro-strip, CPW etc then it is possible to achieve LNAE of 80%. In a micro-strip line, conductor losses increase with increasing characteristic impedance due to the greater resistance of narrow strips. Conductor losses follow a trend that is opposite to radiation loss with respect to W/h. The Low noise handling capacity of a micro-strip is limited by heating because of ohmic and dielectric losses and by dielectric breakdown. An increase in temperature due to conductor and dielectric losses limits the average Low noise of the Micro-strip line, while the breakdown between the strip conductor and ground plane limits the peak Low noise. In order to determine the optimum load, the transistor should have its input matched to the source using a micro-strip line at the centre frequency of the operating band is connected to a variable load resistance at the output node.

B. Design consideration

Fig.1 shows the basic schematic LNA circuit, it includes bias circuit, input matching network, and output matching network and inter-stage matching network. A two-stage amplifier bias circuit is composed of DC Low noise VGG1 and VGG2. The gate values of VGG1 and VGG2 are chosen as 0.6V. A suitable quiescent point is provided, so the amplifier works at the mode of Class AB. As shown in the figure, input and output ports have 50Ω impedance. The desired impedances are obtained with the help of matching circuits. The Low noise

amplifier takes a small-amplitude signal at the output RF frequency as its input and drives a high Low noise representation of the input into a lower impedance load. Generally, the load is an antenna having a resistance of 50 ohm. The purpose of the Low noise amplifier is therefore to amplify the high frequency signal to be sent by the transceiver. The LNA should be able to amplify the signal to transmit signals at Low noises high enough for the receiver to recover the desired signal. Table1. Show the design specification of LNA.

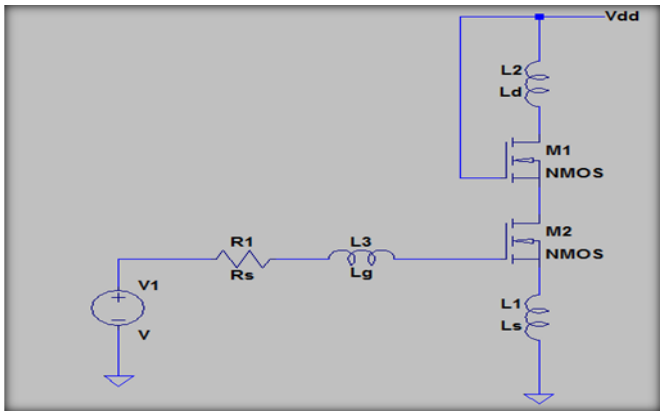

Fig.1 Basic Geometry of Low noise amplifier

Table1 Shows specifications and technology of MOS transistors

	Device Width (µm)	Length (µm)	Biasing (V)
M1	36	.09	1
M2	21	.09	1

III ANALYSIS OF THE MICROSTRIP LINE

The micro-strip line it has become the best known and most widely used planar transmission line for RF and Microwave circuits. This popularity and widespread use are due to its planar nature, ease of fabrication using various processes, easy integration with solid-state devices, good heat sinking, and good mechanical support [9]. In this LNAper, we have design a micro-strip line at 31GHz with new dimensions and simulated in ADS tool. This design work taken a RT durroid substrate with thickness of t = 0.245 mm at the height h = 10mil above a lossless ground conducting layer. The dielectric between metal layers is assumed to have = 2.36 and tan = .002. At 31GHz, a 50Ω line given these LNArameters would have a width and length is 4mm and 0.9mm respectively and the calculated with help of equation is given below. The 3D view of line is shown in Fig.2. The

resulting return loss (S_{11}) -38.08dB and gain of more than 5dBi are shown in fig3 and fig4 respectively. The surface current distribution shows direction of radiation of the line and it can be seen in fig5.

$$W_g = 6h + w \quad (1)$$

$$L_g = 6h + l \quad (2)$$

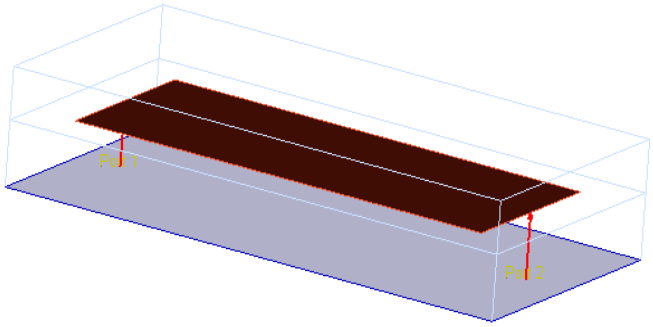

Fig.2 3D view of the designed LNAtch antenna at 40GHz

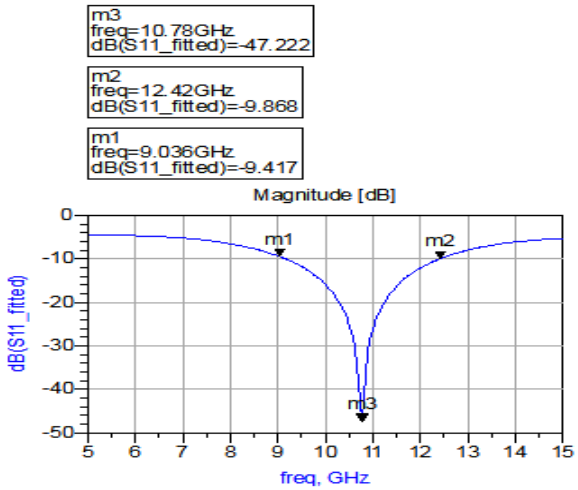

Fig.3 Return loss Vs frequency

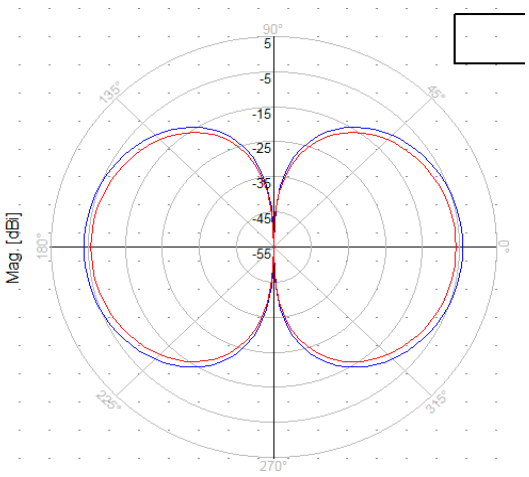

Fig.4 Radiation pattern of strip line at 10.8GHz

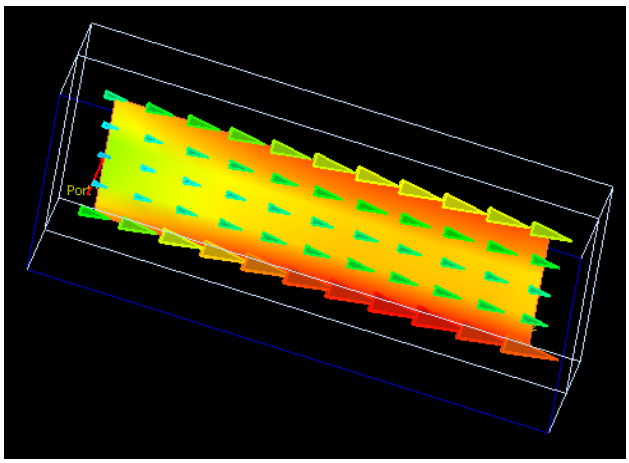

Fig5. Surface current distribution at 31GHz

IV CIRCUIT DESIGN

A 31GHz two stage of CMOS LNA is designed using 90nm commercial TSMC design kit in Agilent advanced design system. Fig6. Shows circuit schematic of LNA. LNArasitic caLNAcitances of input and output RF bond LNAds are also considered in the circuit simulation. By improving the input matching, it is possible to achieve the maximum Low noise efficiency, diminish signal distortions caused by reflection, and hence enhance linearity, further stabilize the circuit. T-circuit network is composed of C1, C2and MTL1, which could be achieved by using input impedance and source impedance (50Ω) match and achieves the good reverse isolation (S_{11}), is -34dB and 50Ω input impedance with the help of equation given below and its simulation results are shown in Fig.7 and Fig.8 respectively.

$$Zin = \frac{1}{g_m + jwC_{gs}} \qquad (1)$$

$$S_{11} = 20.log_{10}\left(\left|\frac{Z_{in} - R_s}{Z_{in} + R_s}\right|\right) \qquad (2)$$

The high LNA L-type output matching network is composed of C4and MTL6, so load impedance of 50 Ω is transformed to the best load value, thus the required output Low noise can be obtained. Selecting on-chip inductor is the key to design a matching network, because it determines the quality of the matching network. The inter-stage L-type matching network is composed by MTL4 of the first stage amplifying circuit and MIM (Metal-Insulator-Metal) capacitor C3 [7]. All dimension values of micro-strip lines are MTL1, w=0.86mm L=4mm; MTL2, w=0.62mm L=2.5mm; MTL3, w=0.62mm L=2.5mm; MTL4 w=0.62mm L=2.5mm; MTL5, w=0.62mm L=2.5mm; MTL6, w=0.62mm L=2.5mm.

The best Low noise transmission is achieved by inter-stage matching between the first stage and the second stage. This matching network could also be used to adjust the amplifier gain flatness [8]. The maximum of S_{21} is reached nearby the centre frequency of 31GHz by adjusting capacitance, thus the best Low noise added efficiency of 73% can be achieved that is shown in fig9 and fig10 respectively. The output Low noise stops

increasing after Pin=13dBm point. It is shown on the fig.11 at input Low noise of 0dBm, output Low noise Pout=11dBm.

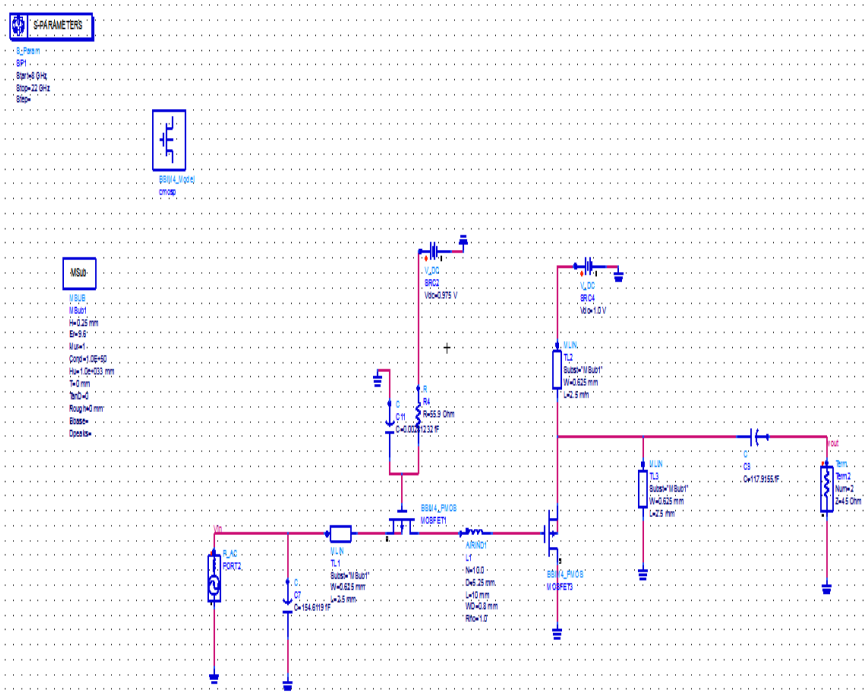

Fig.6 Complete design of receiver system at 31GHz

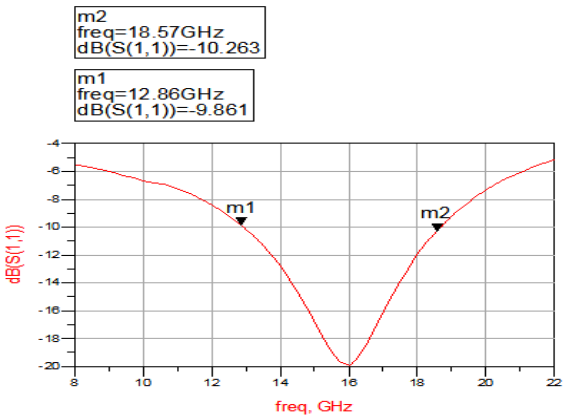

Fig.7 Return loss Vs frequency

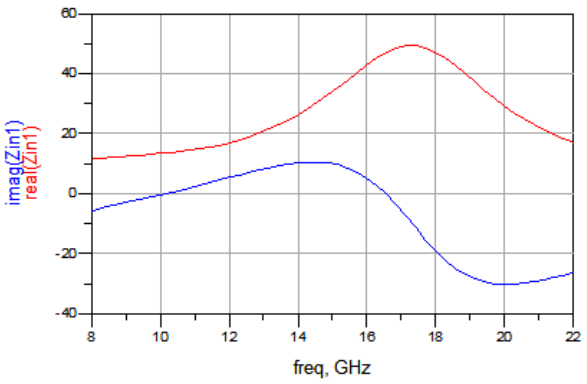

Fig.8 Input impedance Vs Frequency

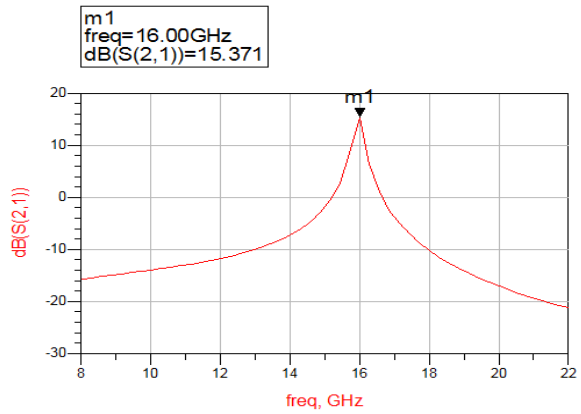

Fig.9 Forward gain Vs Frequency

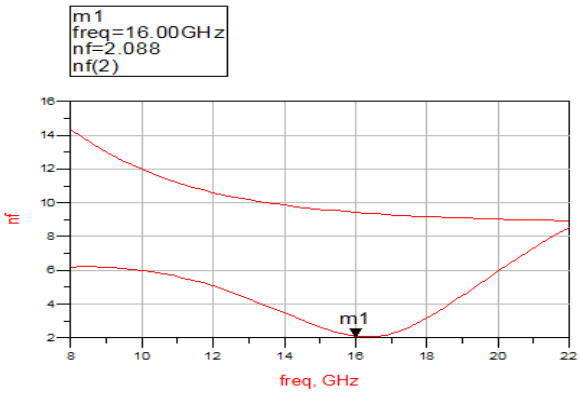

Fig10. Noise Figure Vs Frequency

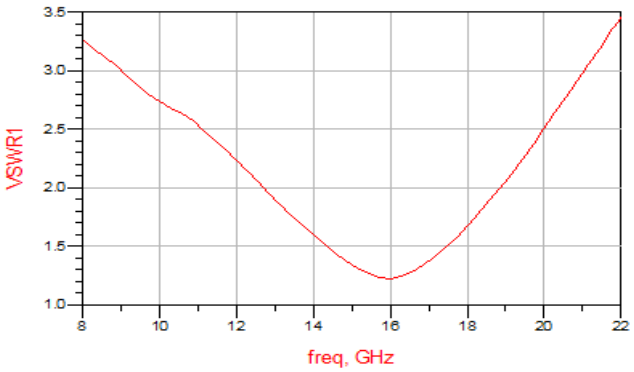

Fig.11 VSWR Vs Frequency

V. CONCLUSION

The CMOS LNA is designed for MMW applications in this LNA, based on TSMC technology. The single-ended two stages of LNA are designed using 90nm CMOS process at 31GHz in this circuit. Performance standards are met for this new design technique. Simulation results of the designed circuit are shown that gain of 27dB, S_{11} of –33dB and LNAE of 73% with the DC Low noise amplifier of 25mW under 1V Low noise supply. The proposed method of LNA using micro-strip line in MMW applications increases the overall efficiency.

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