9th International Conference on Science, Technology and Management
Indian Federation of United Nations Associations, New Delhi (India) ICSTM-17
14th October 2017, www.conferenceworld.in ISBN: 978-93-86171-71-9

256 BIT LINEAR CARRY SELECT ADDER

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ABSTRACT

Design of power-efficient and high-speed data path logic systems are one of the most substantial areas of research in VLSI system designIn many data-processing processors Carry Select Adder (CSLA) is one a fastest adders used to perform arithmetic functions. The upcoming technologies depicts that there is a scope for reducing the area and power consumption in the CSLA. To significantly reduce the area and power of the CSLA this work uses a simple gate level modification . Based on this modification CSLA architecture have been developed and can be compared with the regular CSLA architecture. However,the regular CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux). 1 instead of RCA in the regular CSLA to achieve high speed and low power consumption.The results analysis shows that the proposed CSLA structure is better than the regular CSLA.

Keywords- Delay; Area; Array Multiplier, Low power, VHDL Modelling & Simulation.

I. INTRODUCTION

Area and power reduction on data path logic systems are the main area of research in VLSI system design. High-speed addition, multiplication has always been a fundamental requirement of high-performance processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adders. The sum for each bit position in an elementary adder is generate sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speeded limitation in any adder is the production of carries, many authors have considered the addition problem.

The CSLA is used in many computational systems. To moderate the problems of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.However, the CSLA is not area efficient because it uses multiple pair of Ripple Carry Adders (RCA) to be generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexer (mux). To overcome above problem, the basic idea of the proposed work is by using n-bit binary to improve the speed of addition. This logic can be implement with type of adder to further improve the speed. Using Binary to instead of RCA in the regular

CSLA to achieve lower area and power consumption. The main advantages of this RCA logic comes from the less number of logic gates than the Full Adder (FA) structure.

In electronics,[1] a carry-select adder is a particular way toimplement an adder, which is a logic elementthat computes the -bit sum of two -bit numbers. The carry-select adder is simple but ratherfaster, having a gate level depth of$O(\sqrt{n})$. The carry-select adder generally consists of two Ripple Carry Addersand a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders [therefore two ripple carry adders] in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming ones. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is knowns. The numbers of bits in each carry select blocks can be uniform or variable. In the uniform case, the optimal delay occurs for a blocks size of$\lfloor\sqrt{n}\rfloor$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it so that the carry out is calculate just in time. The$O(\sqrt{n})$delay is derived from uniform size, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that yield an equal number of MUX delays.

1. Basic building block

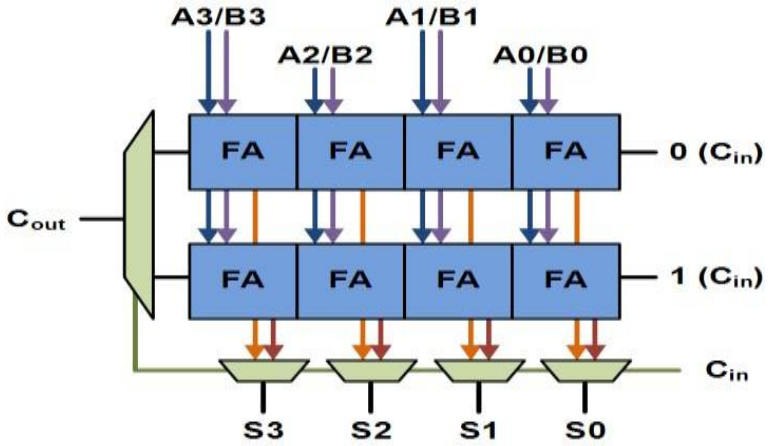

Fig.1.Basic carry Select adder.

Above is the basic buildings block of a carry-select adder, where the block size is 4.

2.Fundamental Adder Block

Ripple Carry Adder (RCA) shows the compact designs but their computation time is longer. Carry Look-Ahead Adder (CLA) is used in time critical applications to derive fast results but it leads to increase in areas. But

the carry select adder provides a compromise or bridgeway between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous or preceding adder becomes the input carry of next or succeeding full adder. Therefore, the carry of this adder traverse longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of Ripple carry adder. Now as the value of N increases, delay of adder also increase in a linear way. RCA inspite of having an advantage of covering least area, it has the lowest speed amongst all the adders because of large propagation delay, now CSLA provide advance way to get around this linear dependency that is anticipate all possible values of input carry , 0 and 1 and evaluates the result in advance.Result can select using the multiplexer stage once original value of carry is known. Therefore the convention CSLA make use of dual RCA's to generate the partial sum and carry by assume input carry Cin=0 and Cin=1, then the multiplexers selecting the final sum and carry.

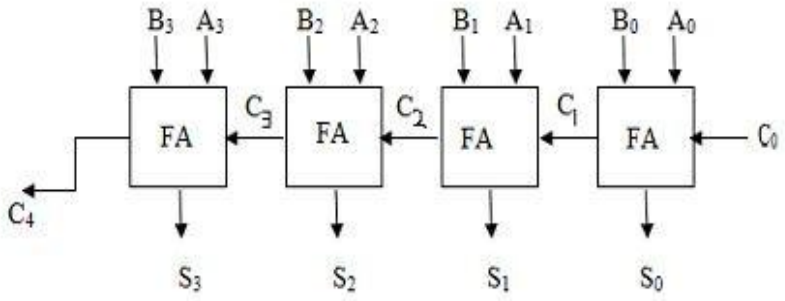

Fig.2: 4-bit Ripple Carry Adder.

3.Uniform-sized adder

A 16-bit carry-select adder with a uniform block size of 4 can created with three of these blocked and a 4-bit ripple carry adder [3]. Since carryin is also known at the beginning of computation, a carry select block is need not for the first four bits. The delay of this adder will be four full adder delay, plus three MUX delay.

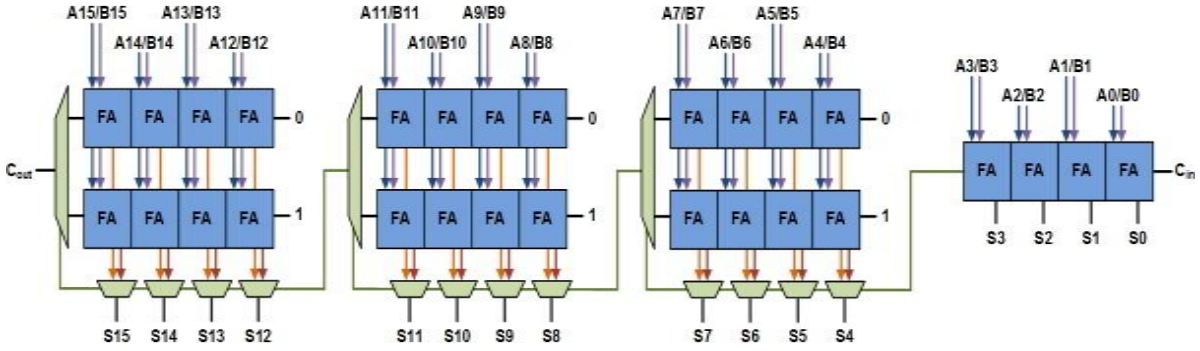

Fig.3: Regular Fixed Size CSLA

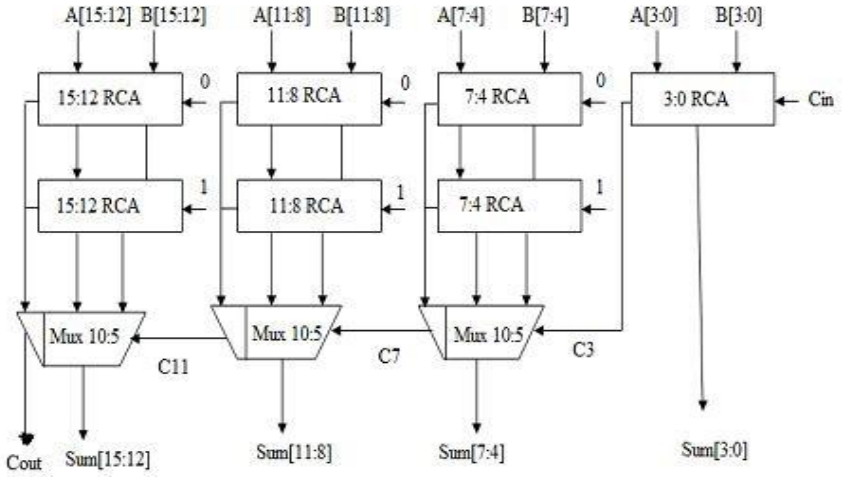

Fig. 4: 16-bit conventional carry select adder

4. Architecture of 128-bit CSLA

A 16-bit carry select adder can be developed into two different sizes namely uniform block in size and variable block in size. The number of bits required for RCAlogic is equal to 1 bit Similarly a 32, 64 [5]and 128-bit can also be developed by two modes of different block sizes. Ripple-carry adders are simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least significant bit to most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders.

The importance of the RCA logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 8-bit RCA is listed improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay.The structure of 128-b regular CSLA is shown in Fig. 6. It has five groups in different size RCA. The delay and area evaluation of each group are shown in Fig. 3, in which the numerals with in specify the delay values.

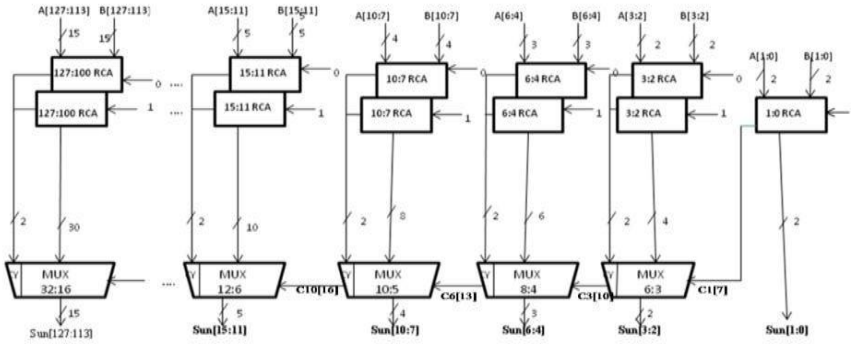

Fig .4 Architecture of Regular 128-b CSLA

V. SIMULATION REULTS

The simulation result for the above specified 256 bit linear carry select adder REFERENCES[8]depicted below using Xilinx software.

TABLE.1

PARAMETERS	EXISTING CSLA	PROPOSED CSLA
POWER(µw)	969.9	867.9
AREA(µm2)	3985	3256
DELAY(ns)	5.482	4.856

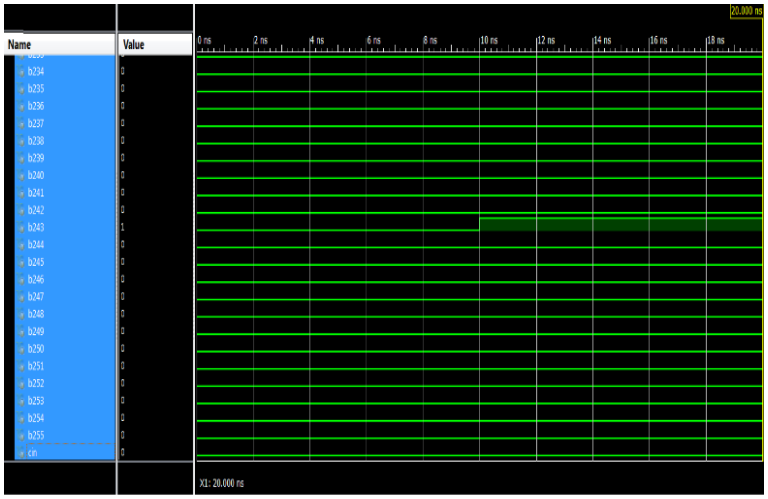

Fig .5 Output of 256-b linear carry select adder (using Xilinx software).

VI. CONCLUSION

This work presents a Efficient Architecture of 256 bit linear Carry Select Adder simple approach to reduce the area, delay Design by Common Booleanand power of CSLA architecture.The conventional carry select adder has the disadvantage on more power consumption and occupying more chip area. The proposed CSLA using common Boolean logic has low power [6], less delay and reduced.

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