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DESIGN AND VERIFICATION OF UART USING VERILOG HDL

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ABSTRACT

UART architecture involves and attempt to the serial communications. UART is appetent for make an interface between RS232 line and a microcontroller or an IP core. For this, UART is implemented on VCS tool of Synopsys platform of UNIX and the source code is written in Verilog and verification byVerilog.

Keywords: Serial Communication, Interface, Verilog

I.INTRODUCTION

This paper consists of the Designing and the Verification of UART [1]. UARTs are now very often added in microcontrollers. A UART is typically an exclusive (or part of an) integrated circuit (IC) used for serial communication on to a computer or peripheral device serial port. It operates magnificentlywhen linked to a serial port of a PC for data exchange with custom electronic. UARTs are now often added in microcontrollers. A UART is a full duplex transmitter or receiver. UART is the sort of serial communication protocol.In this paper Verilog is used to endorse a design and to evolve a Test bench that can reprocess and it is outline in step by step as defined by verification principles andmethodology.

II. ARCHITECTURE OF UART

2.1BAUD RATE GENERATOR

Baud Rate Generator is actually a frequency divider. The baud rate frequency factor can be calculated according to a given system clock frequency (oscillator clock) and the requested baud rate. The calculated baud rate frequency factor is used as the dividing factor. In this design, the frequency clock generated by the baud rate generator is not the baud rate clock, but 16 times the baud rate clock. The motive is to exactly represent the asynchronous serial data at the receiver. Assume that the system clock is 50MHz, baud rate is 115200 bps, and then the output clock frequency of baud rate generator should be 16 * 115200Hz.Therefore the frequency coefficient (M) of the baud rate generator is: M =50MHz/16*115200Hz. When the UART accepts serial data, it is very analytic to determine where to sample the data information. The ideal time for comparing is at the middle point of each serial data bit. In this block, the accepted clock frequency is designed to be 16 times the baud rate, hence, each data width accepted by UART is 16 times the receive clock cycle.

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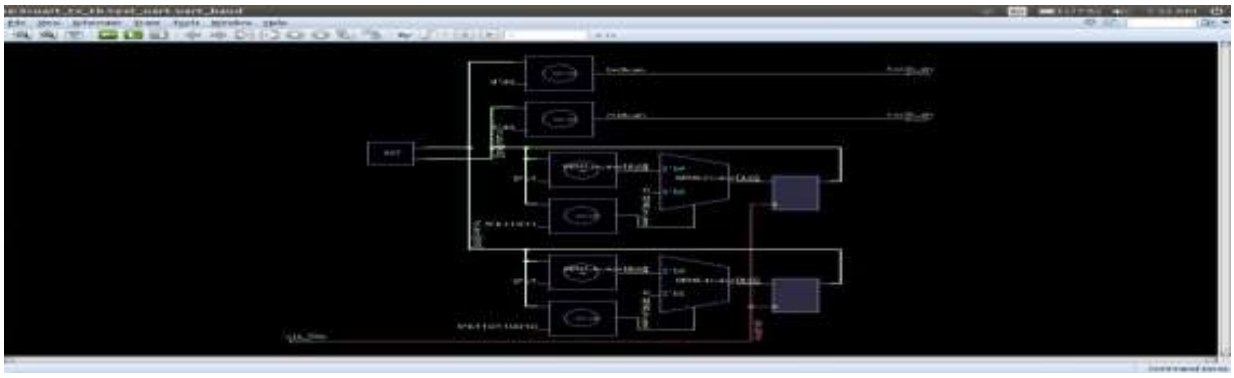

***Fig.1:-*Block Diagram of Baud Rate Generator**

2.2TRANSMITTER

Asynchronous sending out enables the data to be send without the sender have to send a clock signal to the receiver. In this case, the transmitter and receiver must concur on timing parameters (Baud Rate) prior transmission and special bits are put in to each word to synchronize the sending and receiving units. In asynchronous sending out, the sender sends a Start bit, 5 to 8 data bits (LSB first), an optional Parity bit, and then 1, 1.5 or 2 Stop bits.

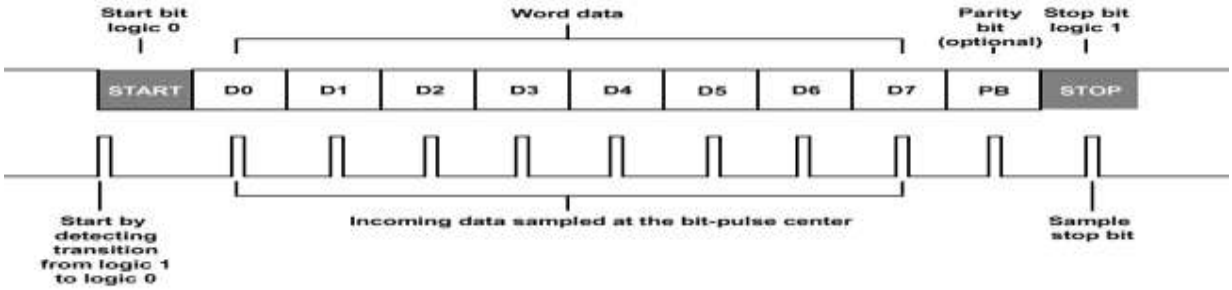

Fig.2:- Data Framing

When a word is moved to the UART for asynchronous transmissions, the Start bit is put in at beginning of the word. So, at first Start bit is used to convey the receiver that a word of data is about to be send, thereby pressurizing the clock in the receiver to be in sync with the clock in the transmitter. It is significantto reckthat the frequency drift linking these two clocks must not exceed 10%. Later then the Start bit, the individual bits of the word of data are sent, beginning with the Least Significant Bit (LSB). And then when the data is fully send out, an optional Parity bit is sent to the transmitter. This bit is usually used by receiver to perform simple error checking. At the end, Stop bit will be sent to indicate the end of transmission.

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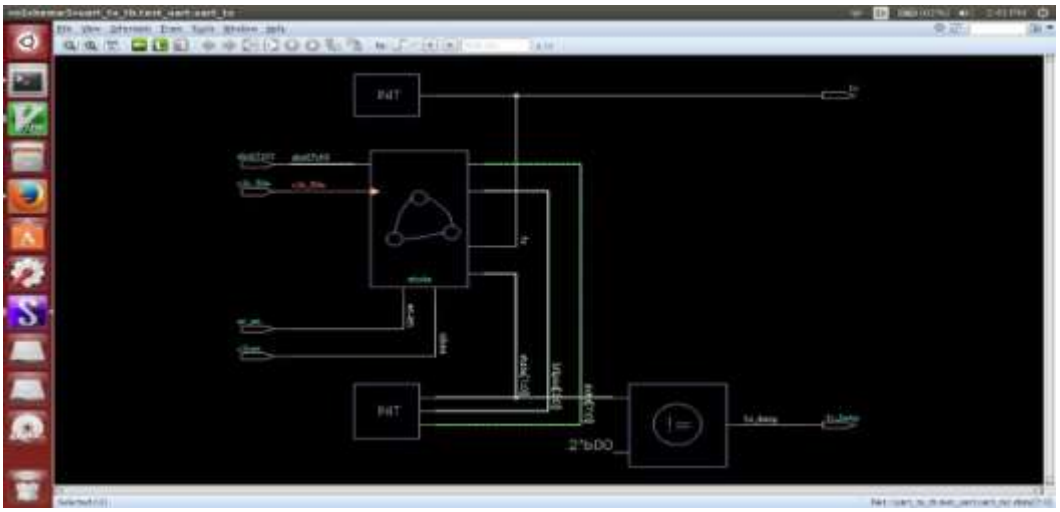

***Fig.3:-*Block Diagram of Transmitter**

2.3RECEIVER

After the transmitting of bits when the receiver has received all of the bits in the data word, it may check for the Parity Bits (both sender and receiver need to symbolize on whether a Parity Bit is to be used), and then thereceiver quest for a Stop Bit. Supposing the Stop Bit does not seem when it is professed to, the UART presume the entire word to be garbled and will report a Framing Error to the host processor when the data word is read. General reason for the take place of Framing Error is in order to the sender and receiver clocks were not running at the same speed, or that the signal was interrupted. Eachand every operation of the UART hardware is controlled through a clock signal which drives at much faster rate than the baud rate.

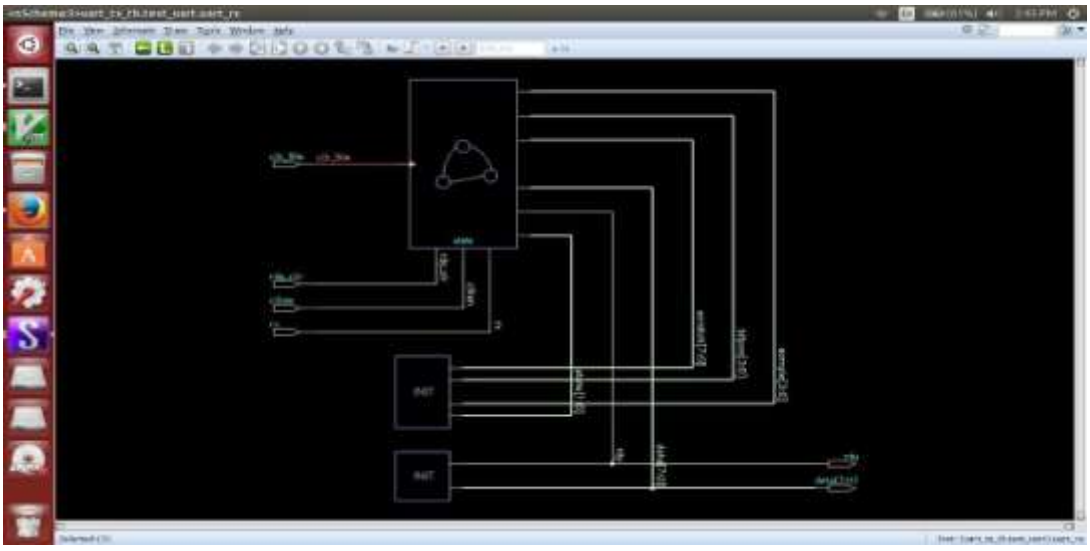

Fig.4:-Block diagram of Receiver

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III.VCS RESULT

3.1SCHEMATIC DESIGN OF UART

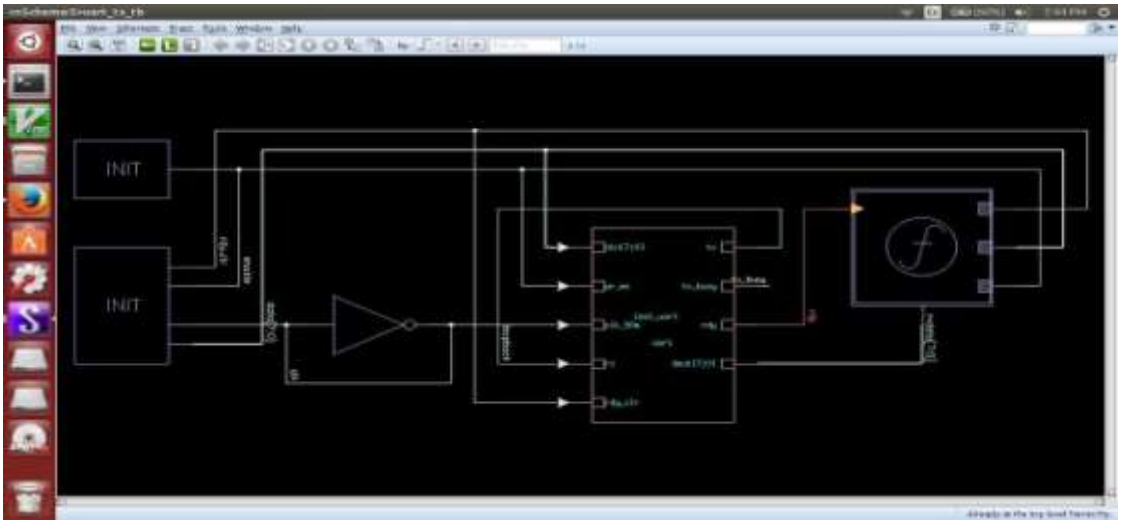

***Fig.5:-*Schematic Design of UART**

3.2SIMULATED WAVEFORM OF UART

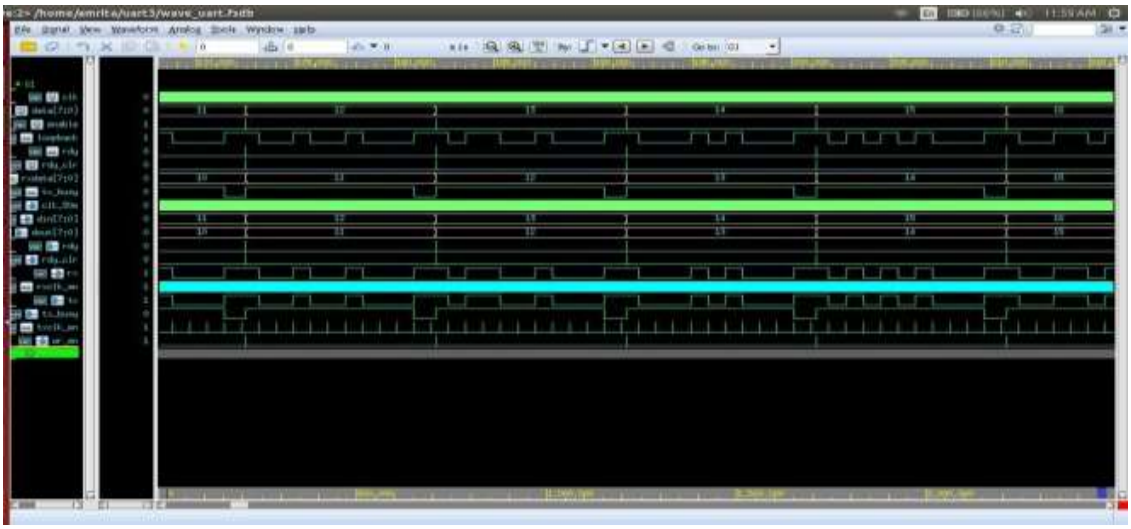

***Fig.6:-* Simulated waveforms of UART**

IV. CONCLUSION

The design of UART has been done successfully by using Verilog code and its communication protocol. The conversion of parallel data into serial data and serial data into parallel data for the communication is done. It shows that the transmitter transmits the data and receiver receives the data with the same baud rate. By this there is no loss of time as it transmit and receive at the same baud rate.

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