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IMPLEMENTATION OF AN AREA AND DELAY EFFICIENT FIXED FIR FILTER USING MULTIPLE CONSTANT MULTIPLICATIONS (MCM) TECHNIQUE

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ABSTRACT

Multiple Constant Multiplications (MCM) are widely used for implementing transpose form pipelined Finite Impulse Response (FIR) filters. In biomedical applications like Electro Cardio Gram (ECG) the coefficients of FIR filters remain fixed. In these applications, Full flexibility of a multiplier is not necessary. Once the MCM method is implemented, it can be called as many times if needed. Transpose form block FIR filter depends on MCM based architecture for fixed FIR filter. Adders play an important role in Digital Signal Processing. In this paper, two different types of adders are used in Pipelined Adder Unit (PAU) for better area and delay realization. Performance comparisons results show that FFIR filter using Ripple Carry Adders (RCA) has a less Area Delay Product (ADP) when compared with FFIR filter using Carry Select Adder (CSLA). Implementation of Fixed FIR filter using MCM is done using VerilogHDL and synthesized using Xilinx 12.2 synthesis tool and ISIM simulator.

Keywords: Electro Cardio Gram (ECG), Finite Impulse Response (FIR) filters, Multiple Constant Multiplications (MCM), VLSI.

I. INTRODUCTION

Digital Signal Processing (DSP) has a great significance in multimedia, communication and industrial applications [1]. Filtering is one of the extensively used operations in DSP. Digital filters are used for the filtering operation. FIR and IIR are two types of digital filters. Finite impulse response (FIR) digital filter plays an important role in many image and signal processing applications. In biomedical applications like Electro Cardio Gram (ECG) the coefficients of FIR filters remain fixed [2] and [3]. The Multiplier is the major component in FIR filter which determines the performance of the desired filter. In order to minimize the complexity of the architecture, multiplier unit in FIR filter can replace by Multiple Constant Multiplication (MCM) technique. So there is need to implement a Fixed FIR filter structure using MCM based architecture to

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support the above mentioned applications. Several researchers have proposed different types of VLSI architectures for the implementation of Fixed FIR filters using distributed arithmetic (DA) [4] and Multiple Constant Multiplications (MCM) based methods [5]. FIR filters use Lookup Tables (LUTs) for storing the filter coefficients and to minimize the system complexity [6] - [8]. Multiple Constant Multiplications (MCM) based architecture is proposed for fixed coefficient implementation in this method, multiplication operation is performed with the help of shift and add unit. Computation sharing programmable FIR filter has been proposed by J. Park [9]. It is used for high speed and low power applications and it minimizes redundant computation in FIR filters by using the Computation Sharing Multiplier (CSHM). R.Mahesh and A.P.Vinod proposed a Common Sub expression Elimination (CSE) technique for implementing FIR filters using binary representation of coefficients [10]. This method reduces the number of adders required in architecture. In this paper, implementation of transpose form pipelined block Finite Impulse Response (FIR) filters that supports Multiple Constant Multiplications (MCM) is presented. The rest of the paper is organized as follows: In section II, VLSI architectures for fixed applications is presented. Simulation results are presented in section III. In section IV, performance comparisons are discussed. Finally, the conclusion is described in section V

II. FIXED FIR FILTER ARCHITECTURE

2.1 Multiple Constant Multiplications (MCM) method

Multiplication operation with a constant term is defined as constant multiplication. Constant multiplications can be categorized into Single Constant Multiplication (SCM) and Multiple Constant Multiplication (MCM). In Single Constant Multiplication, input value is multiplied by single constant. The main objective of multiple constant multiplications is to remove the multiplier block. MCM based method is more efficient when a given input variable is multiplied by more number of fixed constants using shift and add method is shown in Fig.1.

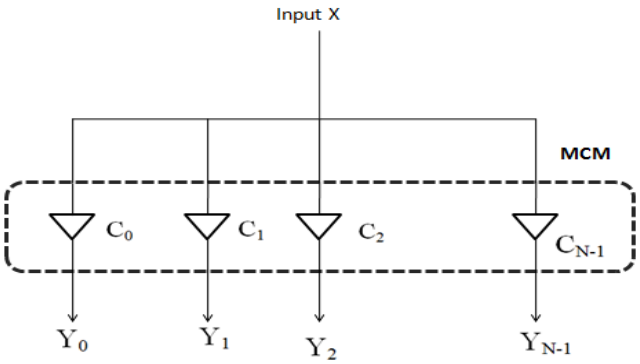

Fig.1. Block Diagram of MCM

It can be implemented by using adders/sutractors and shifters. Initially, the constants are expressed in binary form. Then for every non-zero digits in the binary format of the constant, based on its digit position the input variable is shifted and adds up the shifted variable to obtain a result. MCM is employed in many applications like error correcting codes, frequency multiplication and Multiple Input and Multiple Output systems (MIMO). Full flexibility of a multiplier is not necessary for the constant multiplication. Once the MCM method is

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implemented, it can be used as many times if needed. Filter coefficients are constants for a given filter, so that multiplication operation is performed by using a network of adders, sub tractors, and shifters where the number of adders and subtractors are reduced by using Multiple Constant Multiplication technique.

2.2 Fixed FIR Filter Implementation Using MCM

The architecture of block FIR filter for fixed application is shown in the Fig.2. For Fixed FIR filter implementation, the CSU is not necessary here filter coefficients are fixed. Similarly, Inner Product Units (IPUs) are not used because multiplication operation is performed with Multiple Constant Multiplication (MCM) units to reduce the huge complexity of the architecture

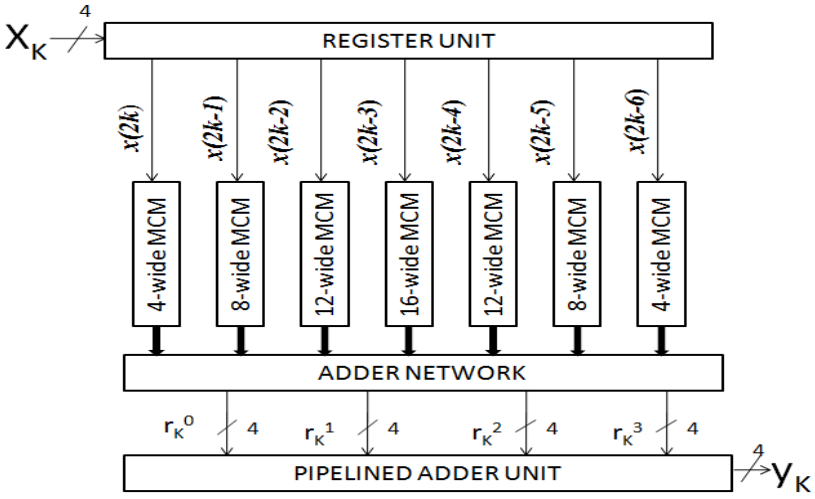

Fig.2. Fixed FIR filter using MCM.

MCM based technique for a Fixed FIR filter with block size L=4, make utilize of symmetry in input matrix S_K^0 to execute vertical and horizontal common subexpression elimination and to reduce the number of shift and add functions in the MCM units. MCM can be employed in both vertical and horizontal order of the coefficient matrix. The MCM based method consists of six input samples similar to six MCM blocks. The input matrix contains four rows of S_k^0 and coefficient group. In all four rows or four columns, the input sample $x(4k-3)$ is present, where the input sample $x(4k)$ present in only one row or one column. So that, the input sample $x(4k-3)$ is multiplied with all rows of the coefficient matrix and the input sample $x(4k)$ is multiplied with the first row of coefficient matrix is shown in Table.1.

$$R= \begin{bmatrix} x(4k) & x(4k-1) & x(4k-2) & x(4k-3) \\ x(4k-1) & x(4k-2) & x(4k-3) & x(4k-4) \\ x(4k-2) & x(4k-3) & x(4k-4) & x(4k-5) \\ x(4k-3) & x(4k-4) & x(4k-5) & x(4k-6) \end{bmatrix}$$

$$\begin{bmatrix} h(0) & h(4) & h(8) & h(12) \\ h(1) & h(5) & h(9) & h(13) \\ h(2) & h(6) & h(10) & h(14) \\ h(3) & h(7) & h(11) & h(15) \end{bmatrix}$$

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Table.1. MCM IN TRANSPOSE FORM BLOCK FIR FILTER

INPUT SAMPLE	COEFFICIENT GROUP
$x(4k)$	{ h(0),h(4),h(8),h(12) }
$x(4k-1)$	{ h(0),h(4),h(8),h(12) } { h(1),h(5),h(9),h(13) }
$x(4k-2)$	{ h(0),h(4),h(8),h(12) } { h(1),h(5),h(9),h(13) } { h(2),h(6),h(10),h(14)}
$x(4k-3)$	{ h(0),h(4),h(8),h(12) } { h(1),h(5),h(9),h(13) } { h(2),h(6),h(10),h(14) } { h(3),h(7),h(11),h(15) }
$x(4k-4)$	{ h(1),h(5),h(9),h(13) } { h(2),h(6),h(10),h(14) } { h(3),h(7),h(11),h(15) }
$x(4k-5)$	{ h(2),h(6),h(10),h(14) } { h(3),h(7),h(11),h(15) }
$x(4k-6)$	{ h(3),h(7),h(11),h(15) }

All MCM blocks compute the required product terms using shift and add method. The outputs of all MCM blocks are given to the adder network to produce the inner product terms. In the Pipelined Adder Unit (PAU) array of RCA and CSLA are used to add inner product values and produce a block of the filter output.

III. SIMULATION RESULTS

The proposed VLSI architectures for fixed applications are written in a Verilog HDL, synthesized and simulated using Xilinx ISE 12.2 design tool and an ISIM simulator. The design properties used for simulation results are Spartan 3E family, XC3S500E device, FG320 package with a speed grade of -5

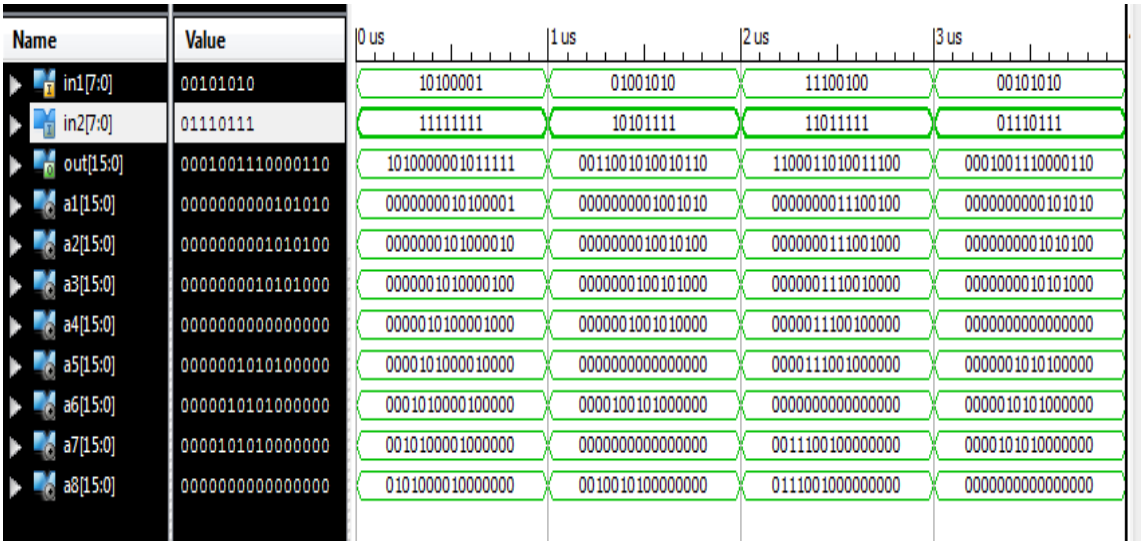

Fig.3. Simulation Result of Multiple Constant Multiplications

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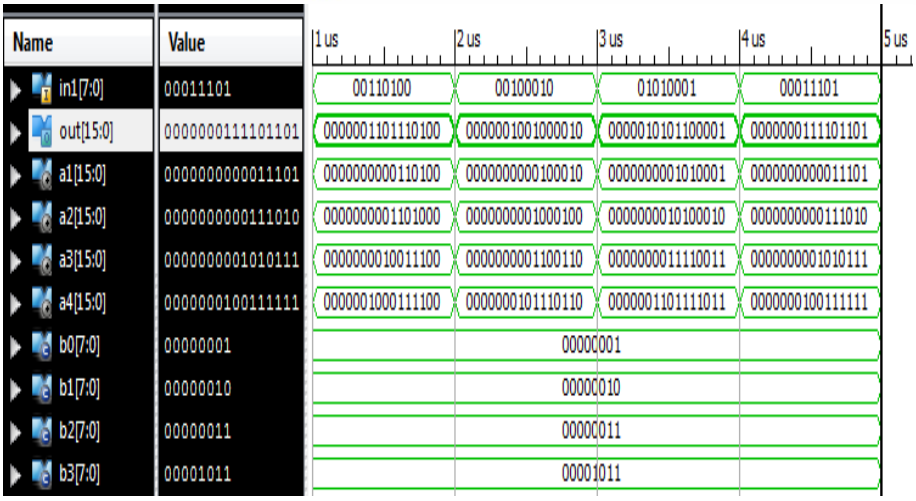

Fig.4. Simulation Result of 4-wide MCM

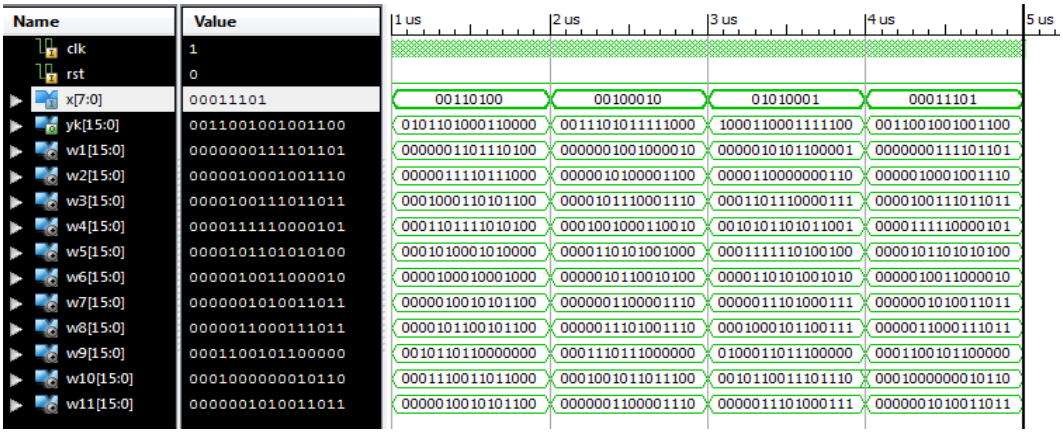

Fig.5. Simulation Result of Fixed FIR filter

The simulation result of Fixed FIR filter is shown in the Fig.5. The input sample X is 8-bit binary value and having the filter length N=16. Input values are applied to RU it produces six input samples of 8-bit binary value. These input samples are multiplied by several constant coefficients using the MCM method. The outputs of all the MCM blocks are given to adder network it produce inner product values. The array of KSA is used in PAU for summation of all the inner product values. Finally, from KSA filter output is obtained. To illustrate the functionality of the proposed architecture a 8-bit input sample Xk=00011101 and fixed coefficient are considered. MCM operation is performed between the input sample and 4- wide MCM (h0, h1, h2, h3) having a width of 8-bit binary value then w1 is obtained. This process repeats for 8,12 and 16 wide MCM and the output obtained are w2, w3, w4, w5, w6, and w7. In adder network, these partial inner products are added which gives w8, w9, w10 and w11. After that by using KSA the summation of w8, w9, w10 and w11 are performed. Finally, the filter output yk is obtained.

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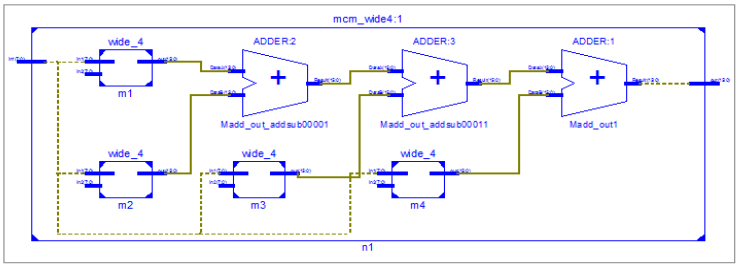

Fig.6. Detailed view of RTL Schematic of 4-Wide MCM

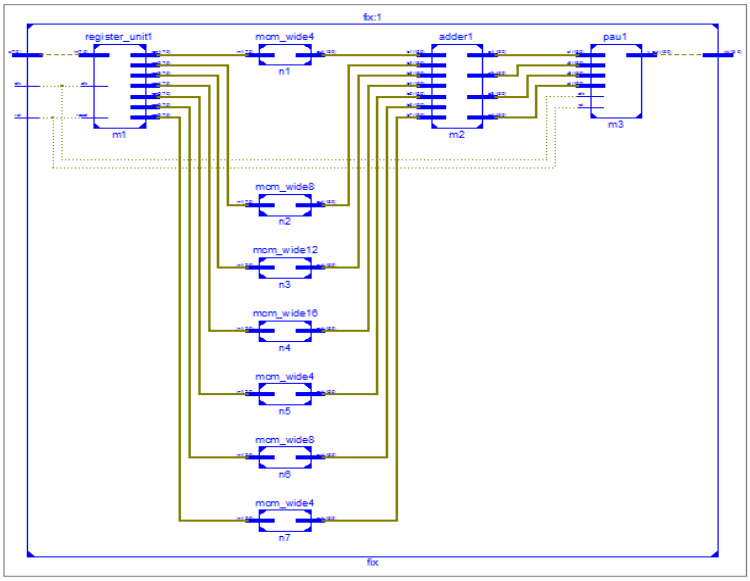

Fig.7. Detailed view of RTL Schematic of Fixed FIR filter

IV. COMPARISONS

The above section deals with the simulation results. In these section comparisons of Fixed VLSI architectures using different types of adders like Ripple Carry Adder and Carry Select Adder are examined. The design properties used for synthesis results are Spartan 3E family, XC3S500E device, FG320 package with a speed grade of -5.

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	92	9,312	1%	
Number of 4 input LUTs	970	9,312	10%	
Number of occupied Slices	649	4,656	13%	
Number of Slices containing only related logic	649	649	100%	
Number of Slices containing unrelated logic	0	649	0%	
Total Number of 4 input LUTs	1,116	9,312	11%	
Number used as logic	970			
Number used as a route-thru	146			
Number of bonded IOBs	26	232	11%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.30			

Fig.8. Area report of FFIR filter implemented with Ripple Carry Adder

ISBN: 978-93-86171-60-3

Device utilization summary of the Fixed FIR filter implemented with Ripple Carry Adder is shown in Fig.8. From the figure, it is observed that, out of 4,656 available slices 649 slices are occupied by the logic and the system utilizes 970 four input LUT's out of 9,312 available 4 input LUT's.

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	86	9,312	1%	
Number of 4 input LUTs	1,251	9,312	13%	
Number of occupied Slices	768	4,656	16%	
Number of Slices containing only related logic	768	768	100%	
Number of Slices containing unrelated logic	0	768	0%	
Total Number of 4 input LUTs	1,397	9,312	15%	
Number used as logic	1,251			
Number used as a route-thru	146			
Number of bonded IOBs	26	232	11%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.55			

Fig.9. Area report of FFIR filter implemented with Carry Select Adder

Device utilization summary of the Fixed FIR filter implemented with Carry Select Adder is shown in Fig.9. From the figure, it is observed that, out of 4,656 available slices 768 slices are occupied by the logic and the system utilizes 1,251 four input LUT's out of 9,312 available 4 input LUT's.

Delay report of Fixed FIR filter implemented with RCA and CSLA

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 41.320ns (Maximum Frequency: 24.201MHz)
   Minimum input arrival time before clock: 1.731ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found
```

```
Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 40.693ns (Maximum Frequency: 24.574MHz)
   Minimum input arrival time before clock: 1.731ns
   Maximum output required time after clock: 4.040ns
   Maximum combinational path delay: No path found
```

Device Utilization Graph of Fixed FIR filter

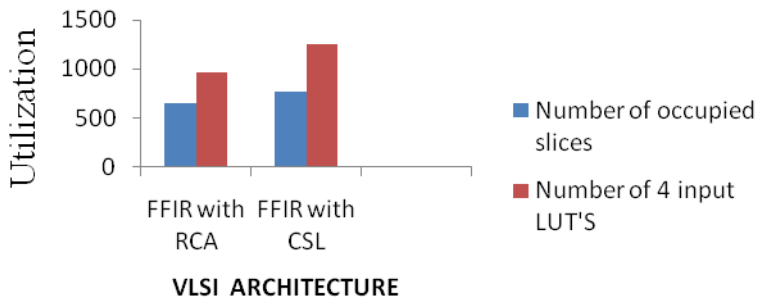

Fig.10. Comparison of area of VLSI architectures for Fixed FIR filters using different adders

From the above statistics, the device utilization graph is drawn for Fixed FIR architectures using Ripple Carry Adder and Carry Select Adder is shown in Fig.10. RCA occupies less area when compared with CSLA.

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Delay Report of Fixed FIR filter

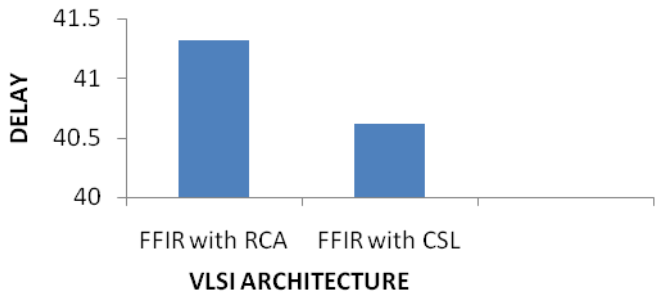

Fig.11. Comparison of delay of VLSI architectures for Fixed FIR filters using different adders

The delay report is drawn for Fixed FIR architectures using Ripple Carry Adder and Carry Select Adder is shown in Fig.11. CSLA has less delay when compared with RCA.

Area Delay Product Report of Fixed FIR filter

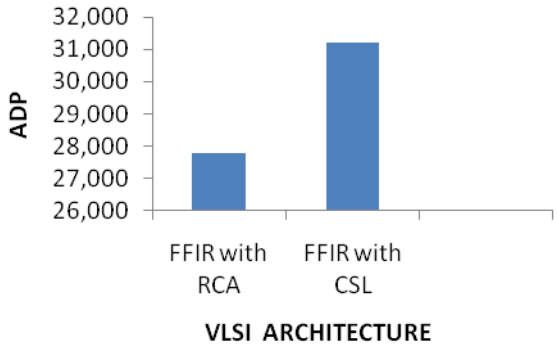

Fig.12. Comparison of Area Delay Product of VLSI architectures for Fixed FIR filters using different adders

From the above area and delay reports, Area Delay Product (ADP) graph is drawn for Fixed FIR architectures using Ripple Carry Adder (RCA) and Carry Select Adder (CSLA) is shown in Fig.12. RCA has less Area Delay Product (ADP) when compared with CSLA.

V. CONCLUSION

In this paper, an area and delay efficient transpose form block FIR filter is implemented for Fixed applications using Multiple Constant Multiplication (MCM) technique. In Pipelined Adder Unit, array of Ripple Carry Adder (RCA) and Carry Select Adder (CSLA) are used. Performance comparisons results show that FFIR filter using Ripple Carry Adders (RCA) has a less Area Delay Product (ADP) when compared with FFIR filter using Carry Select Adder (CSLA). In the future, the area and delay can further be reduced in transpose form Fixed FIR filter by using Kogge Stone Adder (KSA) in Pipelined Adder Unit.

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