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OPTIMUM BODY BIASING TECHNIQUE IN D-LATCH

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ABSTRACT

VLSI outlining of the proficient circuits is pointing towards the gadgets expending less power and creates less postponement with capacity to work in more extensive scope of frequencies. This paper shows a changed plan of d flip flop for low power VLSI applications. The proposed changed outline devours less power utilization, delay, and power delay product item. The plan is tried by applying body biasing method. The outline is re-enacted utilizing TANNER-EDA instrument 13.0 on 65nm technology. Re-enactment comes about demonstrate that power utilization, postponement and power defer item proficient D-latch with empower configuration is better decision for compact applications.

Keywords: CMOS, Conventional body bias, Dynamic power, Substrate Biasing.

I. INTRODUCTION

The most recent advances in versatile battery-fuelled gadgets, for example, the individual Digital Assistants (PDA) and cell phones have set new objectives in computerized VLSI plan. The cells phones require fast and low power utilization and therefore control postpone item assume vital part in the outlining of VLSI circuits. Flip-flops or the information stockpiling components are very nearly a fundamental part of each successive hardware. Among different flip-flops, D flips failures; D flip flop is usually utilized. It catches the estimation of the D contribution at a specific predefined part of the clock beat (rising or falling edge of the clock). Those catch esteem turns into the Q yield. Also, its yield is not influenced at different parts of the clock.

From the planning point of view, deferral delivered by flip-flops expends an extensive part of the process duration while the working recurrence increments. In the course of the last 4 decade CMOS innovation have run under uncommon scaling with the perspective of reconciliation thickness, fast and low power scattering. Control utilization is imperative thought in IC plan. Two sorts of FF are discovered single edge activated (SET) and twofold edge activated (DET). Single edge activated is basic in plan because of testing information either on rising or on falling edge of clock; then again twofold edge activated examined information on both clock edges. DFT is vitality proficient contrasted with SET.

The flip-flop is essential Building Square of the advanced hardware frameworks utilized as a part of PCs and numerous different sorts of frameworks. Level trigger flip flop is known as lock and this flip flop is for the most part utilized as capacity component. There are such a large number of FF designs, for example, JK FF, T FF, D FF, in all above D FF is most straightforward and normal. The D flip flop is generally utilized. It is otherwise called an "information" or "deferral" flip-flounder. Latches and flip-flops are the fundamental components for putting away data. One lock or flip flop can store one piece of data. The fundamental distinction amongst latches and flip-flops is that for locks, their yields are not continually influenced by their contributions the length of the empower flag is

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stated. As such when they are empowered, their substance changes promptly when their data sources change. Flip-flops, then again, have their substance change just either at the rising or falling edge of the empower flag. This empower flag is generally the controlling clock flag. After the rising or falling edge of the clock, the flip-flop content stays steady regardless of the possibility that the info changes. A latch is regularly called level-touchy in light of the fact that their yield takes after their contributions the length of they are empowered. They are straightforward amid this whole time when the empower flag is attested. These are circumstances when it is more valuable to have the yield change just at the rising or falling edge of the empower flag. This empower flag is normally the controlling clock flag. In this way, we can all progressions synchronized to the rising or falling edge of the clock. An edge-activated flip-flop accomplishes this by joining in arrangement a couple of locks.

Correlation of body predisposition strategies utilizing delay, power and PDP demonstrates that independently biasing the pre-charge and assessment transistor bodies allows rapid and vitality productive ultra-low voltage circuits to be figured it out. Least vitality in the sub limit district then depends on supply voltage as well as on the substrate predisposition voltage. In this paper CMOS NOR with gates for D-latch with empower with substrate biasing procedures contrasted and the current one. Power consumption and delay are utilized as parameters at various frequencies, supply voltage and temperatures in sub threshold region. The paper is sorted out as takes after: In Section II different circuit descriptions. Recreation and execution results are introduced in Section III. At long last, conclusions are displayed in Section IV

II CIRCUIT DESCRIPTIONS

The D-latch has numerous applications in advanced circuit outline, principally for brief stockpiling of information or as a delay component. The existing is consist of 14-CMOS in which 7 were PMOS and remaining 7 were NMOS. For the right operation of the flip-flop, the information esteem must be kept up consistent just before setup time (t setup) and just after hold time (t hold) of the triggering of the Enable (clock). D-latch is implemented, at the gate level, by simply utilizing a NOR-based S-R latch, connecting to inputs, and connecting D' to input R with an inverter. When enable (clock) goes high, D is transmitted to output Q (and D' to Q1).when its goes to low, the latch retains its previous state. If enable (clock) =1 then Q1=D, set data mode. If positive feedback is applied clock =0 then Q1=Q1, hold data mode. The D-latch circuit is interpreted as an AOI gate with two inputs to the AND, and 1 input to the OR.

A latch is a device that can receive and hold an input bit. A simple D-latch forms the basis for many designs. The CMOS circuit can be constructed using either the logic diagram or the structural description. At physical level, this can be created by instancing two NOR2 cells and one NOT cell, and then adding the interconnect wiring. Alternately, a custom layout would probably consume less area. An enable control En can be added to the basic D-latch by routing the inputs through AND gates. An enable bit of En=0 blocks the inputs by forcing 0's to AND outputs, which places the SR latch into a hold state. The D-latch circuit is interpreted as an AOI gate with two inputs to the AND, and 1 input to the OR. Although the notation is not standard. It is widely used in practice. The existing circuit is in fig.1.

The schematic of proposed circuit with body biasing plan is appeared in fig.2. Body-Bias is a method intended to diminishing sub limit leakage current, which includes the fundamental segment of static power utilization. Substrate biasing gives a powerful circuit-level method for sub-threshold voltage. The two systems can be consolidated in the

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design that objectives both dynamic and static power utilization. By using the body biasing technique we are able to reduce the overall power, delay and power delay product consumption so the design becomes better applicable for the low power applications.

This type of substrate connection reduces the complexity of the design. Our proposed method will reduce the power consumption though the gate simulations of all the circuits are performed using Tanner EDA Tools 13.0 on 65nm technology. The advantage of this design is threshold voltage will increase which reduces the leakage current of the circuit. This sort of substrate increase association lessens the complexity of the design.

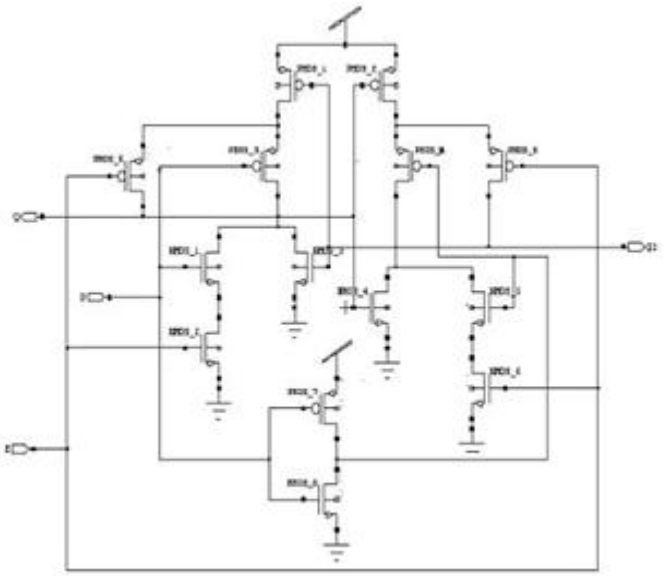

Fig.1. Existing Circuit

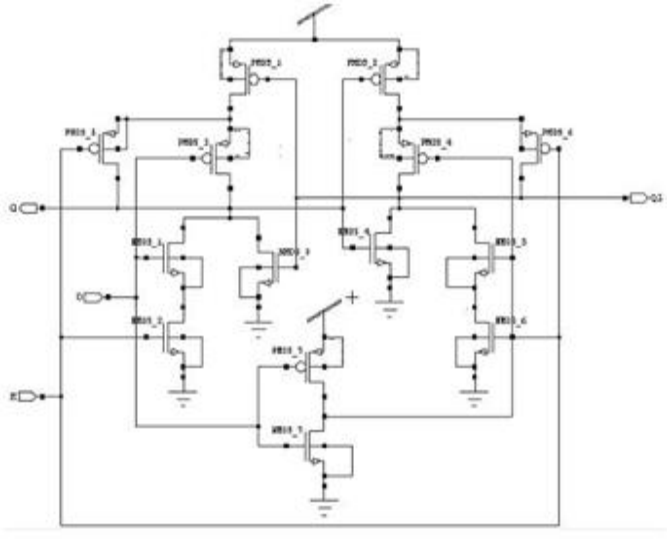

Fig.2. Proposed Design

Here substrate of NMOS is associated with their source and PMOS is associated with their vdd, which builds the sub threshold voltage that decrease Our proposed technique will lessen the power utilization however the door reproductions of the considerable number of circuits are performed utilizing Tanner EDA Tools13.0 on 65nm technology. The benefit of this design is limit voltage will expand which decreases the leakage current of the circuit.

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The output waveform of the circuit is shown in fig.3

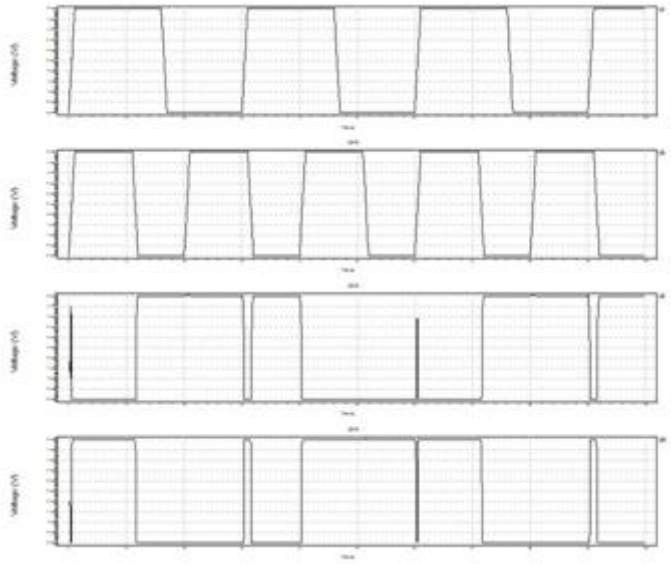

Fig.3. Output Waveform

III SIMULATION AND IMPLEMENTATION RESULT

The standard temperature estimation of 250C, input signal frequency of 5MHz, and supply voltage of 0.3V in 65nm is utilized. Power consumption and delay are measured keeping one parameter variable with two different parameters steady, e.g., power consumption is figured at different frequencies keeping the supply voltage at 0.3V and temperature at 250C in 65nm technology. The design is simulated using Tanner EDA apparatus 13.0 on 65nm technology. We can figure power, delay and power delay product (PDP) for the proposed circuit. Plans are tried in biasing condition when different supply voltage, working frequency, and temperature are taken. The diagram gives the correlation after effect of the two designs. The proposed configuration result is better in contrast with existing design.

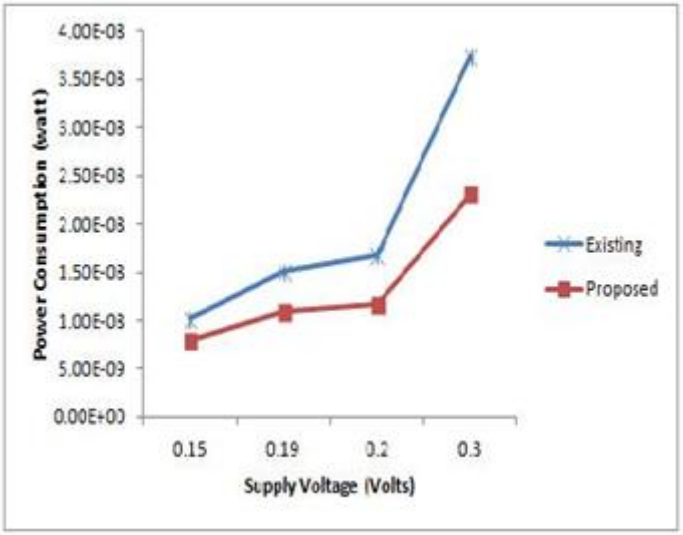

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Fig.4. Power Consumption with different supply

Fig 4 demonstrates the chart for power utilization by keeping frequency at 5MHz and Temp at 250C. In this diagram supply voltage is differs from 0.15 to 0.3.

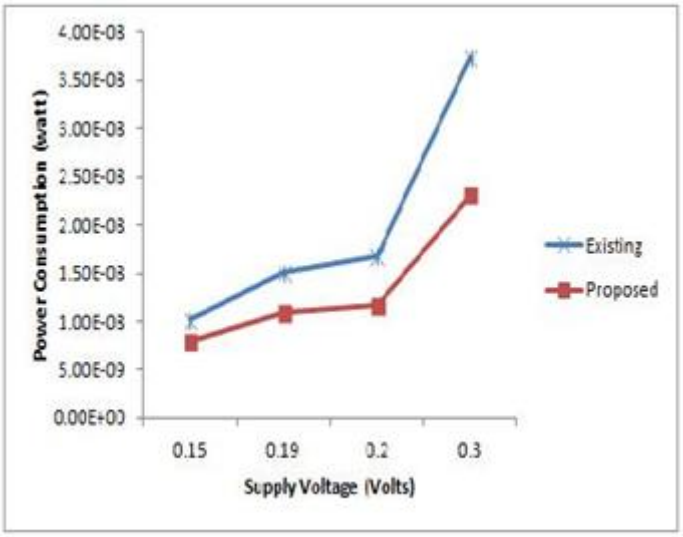

Fig.5. Power Delay Product with different supply voltage

Fig. 5 demonstrates the chart for power delay product for various supply voltage from 0.15 to 0.3 by keeping frequency at 5MHz and Temperature at 250C.

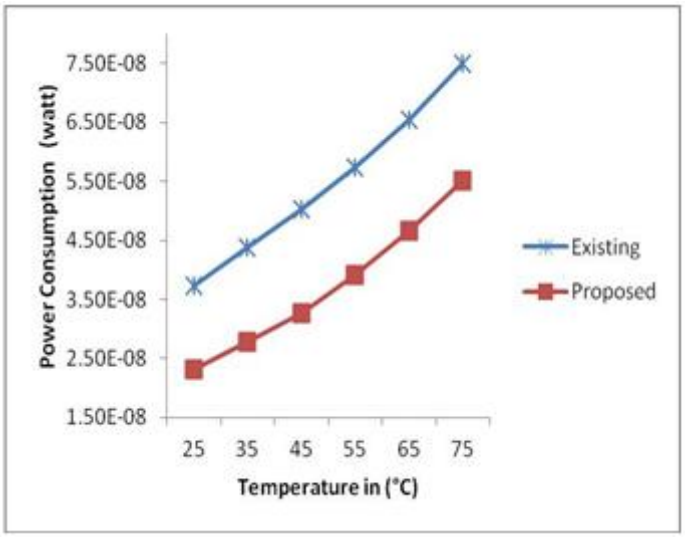

Fig.6. Power Consumption with different temperature

In fig.6 power consumption is calculated by keeping supply voltage at 0.3 and frequency at 5MHz for different temperature.

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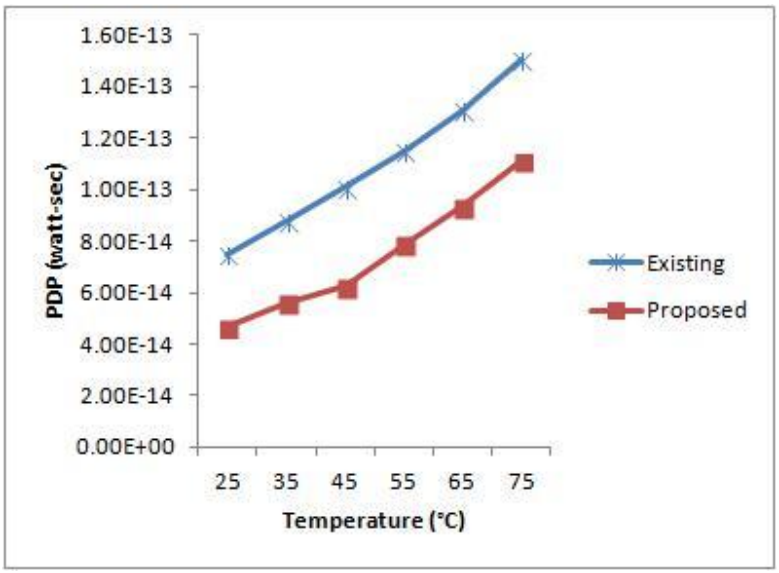

Fig.7. Power and delay product with different temperature

Fig.7 Show the graph of power delay product at different temperature. In this the temperature is varies for 25^0C to 75^0C

In fig.8 power consumption is calculated by keeping supply voltage at 0.3 and temperature at 25^0C for different frequency.

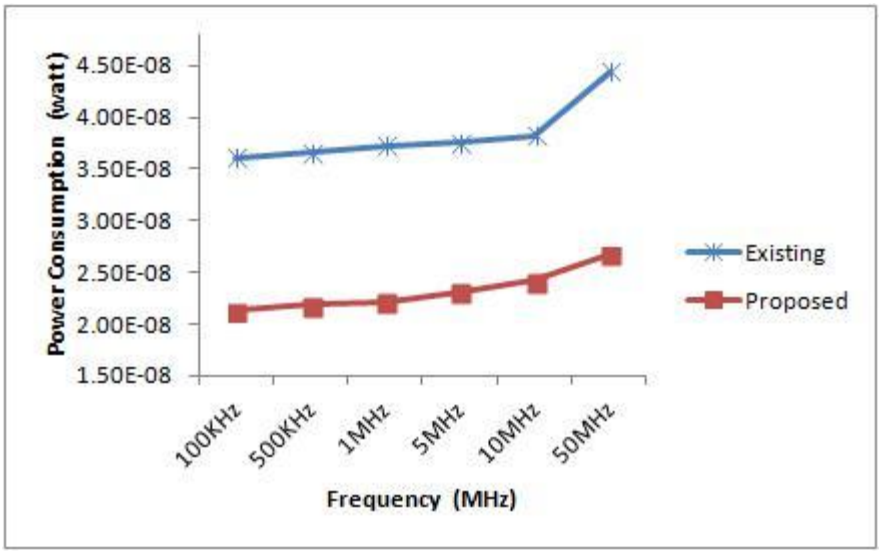

Fig.8. Power Consumption with different frequency

Fig. 9 shows the power delay product with temperature of 25^0C and supply voltage 0.3V at different frequency. In this the frequency is varies from 100 KHz to 5MHz.

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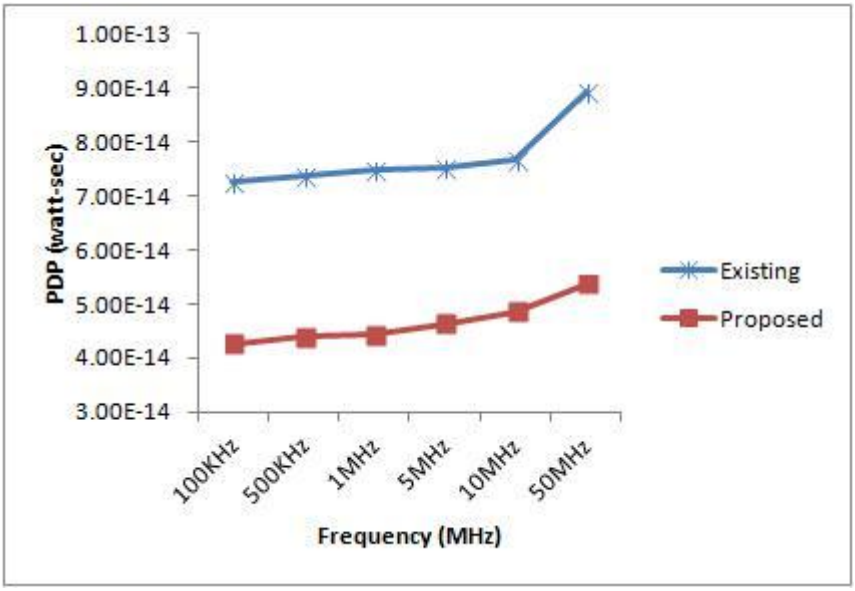

Fig.9. Power and delay product with different frequency

IV. CONCLUSION

In this paper we have executed versatile body bias technique method to enhance the execution of existing circuit. The methods for this circuit working in sub threshold region have been displayed. The D-latch configuration demonstrates the better execution as far as power utilization, delay and power delay product among existing present research article. This design is tried in 65nm technology; accordingly it is likewise independent technology. Consequently the proposed design of D-latch is reasonable for versatile application, as it is more power utilization, delay and power delay product (PDP) efficient.

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