Design and Analysis of 90nm nMOSFET for Lower Leakage

Prashant Kumar[1], Kanika Jain[1], Munish Vashishath[1], P K Bansal[2]

[1]*Department of EE, YMCA University of Science & Tech. Faridabad, Haryana, India*

[2]*Former Principal, MIMIT Malout, Punjab, India*

ABSTRACT – *In today time Leakage is a big challenge in MOSFETS based circuit. The focus of the research is to develop MOSFET and lower the technology. The off state current which is contributed by the sub threshold current has become a major issue while reducing the size of a MOSFET. The suppression of Short channel effects (SCE) can be achieved by Lightly-Doped Drain (LDD), halo implantation and retrograde well implantation. In this paper characteristics of* I_d-V_{gs} *, off state leakage current (*$_{Ioff}$*), ratio of* I_{on}/I_{off} *have been analyzed for better performance of MOSFET at 90nm.*

Keywords- *Halo implant, Leakage, Lightly-Doped Drain implant, Retrograde implant, Short channel effects*

1. INTRODUCTION

The miniaturization demand of MOSFET has been increased continuously and this continuous shrinking of MOSFET caused short channel effects (SCE), static power dissipation and high off- state leakage current. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) should dissipate low power and have better performance. Scaling of MOSFET is carried out due to the following reasons:

1. Reduced chip area is required to accommodate more transistors per chip.
2. Fabrication cost is reduced which depends on Production of number of chips per wafer [1].
3. Lower switching time and improvement in speed are achieved due to smaller capacitance

Scaling of MOSFET can be performed by two different scaling techniques: constant field scaling and constant voltage scaling [2]. The basic principle employed in Constant field scaling to increase the MOSFET performance is the reduction of the transistor size linearly along with the supply voltage and by increasing the concentration of dopant such that there is no effect on electric field. Power supply (V_{dd}), Threshold voltage (V_t), channel length (L), oxide thickness (T_{ox}) are scaled by a same factor, S while electric field remains the same.

Main drawback of this scaling is carrier mobility degradation due to high doping in the channel and short channel effects thus device performance is degraded. In constant voltage scaling the value of the length of the channel (L_{ch}), oxide thickness (T_{ox}) are reduced by a scaling factor, (S>1) and value of Power-supply (V_{dd}), Threshold voltage (V_t) remain unchanged. The doping densities are increased by a factor of S^2 (N_a, N_d) [3].

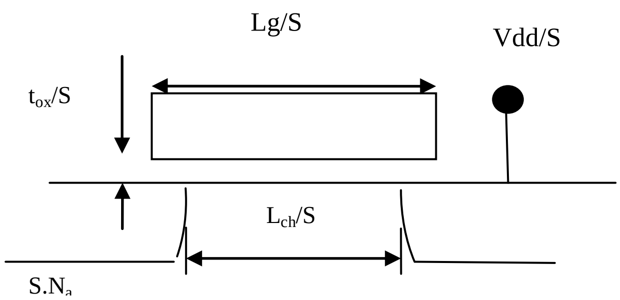


Fig.1: Constant-Electric-Field Scaling

Fig 1.shows the value of oxide thickness (T_{ox}), length of the channel (L_{ch}), length of the gate (L_g), power supply (V_{dd}) are reduced by a scaling factor (S) and the doping density (N_a) is increased by a factor S.

2. METHOD FOR REDUCTION OF SHORT CHANNFEL EFFECTS

In the current reported work Retrograde well and Halo implantation is used to reduce the effects of punch-through while lightly doped drain is applied for removal of hot carrier effect [4]. To minimize the off-state leakage current, the thickness of the oxide and gate depletion width (d_m) should be reduced to reduce the short channel effect [5]. This is shown in equation below

$$Wdm = \sqrt{\frac{4\epsilon si\varphi B}{qNa}} \quad (1)$$

Retrograde implant creates a channel at the surface having less concentration which increases its mobility, while the region at the surface having high doping reduces the punch-through effect by becoming a barricade against it [5].

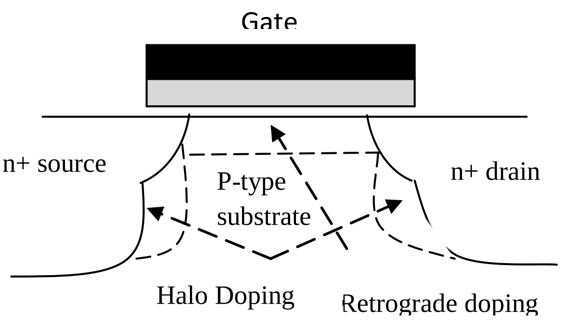


Fig.2: Halo-Doping

Fig.2 shows halo doping near source-drain extended regions and retrograde well to reduce the short channel effects. Halo doping creates a two-dimension distribution of dopant near the Source –Drain extended regions

Implantation of Lightly Doped Drain reduces the high drain electric field as compared to source/drain region to reduce the hot carrier effects [6].

3. THESHOLD-VOLTAGE ADJUST IMPLANT

With increase in the substrate doping of a MOSFET, threshold voltage also increases. Boron can be used to shift up the threshold voltage while arsenic can be used to shift down the threshold voltage [7].

Threshold voltage is given by

$$Vt = \varnothing ms - \left(\frac{Qtot}{Cox}\right) + 2 \in q \frac{\sqrt{KsieNsub\varnothing F}}{Cox + 2\varnothing F} \qquad (2)$$

Where

K_{si} = Dielectric constant of Silicon, Q_{tot} = total charge on oxide, N_{sub} = concentration of substrate, C_{ox} = capacitance of Oxide, $\varnothing ms$ = difference of work function between metal-semiconductor.

The equation, (2) shows the V_t of a long channel MOSFET which has uniform doping [3]. Keeping the material of implant and substrate same and dmax greater than the effective implant depth Xj, the shift in V_t can be given by equation below [2]

$$\Delta Vt = q/DiCox \qquad (3)$$

D_i is implantation dose for V_t adjust, X_j is effective implant depth.

4. RESULTS AND DISCUSSION

4.1 Simulated Results

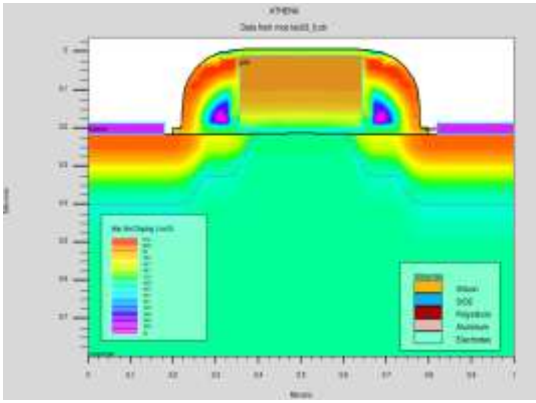
Table 1: Parameters and Their Values Used in the Simulation of 90nm Process

Process	Parameter	Value
Initial substrate	Phosphorous (P)	1.0e14 cm^{-3}
	orientation	<100>
Retrograde well	Boron (B)	1e12 cm^{-3}
	Energy	100 KeV
Gate oxide	SiO_2	2nm
Threshold voltage (Vt) adjust implant	Boron (B)	4.0e13 cm^{-3}
	Energy	10 KeV
Poly Deposition	-	100nm
Source/Drain Extension(LDD)	Arsenic (As)	2.0e12 cm^{-3}
	Energy	20 KeV
	Boron (B)	4.6e12 cm^{-3}

Halo implant	Energy	40 KeV
	Tilt	60^{0}
	Rotation	Full
Spacer deposition	-	100nm
Source/Drain	Arsenic (As)	1e15 cm^{-3}
	Energy	50 KeV
Rapid thermal Annealing (RTA)		^{0}

The Athena package of Silvaco TCAD Tool is used for simulation of the structure and all the process steps during the fabrication of nMOSFET. Various parameters used for simulating the 90nm nMOSFET are given in Table 1.

4.2 Simulated nMOSFET structures



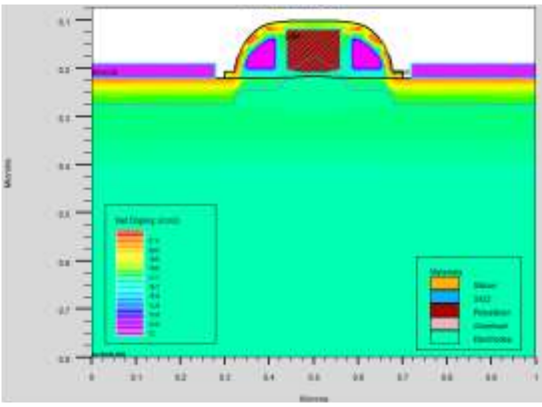
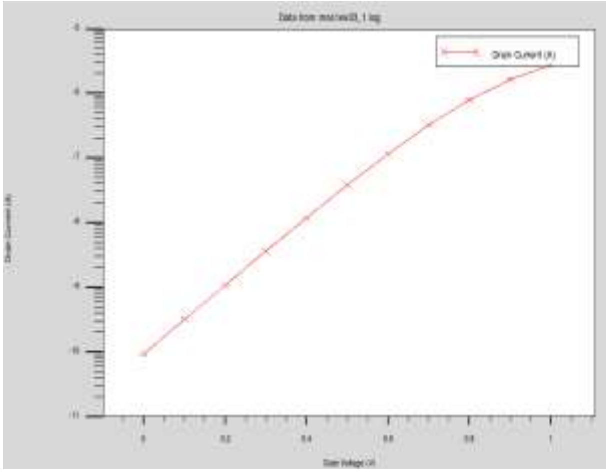


Fig.3: Structure of nMOSFET After All the Processing Step without Halo Doping and Retrograde Implant Fig.4: Structure of nMOSFET With All the Fabrication Techniques

Figure 3shows the simple nMOSFET structure without halo doping and retrograde well. The figure 4 shows the nMOSFET structure implemented with all the discussed techniques

4.3 Analysis of Electrical characteristics of nMOSFET



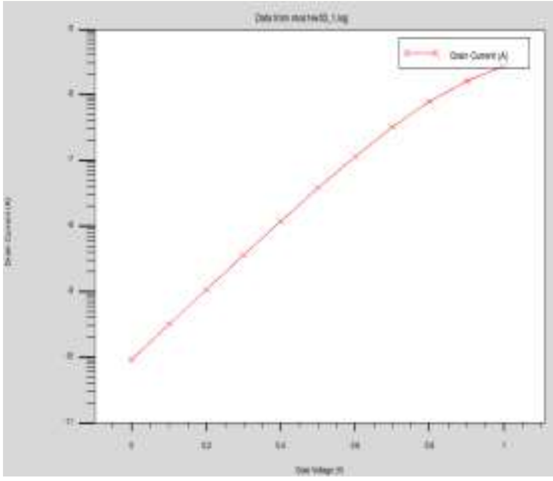


Fig.5: 90nm nMOSFET I_d - V_{gs} Characteristics (Semilog) Fig.6: 90nm nMOSFET I_d-V_{gs} Characteristics with Retrograde Well Implant (Semilog)

The Id-Vgs characteristic of nMOSFET with LDD with a sub threshold leakage 2.80 x 10^{-10} A is shown in Fig.5. The Fig.6 shows the I_d - V_{gs} characteristics for retrograde well where leakage is reduced up to 2.24 x 10^{-10} A. Finally, with the implantation of Halo the leakage is found to be 4.53 x 10^{-11} A and characteristics is shown in Fig. 7. The value of I_{on} is approximately equal in all the three cases. Table II shows the results of I_{off} and I_{on}/I_{off} for using different fabrication techniques.

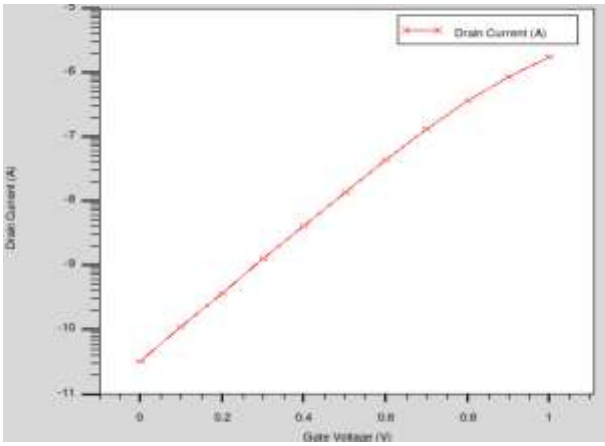


Fig.7: 90nm nMOSFET I_d - V_{gs} Characteristics with Halo and Retrograde Techniques (Semilog)

5. I_{ON} AND I_{OFF} CURRENT

At V_{gs}=0, I_d current is called as the I_{off} current. To minimize the power consumption of the MOSFET, I_{off} current should be very small [6]. Improvement in the speed can be achieved by maximizing the Ion current with a smaller threshold voltage, V_t but it can increase the leakage current Ioff. So, thickness of oxide (T_{ox}) should be thin enough to improve the threshold voltage roll-off as well as Ion current [8].

Table 2: Table of Result

Process techniques	Leakage observed (I_{off} A)	I_{on}/I_{off}(uA/nA)
Simple MOS, LDD	2.80 x 10^{-9}	6.28
LDD, Retrograde well	2.24 x 10^{-10}	78.571
LDD, Retrograde well, implantation of Halo	4.53 x 10^{-11}	388.52

6. THRESHOLD VOLTAGE DEPENDENCE ON DIFFERENT PARAMETERS.

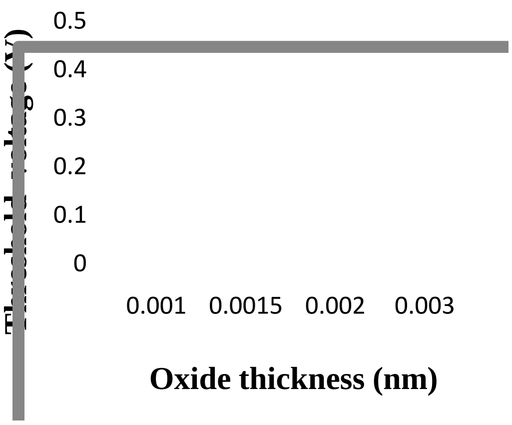
6.1 Effect of Thickness of Gate Oxide:

The oxide material and its thickness directly affect the threshold voltage (V_t). Fig.8 presents the influence of a change in gate oxide thickness on threshold voltage.

$$Vt = Vto + \gamma\left(\sqrt{|Vsb + 2\emptyset F|} - \sqrt{|2\emptyset F|}\right) \qquad here\ \gamma = \left(\frac{Tox}{\epsilon ox}\right)\sqrt{2q \in siNa} \qquad (4)$$

The equation , (4) shows the dependence of gate oxide thickness on threshold voltage [3].

Here V_t is the threshold voltage when there is a presence of substrate bias, V_{to} is threshold voltage when substrate bias is zero, V_{sb} is the substrate bias of source-to-body, 2ΦF is the potential at the surface, parameter of body effect is γ, T_{ox} is thickness of oxide, ε_{Si} is permittivity of silicon (Si), ε_{ox} is oxide permittivity (SiO_2), N_a is the acceptor doping concentration, q is Elementary charge. It can be seen that V_t is directly proportional to γ, and T_{ox} .Thus, when the thickness of oxide is very less, the threshold voltage will be reduced.



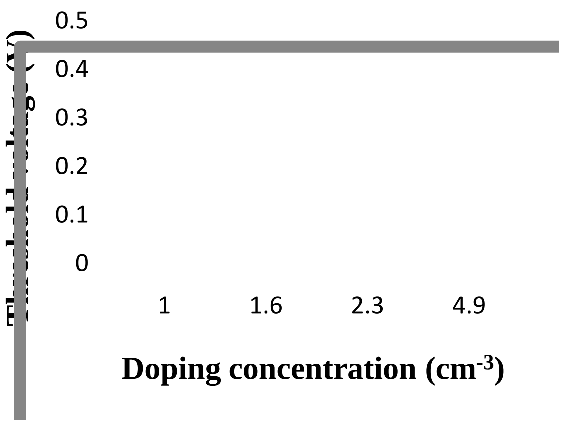


Fig. 8: Variation of Threshold Voltage with Thickness of Oxide Fig. 9: Variation of Threshold Voltage at Different Doping Concentration

From the figure 8 it can be seen that with the thickness of gate oxide is reduced, the threshold voltage (V_t) is also reduced.

6.2 Effect of Threshold voltage adjust implantation on concentration of dopant:

The Threshold voltage (V_t) directly depends upon threshold voltage implant doping concentration and is shown in Fig.9. It is suggested that lower doses are always be used for this implantation, because it requires only a little variation in the concentration of gate for the adjustment in V_t.

7. CONCLUSION

nMOSFET of 90nm technology has been designed using different Channel engineering techniques like halo doping, retrograde well and LDD implant and the leakage analysis has been carried on Silvaco-Athena package. Leakage reduction up to 4.53×10^{-11} A has been obtained using halo doping. It can also be calculated that since the threshold voltage directly depends upon thickness of oxide (T_{ox}). Hence with reduced T_{ox}, the threshold voltage V_t will be lower and it will increase the speed. Incorporation of these techniques will reduce the power dissipation and improve the speed of circuit.

8. REFERENCES

[1] Kaushik Roy, Saibal Mukhopadhyay, Mahmoodi, Leakage Current Mechanisms and Leakage Reduction Techniques in Deep- Sub micrometer CMOS Circuits, *proceedings of the IEEE, vol. 91, no. 2, February 2003*

[2] Parul Trivedi, Arun Kumar Chatterjee, Hansa Rani Gupta, *Design and Verification of nMOSFET for Low Leakage at 90nm Process Technology*,2013, (CSNT).

[3] Sung-Mo Kang, *CMOS Digital Integrated Circuits Analysis and Design* (Third Edition)

[4] A. Lakhlef, A Benfdila, H. Achour and K. Bennamane, *Characterization of the Short Channel Effect on the Threshold Voltage in Deep Sub-micron MOSFETs*, 2008, African Physical Review 2 Special Issue (Microelectronics).

[5] Kaushik Roy, Sharat C. Prasad, *Low Power CMOS VLSI Circuit Design* (Wiley India , 2010).

[6] Yannis Tsividis, *Operation and Modeling of the MOS Transistor* (Oxford University press, Second edition, 2003).

[7] Maizan Muhammad, Sunaily Lokman, Hanim Husain, Optimizing and fabricating 90nm NMOS Transistors on Silvaco, *IEEE Student Conference on Reserch and Developement, 2009*

[8] Richard S. Mulle, *Device electronics for integrated circuits by* (Wiley India 1986).

[9] Stanley Wolf, *Silicon processing for the VLSI era, the submicron MOSFET Deep-Submicron Process Technology* (volume 4)

[10] Silvaco TCAD available at "ATLAS User's Manual, Device Simulation Software", "ridl.cfd.rit.edu/products/manuals/Silvaco/atlas_users.pdf "

[11] Silvaco TCAD available at "ATHENA User's Manual, Device Simulation Software", "https://perso.esiee.fr/~polleuxj/Documents/athena_users.pdf "