International Conference on New Era in Technologies, Science and Role of Management
Parvatibai Genba Moze College of Engineering, Wagholi, Pune NETSRM-18
9th-10th April 2018 www.conferenceworld.in ISBN: 978-93-87793-13-2

POWER DISSAPATION CHARACTERISTICS IN VARIOUS ADDERS

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ABSTRACT

Adders the most elementary circuits present in the ALU. They are implemented using logic gates, transistors, FETs, CMOS, etc. Adders implemented using CMOS are very efficient and cost efficient. The power dissipation is comparatively less and circuitry is also simple. They can be implemented using Microwind software for simulation purpose.

KEYWORDS: Adders, Carry Skip Adder, Full Adder, Power Dissipation, Ripple Carry Adder.

I.INTRODUCTION

Adders are digital circuits that perform addition of binary bits. They can be implemented using logic gates like AND, OR, NOT, EXOR, EXNOR, etc. or by using transistors or FETs or CMOS. Adders perform very basic arithmetic operations which are used in almost all processors. Adders implemented using CMOS are very popular now-a-days because CMOS implementation gives a low power dissipation. CMOS stands for Complementary Metal-Oxide Semiconductor and is used in various applications like microprocessors, microcontrollers, analog and digital circuits alike. The 'complementary' in CMOS refers to the design style of CMOS circuits, where complementary and symmetrical pairs of p-type and n-type MOSFETs are used. CMOS implementations of adders are used because of their high noise cancelling capabilities and low power dissipation.

Here we discuss three types of adders and their CMOS implementation:

1. 8T Full Adder
2. Ripple Carry Adder
3. Carry Skip Adder

A full adder circuit performs addition by the combination of three bits and gives a sum and a carry output. The ripple carry adder is a modified full adder which adds two numbers and the third bit is the carry bit of the previous addition. The carry skip adder is also a full adder or a modified ripple carry adder where the delayed is decreased in propagation.

II.ADDERS DISCUSSED

The three adders which are discussed are described below with their CMOS implementation and layout generation:

1.1 8T Full Adder:

A full adder circuit is implemented for adding three binary bits. In CMOS, 2 XOR gate is implemented to get the sum output[2]. For carry 2TMUX is used. Thus the sum and carry module need 6 and 2 transistor respectively. The sum bit and the carry bit is implemented as:

$$Sum=a\oplus b\oplus c$$

$$Carry=ab+bc+ca$$

Advantages:

(i) It can efficiently handle the voltage level problems.

(ii) The power delay product and the area of the adder, is better when compared to another type of adders.

Disadvantages:

The power dissipation is comparatively high.

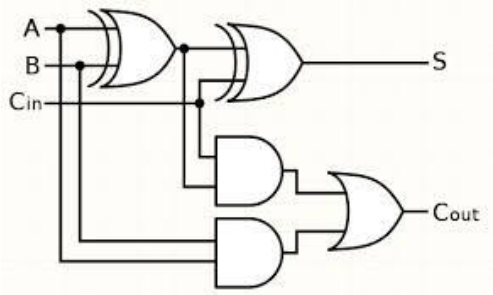


Fig. 1 Full Adder using logic gates

This circuit has been implemented using CMOS logic:

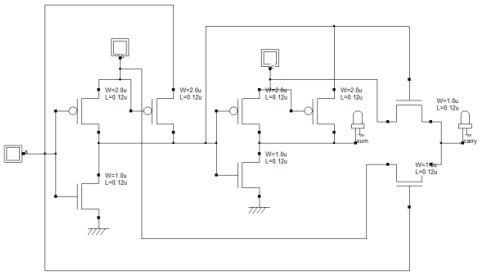


Fig 2.CMOS implementation of 8T Full adder

The corresponding layout generation is:

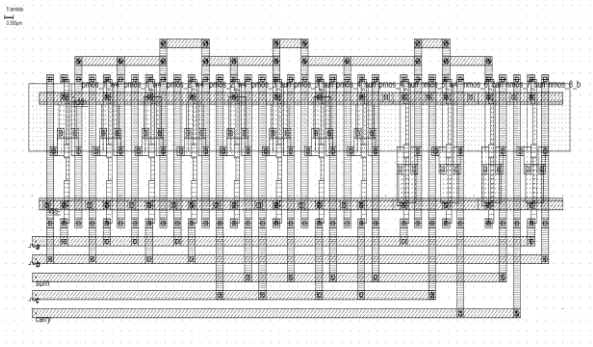


Fig.3. Layout generation of CMOS implemented 8T Full Adder

1.2 Ripple Carry Adder:

The Ripple Carry Adder is a series of full adder, in which the carry of the first full adder is given to the succeeding stages (the carry ripple to the next stage).By using this method the carry is increased when the stages get increased, this cause much delay in the adder circuit. This delay can be eliminated by removing an inverter in the circuit. The reason for these delays is the propagation delay in the logical circuit. Propagation delay is the time elapsed between the application of the input and the corresponding output. Similarly the carry propagation delay is the delay occurred due to the time elapsed between the carry input signal and the generation of carry out signal[3].

Advantages:

(i)The ripple carry adder is more efficient and low cost.

(ii)Power consumption is less and thus produces a compact layout with a smaller chip area.

Disadvantages:

Due to the feedback connection of carry from one stage to the next stage produces an inappropriate delay and the delay is linearly proportional to the number of stages (N).

The gate level implementation of ripple Carry Adder using 4 full adders is shown below:

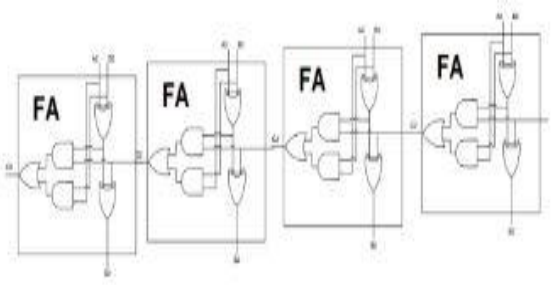


Fig 4.Gate level implementation of Ripple Carry Adder

The above Ripple Carry Adder is generated using transistors in microwind and their corresponding schematic layout generation is given below:

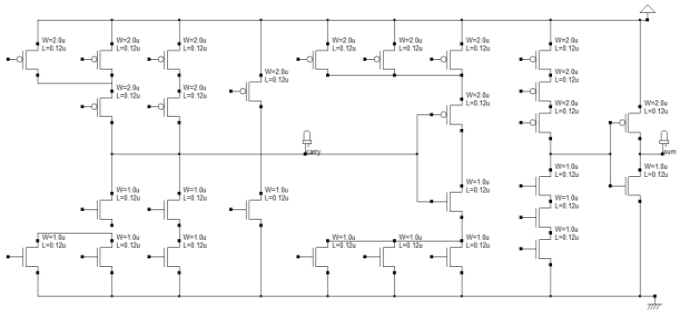


Fig 5. CMOS implementation of ripple carry adder

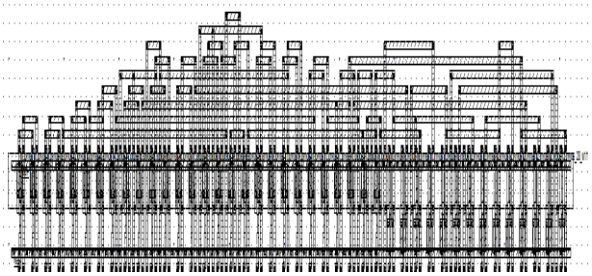


Fig 6.Layout generation of ripple carry adder

2.3 Carry Skip Adder:

A carry skip adder is a modified ripple carry adder that improves the delay time of the ripple carry adder. The delay time is reduced by skipping directly to iteration i without waiting for rippling. So this adder saves time as delay propagation is reduced. The stages are divided into blocks to implement this adder.

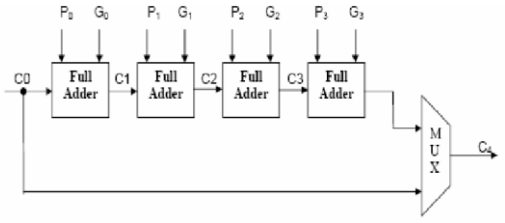


Fig 7.Carry Skip Adder

Advantages:

(i) In CSA, carry chaining is avoided.

(ii) The propagation and carry delays are eliminated.

Disadvantages:

It is more useful when there more than three operands.

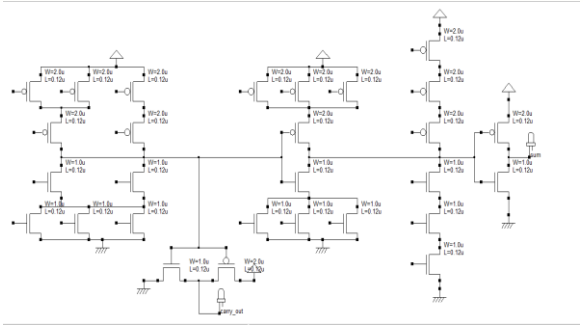


Fig 8.CMOS implementation of carry skip adder

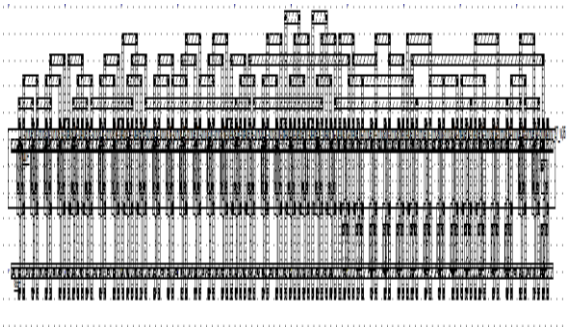


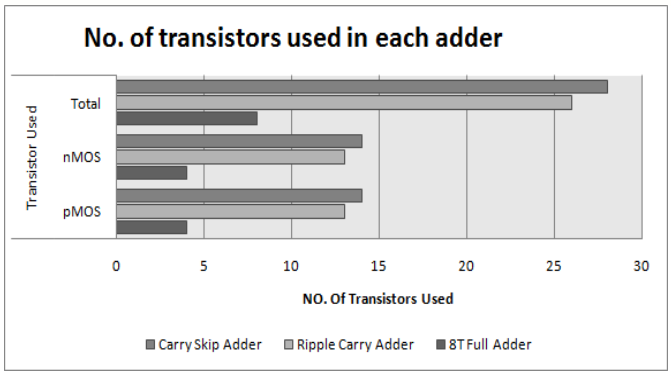
Fig 9: Layout Generation of Carry Skip Adder

III.COMPARISON

The number of transistor used for the implementation of the full adder, Carry Save Adder, Ripple Carry Adder is tabulated as follows:

Type of Adder	Transistor Used		
	pMOS	nMOS	Total
8T Full Adder	4	4	8
Ripple Carry Adder	13	13	26
Carry Skip Adder	14	14	28

Table 1:No. of transistors used in each adder

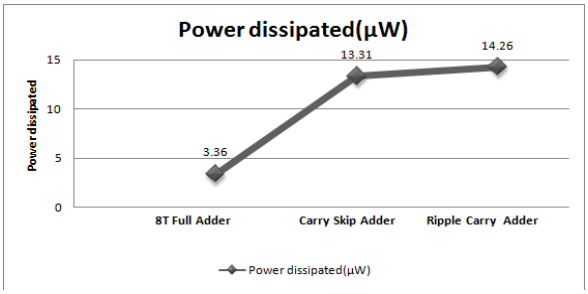


Graph 1:No. of transistors used in each Adder

The power dissipated is tabulated as:

Type of adder	Power dissipated(µW)
8T Full adder	3.36
Carry Skip Adder	13.31
Ripple Carry Adder	14.26

Table 2: Power Dissipated by the Adder

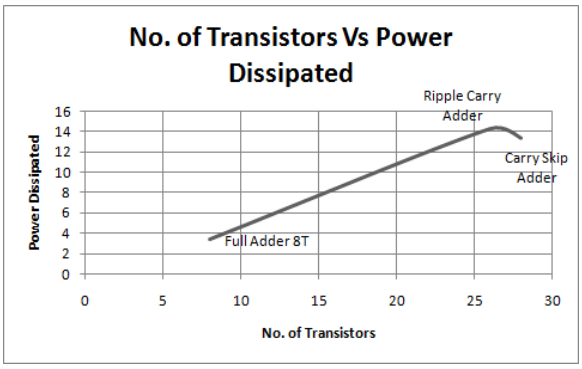


Graph 2: Power Dissipated Vs. Adder Used

The power dissipated vs the number of transistors used is tabulated as:

Type Of Adder	No. of transistors	Power Dissipated(µW)
Full Adder 8T	8	3.363
Ripple Carry Adder	26	14.226
Carry Skip Adder	28	13.317

Table 3: Power dissipated Vs. No. of transistors Used



Graph 3:No. of transistors used Vs. Power dissipated

IV.CONCLUSION

From the implementation of 8T full adder, Ripple Carry Adder and Carry Skip Adder shown, using microwind we can analyze that the power dissipation is high for the ripple carry adder when compared to the carry skip adder, even though the carry skip adder has a higher number of transistors. Here we can conclude that by comparing these adders implemented here carry skip adder is the most efficient.

V.ACKNOWLEDGEMENTS

We would like to thank the Research Centre, Department of ECE, Valliammai Engineering College for carrying out our work.

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