A Comparative Analysis of Multilevel Inverter: A Theoretical Review

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ABSTRACT

This paper presents a theoretical analysis and review of multilevel inverter (MLI) topologies. Multilevel inverters are getting popular in applications like solar PV cell, fuel cell, uninterruptible power system (UPS) systems, motor drives, etc.The three most important topologies like diode-clamped inverter (neutral-point clamped), flying capacitor (capacitor clamped) and cascaded H bridge topologies have been discussed in this paper. Here different inverter topologies and most preferable modulation PWM techniques preferred for the particular topology, advantages and drawbacks are discussed. Also the conventionally available three level NPC (3L NPC) inverter and one new proposed NPC inverter topologies have been compared.It is observed that the topologies are closely related to each particular application, depending on their unique features and limitations like power or voltage level, performance, reliability, count of component used, costs and other technical specifications.

Keywords: Multilevel inverter (MLI), PWM techniques, Neutral-point clamped

I. INTRODUCTION

In recent year the demand of high power is increases, so the high power equipment requirement also increases in industries. In industries,the power drives recently being used most frequently to get better and desired output with reduction in the cost. The high-power drives has been one of the most active areas in research and development of powerelectronics in the last decades.The development of high-power converters (rectifier and inverter), medium-voltage drives, etc. with various topologies is the recent trend [1].

Now a days "Multilevel Inverters" are used in wide range of applications.The term multilevel starts with the three level inverter introduced by Nabae et al. Multilevel refers to the multiple connections of individual inverters termed as 'stages' to provide the output voltage with required 'levels'. Increasing the number of levels will result in the reduction of harmonic distortion. It is found to be of extreme importance in industrial applications like photovoltaic system (PV), uninterruptible power supply (UPS), fuel cell, etc. [2], [4].

The important features of a multilevel inverter are [5]:

1) MLI can generate output voltages with extremely lowdistortion and lower dv/dt.
2) MLI draw input current with very low distortion.

3) MLI generate smaller common-mode (CM) voltage, thusreducing the stress in the motor bearings.
4) MLI can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

II. MULTILEVEL INVERTER TOPOLOGIES

The commercially existing inverter topologies are diode clamped or neutral point clamped (NPC) inverter, flying capacitor (FC) and cascaded H bridge (CHB) inverter topologies are briefly explain in this section[2]. The classification is done based on type of dc source utilizingfor the particular topology as shown in Fig.1.

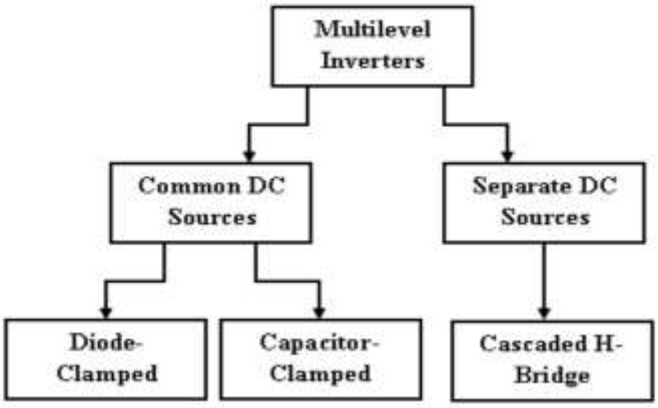

Fig. 1: Multilevel Inverter Topologies

2.1 Diode clamped or neutral point clamped (NPC) MLI

One of the traditionally accepted and widely used topology for various industrial and power sector applications is diode clamped or neutral point clamped converter which was proposed by Nabae, Takahashi and Akagi in 1981[3]. The diode-clamped inverter is also known as neutral-point clamped (NPC) inverter.

This inverter is consists of two pairs of series switches (upper and lower). Each phase has complementary switch pairs such that turning on, one of the switches of the pair require that the other complementary switch be turned off. Here common dc voltage source is share by both upper and lower switches which is then subdivided by two series connected capacitor. In between two capacitor the midpoint is there which divides the main DC voltage into smaller voltages. This midpoint of the two capacitors is defined as the “neutral point”, as shown in Fig. 2. As the two level inverter has the drawback of achieving higher power levels so three level inverter configuration was developed to meet the requirement of high voltage dc operation in traction application. Since all semiconductors are operated at a commutation voltage of half the dc-link voltage, thetopology offered a simple solution to extend voltage and powerranges of the existing two level technology, which were previouslylimited by the blocking voltages of power semiconductors withactive turn-on and turn-off capabilities. Hence, the converterwas of particular interest for median voltage MV applications.However, as the number of levels has increased the number of clamping diodes, switching devices and dc capacitors also increases, thus the circuit configuration becomes more complicated [4].

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In general, for an *m*-level diode clamped inverter, for each leg *2(m-1)* switching devices, *(m-1) * (m-2)* clamping diodes and *(m-1)* dc link capacitors are required. Generally, the voltage across each capacitor for an *m*-level diode clamped inverter at steady state is *Vdc/(m-1),* where *Vdc* is dc bus voltage. Switching devices in NPC topology are required to block only a voltage level of *Vdc* but the clamping diodes require different ratings to block the reverse voltage.

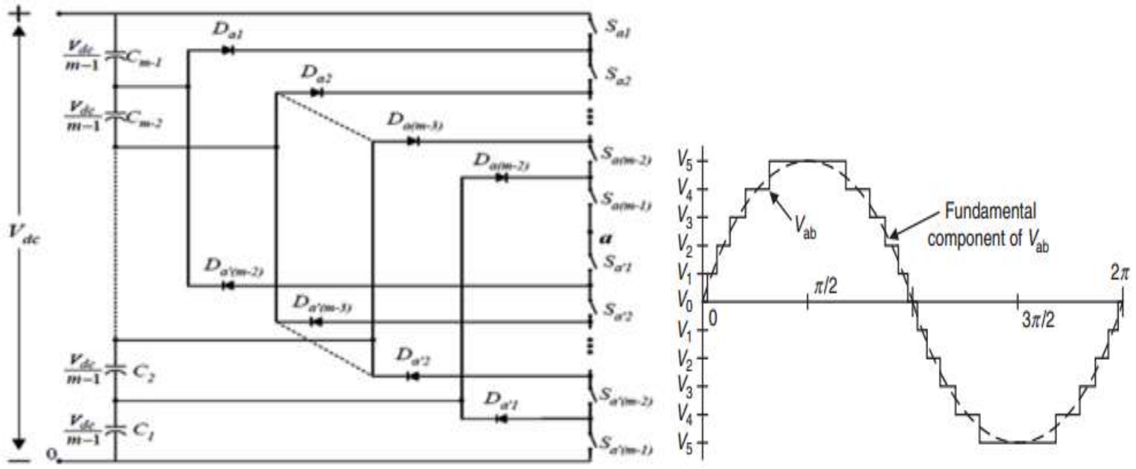

Fig. 2:*m*-level diode clamped inverter topology and its line voltage waveform

Though, the operation of NPC topology is simple and straightforward but as the number of inverter levels increases, number of devices increases and also increased the capacitor voltage balancing which becomes a major problem. Hence, design and implementationbecomes more complicated for higher number of levels.

There are different modulation schemes to generate the desired converter voltage. Commonly applied modulation methods in industry for diode clamped inverter are the carrier-based sine-triangle modulation [2] based on multiple-carrier arrangements in vertical shifts. In addition, the space-vector modulation has been extended for the multilevel case. From all these modulation technique any one can be preferred depend on in which application this inverter is used, but the most preferable is carrier-based sine-triangle modulation in which the sine wave is compared with triangular wave and provide PWM signal for the switches used in the inverter and also its implementation is easy. The Carrier-based sine triangular modulation is as shown in Fig. 3.

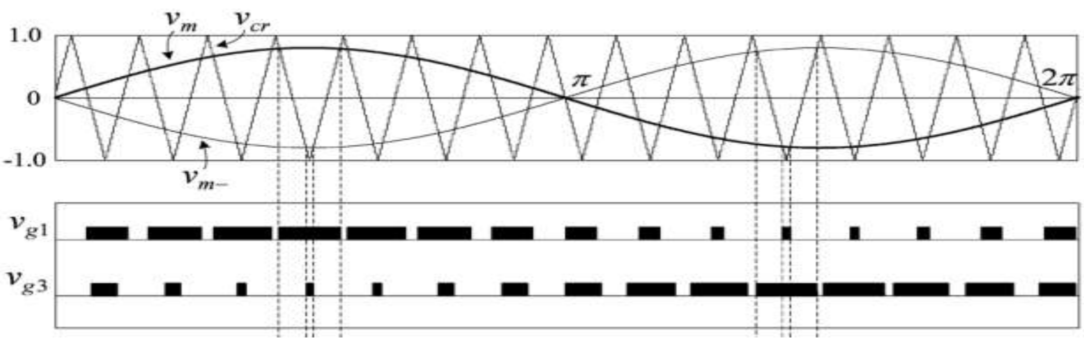

Fig. 3: Carrier-based sine-triangle modulation (Unipolar PWM)

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Following are the advantages of diode clamped or neutral point clamed MLI

i. All the phases share a common dc bus, due to which the capacitor requirements for the converter minimizes.
ii. As a group, capacitors can be pre-charged.
iii. Converter efficiency is high, if it operates at fundamentalswitching frequency.

While the disadvantages are the number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels.

Currently, the three level neutral point clamped inverter is the most widely spread topology in MV drives. MV-drive applications is a wide range of areas, among them are oil and gas, metals, power, mining, water, motor drives applications, marine, and chemical processes[5].

2.2 Flying Capacitor (FC) MLI

The Flying capacitor inverter alternatively known as capacitor clamped inverter topology which was proposed by Meynard and Foch.This inverter topology is similar to that of the NPC topologyexcept the usage of clamping diodes. This inverter topology uses capacitors instead of clamping diodes. Flying capacitor MLI has capacitors on dc side and connected like ladder structure, where the voltage across each capacitor differs from that of the next capacitor as shown in Fig. 4.The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Similar to neutral point clamped inverter, the capacitor clamped inverter requires a large number of bulk capacitors of voltage clamping. The voltage rating of each capacitor used will be the same as that of the main power switch, therefore, an m-level converter will require a total of (m - 1)(m - 2) ⁄2 clamping capacitors per phase leg in addition to (m - 1) main DC-bus capacitors. Thus, as the number of levels has increased, more number of storage capacitors are required which results in a bulky and expensive structure when compared to diode clamped inverter topology [5].

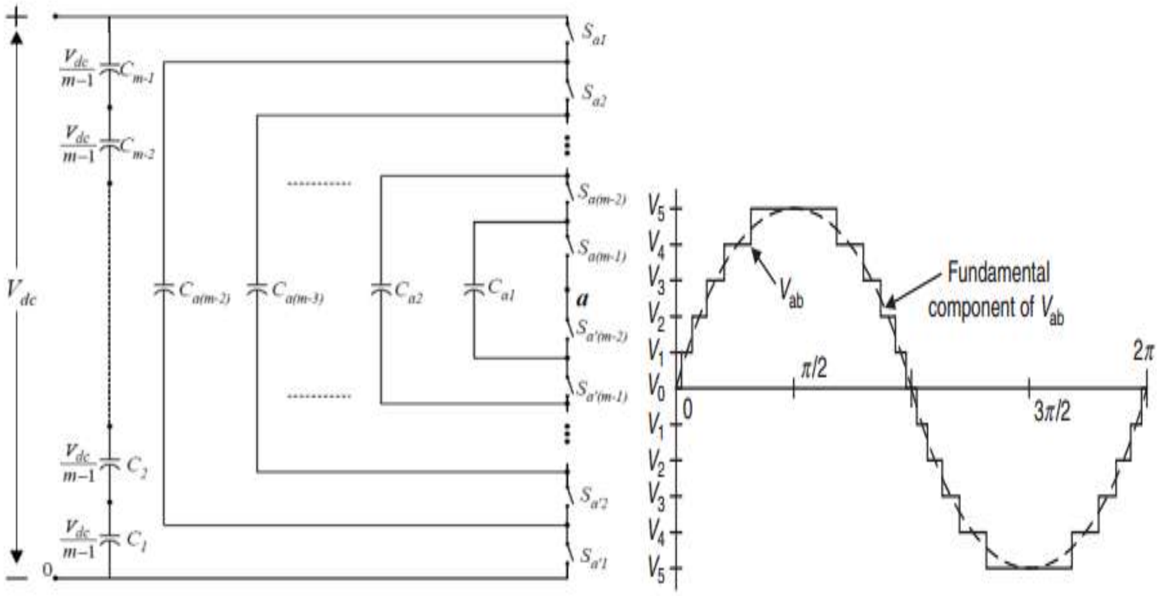

Fig. 4:*m*-level flying capacitor inverter topology and its line voltage waveform

Here also different modulation methods are available but the preferred modulation strategy is phase shift modulation (PS-PWM), since a natural voltage balance of the FCs is achieved [2]. The bipolar PWM is used instead of unipolar PWM which is shown in following Fig.5.

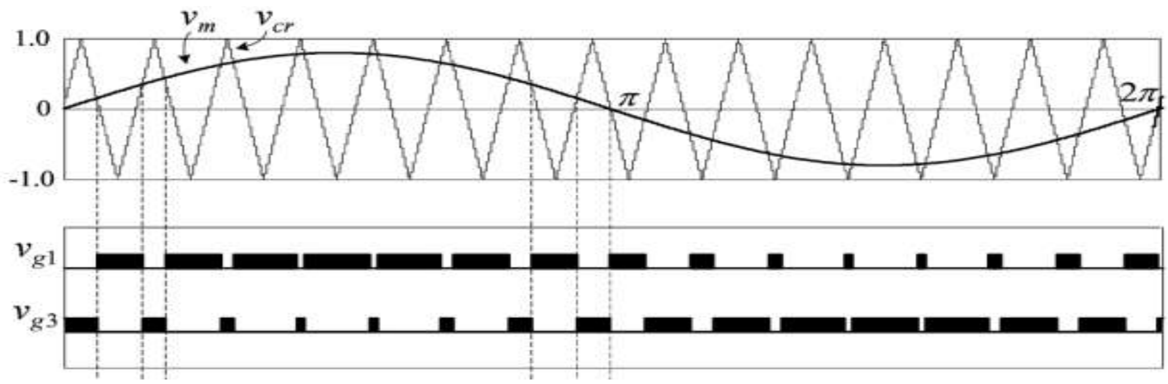

Fig. 5: Bipolar PWM

The main advantages of this topologies are as follows,

i. Phase redundancy due to which balancing the voltagelevels of the capacitors is possible.

ii. The large number of capacitors enables the inverter to ridethrough short duration outages and deep voltage sags.

iii. Real and reactive power flows can be controlled

The disadvantages are the requirement of more numbers of capacitorsresults in bulky and expensive structure than diode-clamped multilevel inverter and complex control is required to maintain the capacitorsvoltage balance so the inverter control is complicated for higher number of levels.

The major application of this topology are interesting in applications like high-speed MV drives and test benches, which require a high frequency of the fundamental output voltage.

2.3 Cascaded H Bridge (CHB) MLI

The concept of series H-bridge inverter was first proposed by R. H. Baker and L. H. Banister [38]. In order to overcome the drawbacks of NPC and FC topologies such as extra clamping diodes and capacitors, Marchesoni M.,et.al [5] have proposed Cascaded H Bridge Inverter. The basic idea of connecting single-phase H-Bridge inverters in cascade with multiple isolated dc supplies to realize multilevel waveforms was first introduced in 1990 for plasma stabilization. This topology structure has been subsequently extended for three-phase applications, such as reactive power compensation by Peng F.Z., et.al [7]. The CHB is designed by the series connection of H-bridge power cells as shown in Fig. 6. For this reason, the CHB is also known as a multi-cell inverter. Each cell includes a single-phase H-bridge inverter, a capacitive dc-link, a rectifier, and an isolated voltage source. The number of output phase voltage level is given by m=2s+1, where s is number of separate dc sources and by cascading H bridges the inverter voltage get added [5].

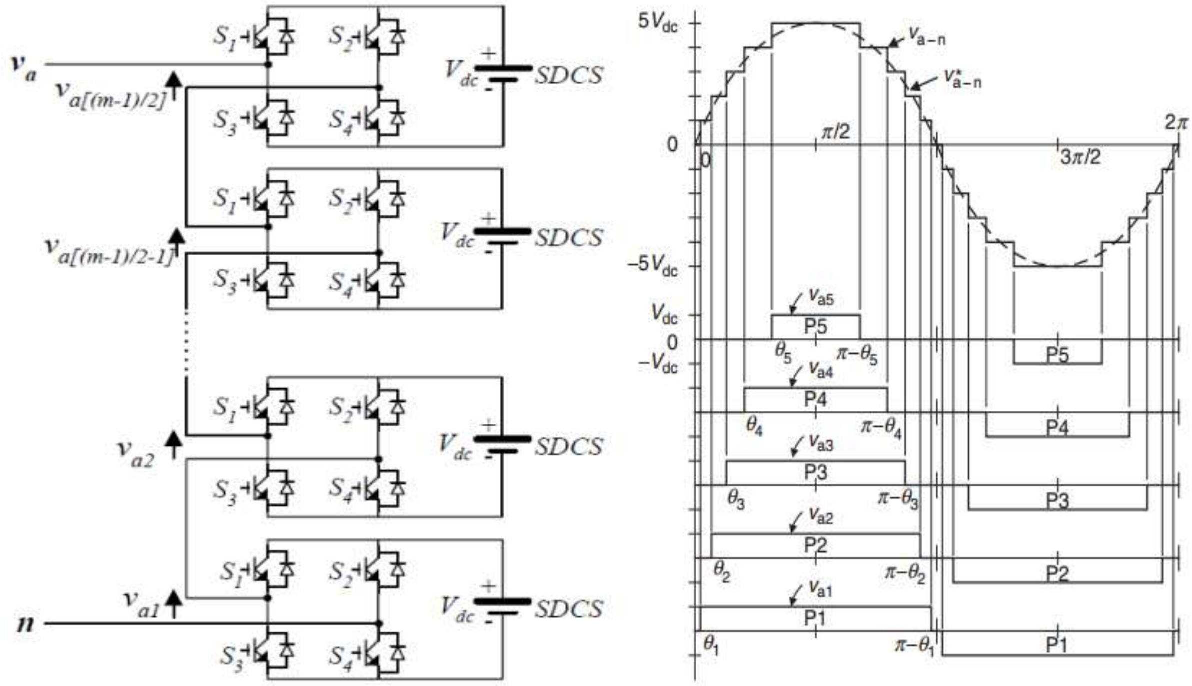

Fig. 6:*m*-level CHB inverter topology and its output voltage waveform

The three modulation techniques mentioned for the diode clamped inverter can also be implemented for the CHB but they present some drawbacks that makes them not the preferred for this inverter. So selective harmonic elimination (SHE) is slightly modified and referred as staircase modulation for CHB. For low-switching-frequency applications, the staircase modulation is used. The main advantage of this method is that the converter switches very few times per cycle, reducing the switching losses to a minimum and low-order harmonics are eliminated. Howeverthis method needs important offline calculations to compute the angles for a variety of modulation indexes and is therefore not very suited for highly dynamic systems.

Advantage of cascaded H bridge MLI are the number of possible output voltage levels is more than twice the DC sources ($m = 2s + 1$), simple voltage balancing and no extra clamping diodes or voltage balancing capacitors are necessary. But separate DC sources are required for each of the H bridges is major disadvantage of the topology which increases cost of the inverter [5], [6].

From the above discussion the comparative analysis is done and put it into the tabular form as shown in Table 1.

Table 1: Comparative analysis of MLI topologies

MLI topologies	**DCMLI or NPC MLI**	**Flying Capacitor MLI**	**Cascaded *H-bridge* MLI**
Description	Clamped diodes and dc capacitors are used in order to generate ac voltage.	Structure of this inverter is similar to DCMLI, Only difference is that clamping diodes are replaced by capacitors.	Several H-bridge cells connected in series and separate dc source required for each cell.

Switches	(m-1)*2	(m-1)*2	(m-1)*2
Clamping Diodes	(m-1)*(m-2)	0	0
DC-Bus Capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)*(m-1)/2	0
Advantages	All the phases share a common dc bus, which minimizes the capacitance requirements of the converter and Efficiency is high for fundamental frequency switching.	Phase redundancies are available for balancing the voltage levels of the capacitors.	The number of possible output voltage levels is more than twice the DC sources ($m = 2s + 1$) and Simple voltage balancing.
Drawback	The number of clamping diodes required is more and it should be properly connected.	Control is complicated to track the voltage levels for all of the capacitors.	Separate DC sources are required for each of the H bridges.

III.THREE LEVEL Z-SOURCE NPC MLI WITH TWO LC IMPEDANCE NETWORK

The three level neutral-point-clamped (NPC) inverters, having many inherent advantages, are commonly used for medium voltage ac drives and have recently been explored for other low-voltage applications including grid-interfacing power converters and high-speed drive converters. Three-level Z-source inverters were proposed for buck-boost energy conversion with all favorable advantages of three-level switching retained. Normally Z-source inverter means it utilizes the impedance network between dc source and the inverter [7]. Conventional three-level Z-source neutral-point-clamped (NPC) inverters are explored for medium-power and low-power applications. It provides better power quality at the same time voltage stress across switches and output filter requirements are less. This uses two isolated dc sources which may require isolation transformer and additional rectifier circuits (in case isolated dc sources are not readily available).Despite their effectiveness in achieving voltage buck-boost conversion, existing three-level Z-source inverters use two impedance networks and two isolated dc sources, which can significantly increase the overall system cost and require a more complex modulator for balancing the network inductive voltage boosting. This conventional topology’s circuit diagram is as shown in Fig. 7.

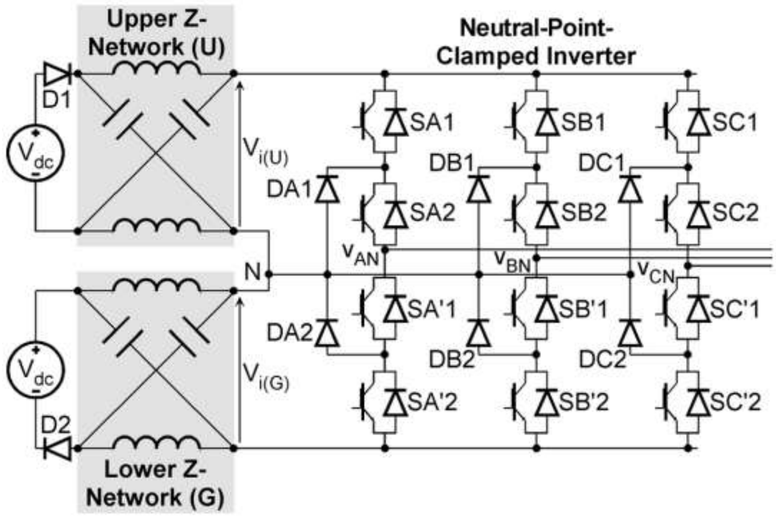

Fig. 7: Topology of Z-source NPC inverter with two LC impedance networks

As this traditional NPC inverter uses two Z-source impedance networks for boosting its dc inputvoltage from to a higher dc link voltagefor driving the inverter directly [8]. Although it is theoretically feasible,the inverter in Fig.7 is not a favorable economical solution,since it uses two isolated dc sources and a number of passive LC elements, which can significantly increase the cost, sizeand weight of the inverter [9].

IV.A NEW TOPOLOGY: THREE LEVEL NEUTRAL POINT CLAMPED (3L NPC) MLI WITH SINGLE LC IMPENDENCE NETWORK

A single-stage high-voltage gain boost inverter is getting popularity in applications like solar photovoltaic, fuel cell, uninterruptible power system (UPS) systems, etc. Previously, single-stage voltage boost multilevel Z-source inverter (ZSI) and quasi-Z-source inverter have been proposed for dc–ac power conversion with improvedpower quality. Multilevel ZSI uses more number of high-power passive components in the intermediate network, which increase the system size and weight. So here, a continuous current input three-level NPC inverter with *LC* impedance network is proposed, which uses comparatively less number of high-power passive components at thesame time retains all the advantages of multilevel QZSI/ZSI. It is able to boost the input dc voltage and give required three level ac output voltage in a single stage [11]. The circuit diagram for the proposed 3L NPC inverter with single LC network is as shown in Fig. 8 below.

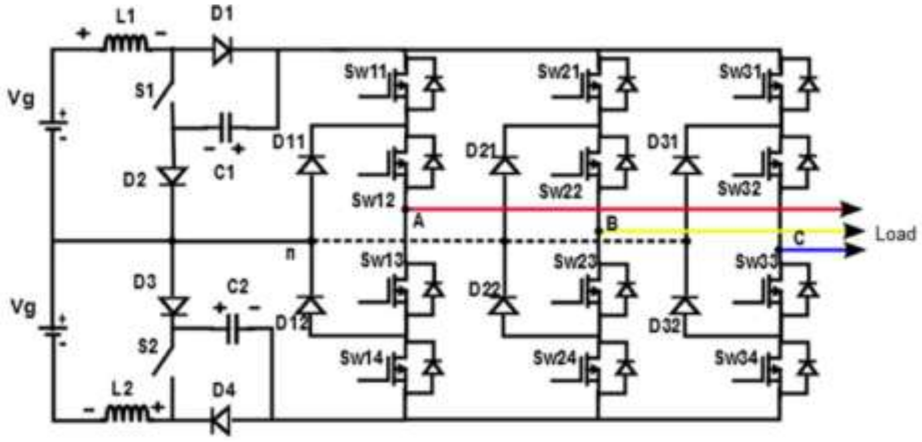

Fig. 8: Proposed topology ofa three level NPC inverter with single LC impedance network

From the above diagram it is seen that this circuit uses only one LC impedance network between the dc source and the inverter.Traditional Z-source NPC three-level inverter is basically operated in two states, i.e., active state (nonshoot-through state) and zero state to give three distinct voltage levels (i.e., +*V*dc, 0, -*V*dc). Whereas the proposed inverter uses additional one more state, i.e., shoot-through state to boost the input dc voltage and give

three distinct voltage levels (+*V*dc, 0, -*V*dc) in a single stage. In multilevel ZSI,[11] shoot-through state is utilized along with passive reactive element to boost the input dc voltage.

Table 2: Comparison of the circuit configuration for conventional 3L NPC inverter and proposed 3L NPC inverter

Parameters	Conventional topology	Proposed topology
Number of dc source	2	1
Number of LC network	2	1
Inductor	4	2
Capacitor	4	2
Diode	2	4

In the above table, it is seen that the component count of proposed 3L NPC inverter is less than the conventional 3L NPC inverter. So from this it is clear that as the component count is less, the overall weight and system size becomes less. And the most important factor the cost also less.

V.CONCLUSION

This paper has provided a brief comparative analysis and review of multilevelinverter circuit topologies. As the multilevel inverters are becoming very important in many industrial and commercial applications so here in this paper different inverter topologieswerediscussed with different applications, advantages and drawbacks. All the topologies are compared and put into tabular form. A conventional and proposed three level NPC inverter circuit configuration also been discussed and compared. It is concluded that the proposed topology with reduced number of inductor and capacitor was found to be cost effective and better than the conventional inverter.

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