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EFFICIENT LOW LEAKAGE NOVEL 10T SRAM CELL ARCHITECTURE

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ABSTRACT

When it comes to Modern Electronic systems Static Random Access Memory (SRAM) is the most common embedded- memory in Computers and portable electronic systems. By keeping today's trend in mind, design of low power and high packed memory chip in scaling limits and short channel effects (SCEs) is more hostile as Low power with supply voltages scaling degrades the stability of read/ write margin. Device scaling improves chip package, it produces more leakages.In this Paper, new 10T SRAM architecture proposed for low leakage and high stability. Leakage power, stability and area of proposed design are compared with existing cell structures.

Keywords:

I.INTRODUCTION

In system on chips (SOCs), 90% of power is on account of embedded memories which declines battery power . In battery operated devices, the high power and high speed memories is the prime target.. Static power rises at fast rate beyond 100nm. There is a decrease in V_{th}, and exponential rise in subthreshold leakage with reduced threshold voltage. Fig: 1 shows 5T, 6T, 7T, 8T and 10T SRAM cells. The basic 6T cell [1] consists of access transistors, cross coupled inverter pair. 5T SRAM [2] requires minimum number of transistors than 6T and improvements is offered 7T SRAM [3]. 7T comprises of three word lines (WWL, WLB, WL) and two complementary bit-lines (BL and WBL), which provides 62% of power reduction and large stability for write operation. 6T SRAM faces a numerous number of challenges like degradation of read static-noise-margin (RSNM) and write margin. To steer away RSNM problem, two more transistors are connected [4]. The two NMOS transistors forms read buffer circuit and the cell's read/write ports is segregated . This is configured so that it has two read ports (read WL and read BL) and three ports write (write WL, Write BL and write BLX) [8]. 10T SRAM has a pair of cross-coupled inverters conventionally, write retrieve devices, and decoupled read-out circuits. The write bit-lines (WBL, WBLB) and the read bit-lines (RBL) are pre-charged to V_{DD} before cell is accessed. Operation READ can be initiated by pulling up the RWL= V_{DD}, then the read bit-line (RBL) is discharged conditionally through pull-down transistors depending on the QB logic state.

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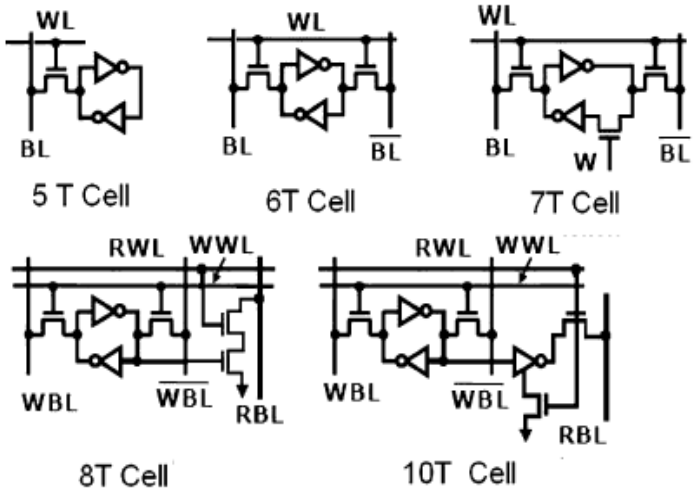

Fig. 1: ***Various SRAM bit cell architectures [5]***

Hence, from the RBL the cell node is decoupled and mode SNM during the read process is retained. When RWL is pulled down to ground, read process can be deactivated and the node QBB is changed to V_{DD} by the transistor T_{10} making the bit line leakage flow from the node QBB to RBL in spite of the data stored in the SRAM cell. which therefore results in a bit line leakage which is independent of the cell data and allows more number of cells to be attached to a single BL [6].

1. Novel 10T SRAM cell: In order to attain low power design focused more on subthreshold leakage. Novel 10T SRAM bit cell is proposed in this paper based on new biasing technique which controls both subthreshold and thereby acquiring a good stability. New 10T cell is shown in fig. 2. The transistors T_1, T_8 and T_3, T_6 forms cross coupled inverters. The key point which is highlighted behind this approach is the declination of leakage power, by precisely disconnecting the leakage path established between supply and ground. This is based on the observations made in [7].

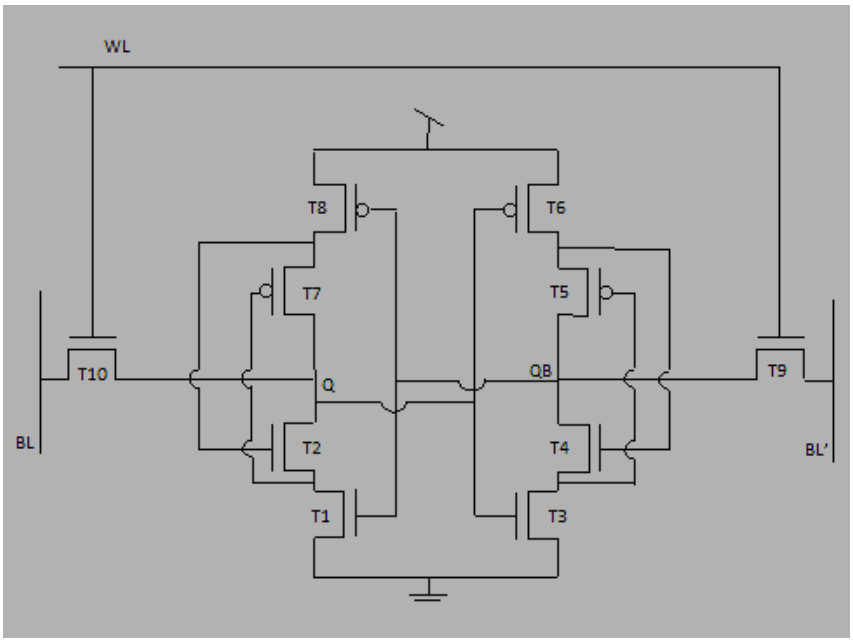

Fig: 2. ***Proposed 10T SRAM architecture***

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***1. Sub threshold leakage modeling*:** Weak inversion conduction current between source and drain comes to play when Vgs< V_{TH}. In account to SCEs and DIBL, the equation is given by

$$I_{DW} = K_1 I_o \exp\left(\frac{V_{gs} - V_{TH}}{n.^* V_T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right] - - - - - (1)$$

$$V_{TH} = V_{THO} + \Delta V_{TH}(SCE) + \Delta V_{TH}(DIBL) - - - -(2)$$

$$\Delta V_{TH}(SCE) = -\left(\frac{0.5 \times DV_{TO}}{\left(Cosh\left(DV_{TI} \times \frac{L_{eff}}{L_{to}}\right) - 1\right)}\right) \times (V_{bi} - \phi_s)$$

$$\Delta V_{TH}(DIBL) = \left(\frac{0.5 \times DV_{TO}}{\left(Cosh\left(D_{sub} \times \frac{L_{eff}}{L_{to}}\right) - 1\right)}\right)(ETA0 + ETAB + V_{bs})V_{DS}$$

Where, ETA0, ETAB: DIBL coefficients. The physical parameters are defined in BPTM. The details of the definition and computations can be found in BSIM 3V3 manual.

***2. Static noise margin (SNM):* S**tability measured by its SNM, depends on three factors such as cell ratio (CR), pull up ratio (PR) and supply voltage. The driver transistor is responsible for 70 % of the SNM value. CR is ratio between sizes of the driver/ load transistors during the read

$$CR = \frac{(W_1 / L_1)n}{(W_5 / L_5)n} \qquad CR = \frac{(W_3 / L3)n}{(W_6 / L_6)n} - -(3) \qquad \text{(OR)}$$

SNM has an impact on both the read/ write margins, related to 'V_{TH}' of the NMOS/PMOS devices. To enhance SNM, high 'V_{TH}' is required. However, 'V_{TH}' reduces with the scaling.

3. CR for reading logic 1: Read cycle begins with pre charging both bit lines to V_{DD}. Since Q=1, T_1& T_4 =ON. On connecting WL=V_{DD}' T_5 & T_6 ,are connected which makes the values of both charging nodes are transferred to the BLs. As no current flows through the T_6, the transistors T_4& T_6 pulls BL to V_{DD} & BL bar discharges through T_1& T_5. This enlarges the voltage at Q bar node from zero. But voltage at Q bar should not exceed par threshold of T_3 (V_{th3}**)**, otherwise the r T_3 will make'ON', leading to an unintended change in the stored cell.

Thus, If

$$\left(\frac{W_5}{L_5}\right) > \left(\frac{W_1}{L_1}\right) \text{ (OR) } L_5 < L_1$$

Resistance of T_5 < resistance of T_1

Hence design issue is:

$$V_{\bar{Q},\max} < V_{Th3} \text{ (OR) } \left(\frac{W_5}{L_5}\right) < \left(\frac{W_1}{L_1}\right)$$

When WL=V_{DD}, T_5= saturation and T_1= Linear region.

$$I_{D,SAT} = \frac{\mu_n C_{OX}}{2}\left(\frac{W_5}{L_5}\right)\left[V_{DD} - V_{\bar{Q}} - V_{Tn}\right]^2$$

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$$I_{D,lin} = \frac{\mu_n C_{OX}}{2}\left(\frac{W_1}{L_1}\right)\left[2(V_{DD} - V_{Tn})V_{\bar{Q}} - V_{\bar{Q}}^2\right]$$

$$I_{D,sat} = I_{D,lin}\cdot\frac{\left(\frac{W_5}{L_5}\right)}{\left(\frac{W_1}{L_1}\right)} = \frac{[2(V_{DD} - V_{Tn})V_{\bar{Q}} - V_{\bar{Q}}^2]^2}{[V_{DD} - V_{\bar{Q}} - V_{Tn}^2]^2}$$

Replacing $V_{\bar{Q}}$ by $V_{Tn,}$ we get

$$\frac{\left(\frac{W_5}{L_5}\right)}{\left(\frac{W_1}{L_1}\right)} < \frac{2(V_{DD} - 1.5V_{Tn})V_{Tn}}{(V_{DD} - 2V_{Tn})^2} ---(4)$$

4. CR for reading logic 0:

$$V_{Q,\max} < V_{Tn} \text{ as } I_{D,sat} = I_{D,lin}$$

$$\frac{\mu_n C_{OX}}{2}\left(\frac{W_6}{L_6}\right)[V_{DD} - V_Q - V_{Tn}]^2 = \frac{\mu_n C_{OX}}{2}\left(\frac{W_3}{L_3}\right)[2(V_{DD} - V_{Tn})V_Q - V_Q^2]$$

as $V_Q < V_{Tn}$, replacing V_Q by V_{Tn}

$$\left(\frac{W_6}{L_6}\right)[V_{DD} - V_{Tn} - V_{Tn}]^2 > \left(\frac{W_3}{L_3}\right)[2(V_{DD} - V_{Tn})V_{Tn} - V_{Tn}^2]$$

5. Pull-up ratio:

PR is the ratio of sizes of the load to access transistor during write operation and is given by

$$PR = \frac{(W_4 / L_4)p}{(W_6 / L_6)n}$$

When $V_Q = V_{Tn}$, T_4 = saturation & T_6 = linear region.

$$I_{D,sat} = I_{D,lin}$$

$$\frac{\mu_p C_{OX}}{2}\left(\frac{W_4}{L_4}\right)[0 - V_{DD} - V_{Tp}]^2 = \frac{\mu_n C_{OX}}{2}\left(\frac{W_6}{L_6}\right)[2(V_{DD} - V_{Tn})V_Q - V_Q^2]$$

But we need to have $V_{Q<} V_{Tn}$,

$$\frac{\left(\frac{W_4}{L_4}\right)}{\left(\frac{W_6}{L_6}\right)} < \frac{\mu_n(2V_{DD}V_{Tn} - 3V_{Tn}^{\ 2})}{\mu_p\{-(V_{DD} + 2V_{Tp})\}^2}$$

For different values of PR, the corresponding SNM has been calculated for supply voltage @ 1.0V. Based on observation the optimum PR=3.0 for the minimum SNM.

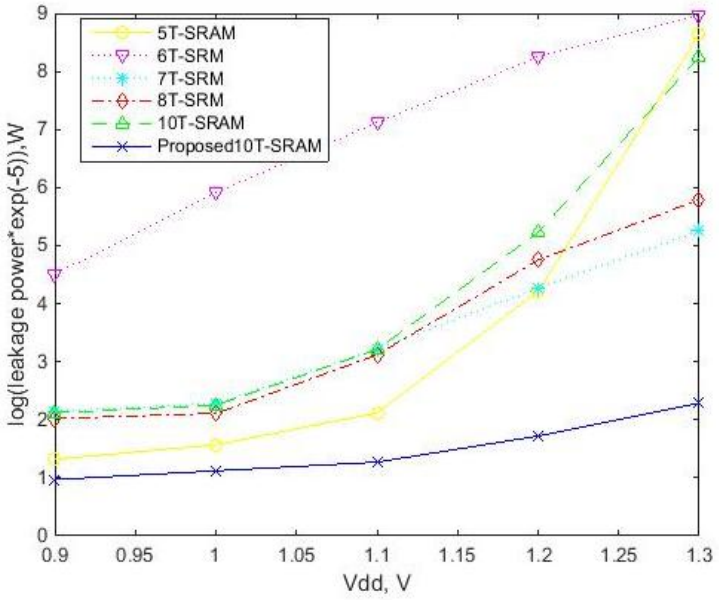

Fig: 3. ***Power comparisons of SRAM bit cells***

	5T	6T	7T	8T	10T	Proposed 10T
Transistor count	5	6	7	8	10	10
No. of BLs	1	2	2	3	3	2
No. of WLs	1	1	2	2	2	1
Area(µm)	-	1.9984	2.2016	2.6578	3.3159	2.0129
Area overhead*	-	-	11%	33%	66%	2%

Table: 1. Comparison of different SRAM cells

***** Here area over head is compared with the standard 6T

V.CONCLUSION

In this aspect , newly designed 10T SRAM cell architecture is proposed. It devours less power compared to 5T, 6T, 8T and 10T cells. The cell is advantageous which is capable of saving up to 45.7%, 0.89%, 50.2%and 81% when compared to 10T, 8T, 5T and 6T cells respectively as shown in the fig:3. From the table: 1, proposed architecture has only 2% area overhead compared to standard 6T. The optimum CR=1.25 and PR=3.0 for beneficient SNM. The new architecture suggested in this letter has a low leakage and high stable and which is recommended for the low power requirements.

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