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Study and Analysis of Combinational Logic Circuits Using Various Techniques

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ABSTRACT

By implementing the self resetting logic to the digital circuit, the power dissipation is drastically reduced. In the VLSI Design this low power technique is very advanced for DSP applications. The dynamic circuits are becoming increasingly popular because of the speed advantage over static CMOS logic circuits; hence they are widely used today in high performance and low power circuits. Self-resetting logic is a commonly used piece of circuitry that can be found in use with memory arrays as word line drivers. Self resetting logic implemented in dynamic logic families have been proposed as viable clock less alternatives. The combinational logic is a type of digital logic which is implemented by Boolean circuits, where the output is a pure function of the present input only.

Digital signals are processed by the digital system which can be built with various logic gates. These logic circuits are made of various logic gates, by connecting them in certain combinations, in order to produce the required output. Digital logic circuits are mainly classified into two types, sequential logic circuits and combinational logic circuits. This article gives a brief idea about the combinational logic circuits.

Keywords: High speed, VLSI, Self-resetting logic (SRL), topologies, power dissipation.

I.INTRODUCTION

Combinational Logic Circuits are made up from basic logic NAND, NOR or NOT gates that are “combined” or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits. An example of a combinational circuit is a decoder, which converts the binary code data present at its input into a number of different output lines, one at a time producing an equivalent decimal code at its output. Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as “universal” gates.

II.FUNCTIONS

The three main ways of specifying the function of a combinational logic circuit are:

1. **Boolean Algebra:** This forms the algebraic expression showing the operation of the logic circuit for each input variable either True or False that results in a logic “1” output. The basic operations of Boolean calculus are as follows.

a) AND (conjunction), denoted $x \wedge y$ (sometimes x AND y or Kxy), satisfies $x \wedge y = 1$ if $x = y = 1$ and $x \wedge y = 0$ otherwise.

b) OR (disjunction), denoted $x \vee y$ (sometimes x OR y or Axy), satisfies $x \vee y = 0$ if $x = y = 0$ and $x \vee y = 1$ otherwise.

c) NOT (negation), denoted $\neg x$ (sometimes NOT x, Nx or !x), satisfies $\neg x = 0$ if $x = 1$ and $\neg x = 1$ if $x = 0$.

2. Truth Table: A truth table defines the function of a logic gate by providing a concise list that shows all the output states in tabular form for each possible combination of input variable that the gate could encounter.

3. Logic Diagram: This is a graphical representation of a logic circuit that shows the wiring and connections of each individual logic gate, represented by a specific graphical symbol, that implements the logic circuit.

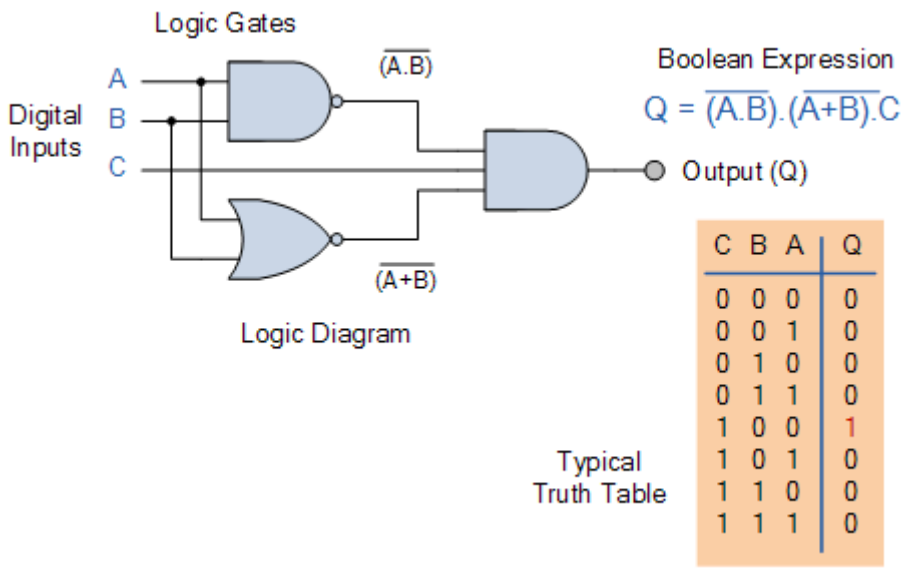

Figure 1: logic circuit representations

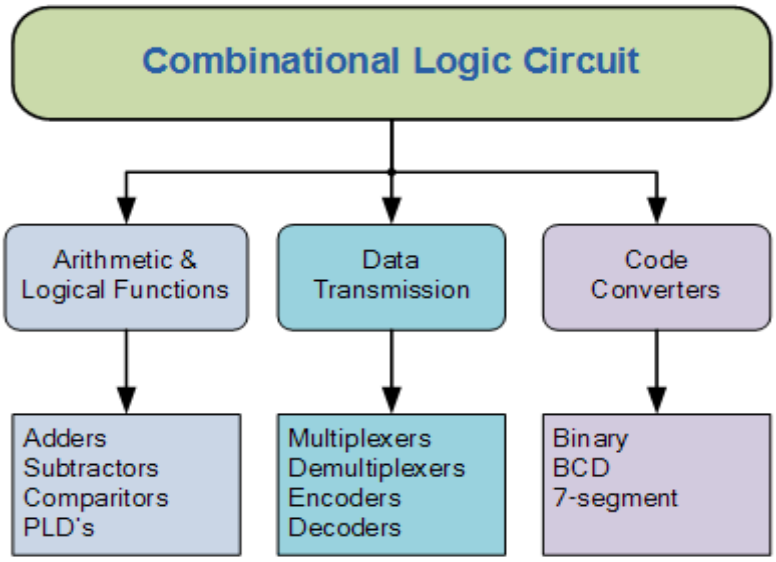

Figure 2: Classification of Combinational Logic

Logic circuits are classified into two types, "combinational" and "sequential."

A combinational logic circuit is one whose yields depend just on its present sources of info. The turning station selector handle on an out-dated TV resembles a combinational circuit—its "yield" chooses a channel construct just with respect to the present position of the handle ("input"). The yields of a successive logic circuit depend on the present contributions as well as on the past arrangement of data sources, conceivably self-assertively far back in time. The channel selector controlled by the all over pushbuttons on a TV remote control is a consecutive circuit—the channel determination relies upon the past succession of up/down pushes, in any event since when you began seeing, and maybe as far back as when you initially fueled up the gadget.

A combinational circuit may contain a discretionary number of logic entryways and inverters however no criticism circles. A. criticism circle is a flag way of a circuit that enables the yield of an entryway to spread back to the contribution of that same door; such a circle for the most part makes consecutive circuit conduct. In combinational circuit investigation we begin with a logic chart and continue to a formal portrayal of the capacity performed by that circuit, for example, a reality table or a logic articulation.

III.COMBINATIONAL LOGIC CIRCUITS USING BOOLEAN ALGEBRA

In computerized circuit hypothesis, combinational logic (once in a while likewise alluded to as time-free logic) is a sort of advanced logic which is actualized by Boolean circuits, where the yield is an unadulterated capacity of the present info as it were. This is as opposed to consecutive logic, in which the yield depends on the present contribution as well as on the historical backdrop of the info. As it were, successive logic has memory while combinational logic does not. Combinational logic is utilized as a part of PC circuits to perform Boolean variable based math on input signals and on put away information. Functional PC circuits typically contain a blend of combinational and consecutive logic. For instance, the piece of a number-crunching logic unit, or ALU, that does numerical counts is developed utilizing combinational logic. Different circuits utilized as a part of PCs, for example, half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders are likewise made by utilizing combinational logic. Combinational logic is utilized as a part of PC circuits to do Boolean polynomial math on input signals and on put away information. Useful PC circuits ordinarily contain a blend of combinational and successive logic. The piece of a number juggling logic unit, or ALU, that does scientific estimations is developed utilizing combinational logic. Different circuits utilized as a part of PCs, for example, half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders are likewise made by utilizing combinational logic circuits. So this paper exhibits an outline development for primitive entryways and viper circuits which lessen postponement and clock skew when contrasted with the dynamic logic snake execution.

Improvement of Combinational Logic Circuits Using Boolean Algebra

- Complex combinational logic circuits must be diminished without changing the capacity of the circuit.
- Reduction of a logic circuit implies a similar logic work with less entryways and additionally inputs.
- The initial step to diminishing a logic circuit is to compose the Boolean Equation for the logic work.

- The following stage is to apply however many tenets and laws as could be allowed keeping in mind the end goal to diminish the quantity of terms and factors in the articulation.
- To apply the tenets of Boolean Algebra it is regularly useful to first evacuate any enclosures or sections.
- After evacuation of the enclosures, basic terms or factors might be expelled leaving terms that can be diminished by the principles of Boolean Algebra.
- The last advance is to draw the logic outline for the diminished Boolean Expression.

Combinational Logic Circuits Using self-resetting CMOS

Another class of dynamic circuits, called self-resetting CMOS (SRCMOS), speaks to signals as brief span beats as opposed to as voltage levels. At the point when an arrangement of heartbeats are sent to the contributions to a logic entryway, they should touch base at basically a similar time and they should cover with each other for a base term. After a logic entryway has handled an arrangement of information beats, a reset flag is actuated that reestablishes the logic door to a state in which it can get another arrangement of information beats. The reset operation is coordinated to happen after the information beats have come back to zero..

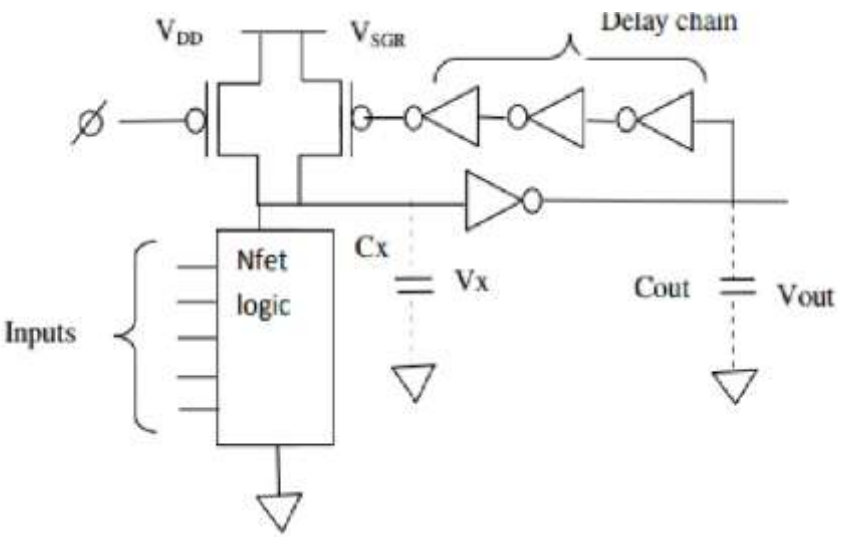

Fig.3: Basic Structure of a Self Resetting Logic Circuit

Thus, there is no need for an evaluate or "foot" transistor since the pull-down network will be off during the reset operation, and this is one of the factors that leads to high-speed operation. Moreover, since the reset occurs immediately after each gate has evaluated, there is no need for a separate precharge phase. Since short-duration pulses are hard to debug and test, special additional test-mode features are sometimes added for these purposes. Two types of reset structures have been proposed for use in SRCMOS. In globally self-resetting CMOS [4], the reset signal for each stage is generated by a separate timing chain which provides a parallel worst-case delay path. Individual reset signals are obtained at various tap points along this timing chain in such a way that the reset pulse arrives at each stage only after the stage has completed its evaluation.

Combinational Logic Circuits Using Quantum-dot Cellular Automata (QCA)

The size of CMOS transistors are decreasing day by day and it will eventually reaches its limitations hence it become necessary to develop an alternate to continually improve the development of electronics devices. The alternatives to conventional CMOS technology, for attaining high computational power and compact design density, are therefore being investigated Quantum-dot cellular automata (QCA) is introduced to create nanoscale devices with high compaction density, capable of performing computation at very high switching speed. Most quantum device designs examined have been similar to classical device implementations in that they use currents and voltages to encode information.QCA is a potential device It does not involve any voltage or current to encode the information. Position of single electron using Coulombic repellent force has been used to encode the information. Each QCA cells consists of four quantum dots. Two electrons are loaded, in antipodal sides which determine the logic 0" and 1" . QCA cells are used to implement combinational logic circuits.

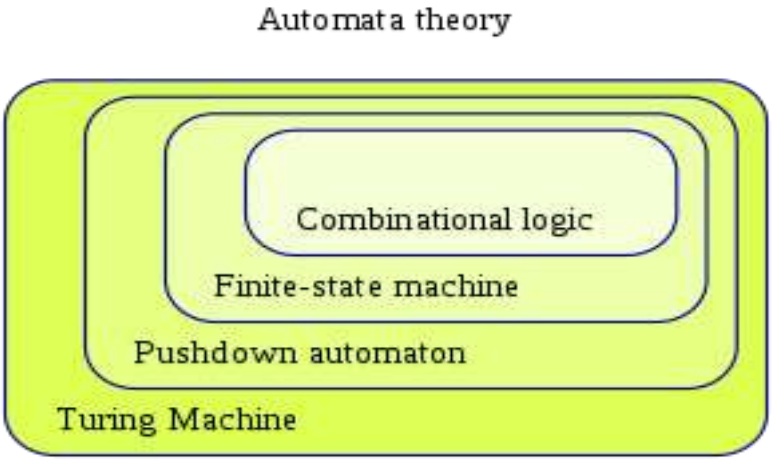

Fig.4: Basic Representation of Automata Theory

Quantum cell automata is a promising nanotechnology that has been perceived as one of the main six rising innovation in future PCs. In this, the strategy for larger part voting plan is utilized to create essential QCA combinational and successive circuits. Using the QCA innovation for actualizing logic circuits is one of the methodologies, QCA can be utilized to execute combinational circuits by appropriately masterminding cells in arrangement. As of late a few examinations have been accounted for about combinational circuit outline, for example, QCA full viper. Quantum-dab Cellular Automata is one of the promising advances for future age ICs QCAs were presented in 1993 by loaned et al, and tentatively checked in 1997. It is relied upon to accomplish high gadget thickness, greatly low power utilization and high exchanging speed .The QCA offers another transistor less figuring worldview in nanotechnology. QCA can be utilized to make s littler gadgets gadget with high calculation exchanging velocity and low power utilization. this make inquire about on QCA prominent and imperative to supplant CMOS transistors in Nano-scale innovation manufacture. That can be utilized to actualize the consecutive and the combinational circuits. It is an alternate sort of innovation that will supplant MOSFET in future. Quantum Cellular Automata (QCA) is a nanotechnology that has as of late been perceived

as one of the best six rising advancements with potential applications in future PCs. It has increased critical prominence as of late. This is principally because of rising enthusiasm for making processing gadgets and executing any legitimate capacity with that. The essential building piece of QCA circuit is lion's share entryway; thus, effectively developing QCA circuits utilizing larger part doors has pulled in a great deal of considerations. A few examinations have announced that QCA can be utilized to configuration universally useful computational and memory circuits. QCA is relied upon to accomplish high gadget thickness, high clock recurrence and to a great degree low power utilization. Lately the improvement of incorporated circuits has been basically in view of downsizing that is, expanding the component thickness on the wafer. Downsizing of reciprocal metal oxide semiconductor CMOS circuits, be that as it may, has its points of confinement. Over a specific component thickness different physical wonders, including quantum impacts, scheme to make transistor operation troublesome if certainly feasible. On the off chance that another innovation is to be made for gadgets of nanometer scale, new plan standards are fundamental. One promising methodology is to move to a transistor less cell engineering in view of communicating quantum specks, quantum spot cell automata QCA

Combinational Logic Circuits utilizing Quantum-dab cell automata

Combinational Logic Circuits comprise of data sources, at least two fundamental logic entryways and yields. The logic entryways are joined such that the yield state depends completely on the info states. Combinational logic circuits have "no memory", "timing" or "input circles", there operation is prompt. A combinational logic circuit plays out an operation doled out consistently by a Boolean articulation or truth table. If two QCA cells are set beside each other, it is conceivable to trade their states, i.e. the modifications of the electrons in them. The QCA cell that should exchange its state to a neighboring cell must have its passage intersections shut, the passage intersections in the neighboring cell must be open, to enable the electrons to go through the passage intersections between the potential wells. When they open, the electrons in the neighboring cell are pushed by the Coulomb power of the first cell as far away as could reasonably be expected. As they likewise are pushed far from each other, they will go into an indistinguishable potential wells from in the first cell. When the passage intersections are shut once more, the exchange of the state is finished. The condition of a phone can likewise be exchanged to numerous neighboring cells. It works the extremely same route as with a solitary neighbor cell, however the passage intersections of all the successively neighboring cells ought to be open in the meantime, which makes the exchange significantly speedier at that point exchanging the state cell by cell. This enables us to fabricate "wires", made of QCA cells, to transport data over bigger separations.

There has been expanding worry as of late that the breaking points of what can be accomplished with current ways to deal with enhancing gadget execution will soon be come to. Quantum-dab cell automata (QCA) is been proposed as a methods for getting around these restrictions. Quantum Cellular Automata is a promising nanotechnology that has been perceived as one of the main six developing innovation in future PCs. In this, the technique for larger part voting plan is utilized to create fundamental QCA combinational and consecutive circuits. Using the QCA innovation for actualizing logic circuits is one of the methodologies, QCA can be utilized to execute combinational circuits by legitimately masterminding cells in arrangement. As of late a few

investigations have been accounted for about combinational circuit plan, for example, QCA full viper. Quantum-dab Cellular Automata is one of the promising advances for future age ICs.

Combinational Logic Circuits utilizing Genetic Algorithm Based Design

For ideal plan of electronic circuits, developmental outline is a feasible option. Transformative Algorithm is the most vital element in evolvable equipment applications. The calculation needs to create ideal circuits, which thus must be actualized on a programmable gadget. In the outline of computerized circuits, landing at the negligible capacity is of incredible essentialness. Utilizing an advanced plan the many-sided quality of the circuit can be decreased, along these lines diminishing the power utilization and cost. Real plan criteria include the postponement of the circuit and the region of the chip which specifically decides the assembling cost. Additionally control dispersal assumes a noteworthy part on the pressing and cooling expense of the framework included. Traditional techniques like Karnaugh guide and Quine McCluskey don't bolster the utilization of XOR, XNOR, or any of the essential building squares like multiplexers or Reed Muller Logic Modules.

IV.SYNTHESIS Vs DESIGN

Logic circuit design is a superset of synthesis, since in a real design problem we usually start out with an informal (word or thought) description of the circuit. Often the most challenging and creative part of design is to formalize the circuit description defining the circuit's input and output signals and specifying its functional behavior by means of truth tables and equations. Once we've created the formal circuit description, we can usually follow a "turn-the-crank" synthesis procedure to obtain a logic diagram for a circuit with the required functional behavior. The material in the first four sections of this chapter is the basis for "turn-the-crank" procedures whether the crank is turned by hand or by a computer. The next chapter describes hardware description languages—ABEL, VHDL and Verilog. When we create a design using one of these languages, a computer program can perform the synthesis for us. Combinational circuits may have one or more outputs. In this chapter we'll discuss methods that apply to single-output circuits. Most analysis synthesis techniques can be extended to handle multiple-output circuits (e.g., "repeat these steps for each output"). The purpose of this chapter is to give you a solid theoretical foundation for the analysis and synthesis of combinational logic circuits, a foundation that will be especially important when we move on to sequential circuits. Although most of the analysis and synthesis procedures in this chapter are automated nowadays by computer-aided design tools, you need a basic understanding of the fundamentals to use the tools and to figure out what's wrong when you get unexpected or undesirable results.

V.CONCLUSIONS

Most of the combinational circuits are available in integrated circuits (ICs) which are extensively used in the design of the digital systems. Depends on the integration capability of gates, these ICs are classified into small, medium, large and very large scale ICs. For performing specific digital functions such as addition, multiplexing, de-multiplexing, encoding, decoding, comparison, etc., mostly medium scale integrated (MSI) ICs are used in digital systems.

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