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# IMPLEMENTATION OF DATA ENCODING AND DECODING ARCHITECTURE FOR NOC APPLICATION

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**ABSTRACT:**

*As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper, we present a set of data encoding schemes aimed at reducing the power dissipated by the links of an NoC. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture). Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.*

***Keywords — Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip(NoC)***

## I. INTRODUCTION

Shifting from a silicon technology node to the next one results in faster and more power efficient gates but slower and more power hungry wires [1]. In fact, more than 50% of the total dynamic power is dissipated in interconnects in current processors, and this is expected to rise to 65%–80% over the next several years [2]. Global interconnect length does not scale with smaller transistors and local wires. Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially. At 32/28 nm, for instance, the RC delay in a 1-mm global wire at the minimum pitch is 25× higher than the intrinsic delay of a two-input NAND fan out of 5[1]. If the raw computation horsepower seems to be unlimited, thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem [3]. The network-on-chip (NoC) design paradigm [4] is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultra-deep submicron meter era. Nowadays, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation-related issues [4]. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption, reliability, etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system-on-chip (SoC) is due to the communication subsystem.

In this paper, we focus on techniques aimed at reducing the power dissipated by the network links. In fact, the power dissipated by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [5].

In particular, we present a set of data encoding schemes operating at flit level and on an end-to-end basis, which allows us to minimize both the switching activity and the coupling switching activity on links of the routing paths traversed by the packets. The proposed encoding schemes, which are transparent with respect to the router implementation, are presented and discussed at both the algorithmic level and the architectural level, and assessed by means of simulation on synthetic and real traffic scenarios. The analysis takes into account several aspects and metrics of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes up to 51% of power and up to 14% of energy can be saved without any significant degradation in performance and with 15% area overhead in the NI. The results for the hardware overhead, power and energy savings, and performance reduction of the proposed data encoding schemes are compared with those of other approaches.

## II. RELATED WORKS AND CONTRIBUTIONS

In these chips, a significant fraction of the total system power budget is dissipated by interconnection networks [6]. Therefore, the design of power-efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architectures. These works concentrate on different components of the interconnection networks such as routers, NIs, and links. Since the focus of this paper is on reducing the power dissipated by the links, in this section, we briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasing line-to-line spacing [9], [10] and repeater insertion [11].They all increase the chip area. The data encoding scheme is another method that was employed to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In the first category, encoding techniques concentrate on lowering the power due to self-switching activity of individual Bus lines while ignoring the power dissipation owing to their coupling switching activity. In this category, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted via these lines. On the other hand, gray code [14] T0 [15] working-zone encoding [16] and T0-XOR were suggested for the case of correlated data patterns. Application-specific approaches have also been proposed [18]-[22]. This category of encoding is not suitable to be applied in the deep submicron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the aforementioned techniques, which ignore such contributions, inefficient [23]. The works in the second category concentrate on reducing power dissipation through the reduction of the coupling switching [22]-[30]. Among these schemes [24]-[28], the switching activity is reduced using many extra control lines. The techniques proposed have a smaller number of control lines but the complexity of their decoding logic is high. The technique described in is as follows: first, the data are both odd inverted and even inverted, and then transmission is performed using the kind of inversion which reduces more the switching activity. In [30] the coupling switching activity is reduced up to 39%. In this paper, compared to that, we use a simpler decoder while achieving a higher activity reduction. Let us now discuss in

more detail the works with which we compare our proposed schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance, and hence, should be considered in any scheme proposed for the link power reduction.

**TABLE I**

EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

| Time | Normal | | | Odd Inverted | | |
|---|---|---|---|---|---|---|
| | Type I | | | Types II, III, and IV | | |
| t − 1<br>t | 00, 11<br>10, 01 | 00, 11, 01, 10<br>01, 10, 00, 11 | 01, 10<br>11, 00 | 00, 11<br>11, 00 | 00, 11, 01, 10<br>00, 11, 01, 10 | 01, 10<br>10, 01 |
| | T1* | T1** | T1*** | Type III | Type IV | Type II |
| t − 1<br>t | Type II<br>01, 10<br>10, 01 | | | Type I<br>01, 10<br>11, 00 | | |
| t − 1<br>t | Type III<br>00, 11<br>11, 00 | | | Type I<br>00, 11<br>10, 01 | | |
| t − 1<br>t | Type IV<br>00, 11, 01, 10<br>00, 11, 01, 10 | | | Type I<br>00, 11, 01, 10<br>01, 10, 00, 11 | | |

In addition, the scheme was based on the hop-by-hop technique, and therefore, encoding/decoding is performed in each node. The scheme presented [26] in dealt with reducing the coupling switching. In this method, a complex encoder counts the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two. If the number is larger than half of the link width, the inversion will be performed. In addition to the complex encoder, the technique only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to higher link power consumption. Therefore, the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the h op-by-hop technique.

In another coding technique presented in bunches of four bits are encoded with five bits. The encoded bits were isolated using shielding wires such that the occurrence of the patterns “101” and “010” were prevented. This way, no simultaneous Type II transitions in two adjacent pair bits are induced. This technique effectively reduces the coupling switching activity. Although the technique reduces the power consumption considerably, it increase the data transfer time, and, hence, the link energy consumption. This is due to the fact that for each four bits, six bits are transmitted which increases the communication traffic. This technique was also based on the hop-by-hop approach. A coding technique that reduces the coupling switching activity by taking the advantage of end-to-end encoding for worm hole switching has been presented. It is based on lowering the coupling switching activity by eliminating only Type II transitions.

In this paper, we present three encoding schemes. In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even inverts and make the inversion which leads to the higher power saving.

## III. DESIGN METHODOLOGY

The main goal of the proposed encoding scheme is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. Let us first describe the power model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P = [T_{0\rightarrow1}(C_s + C_l) + T_c C_c] V_{2dd} F_{ck} \qquad (1)$$

Where,

T 0→1 is the number of 0 → 1 transitions in the bus in two consecutive transmissions.

Tc is the number of correlated switching between physically adjacent lines.

Cs is the line to substrate capacitance.

Cl is the load capacitance.

Cc is the coupling capacitance.

Vdd is the supply voltage and

Fck is the clock frequency.

A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type and hence the coupling transition activity. Tc is a weighted sum of different types of coupling transition contributions [26].

Therefore,

$$\bar{T}c = K_1\bar{T}_1 + K_2\bar{T}_2 + K_3\bar{T}_3 + K_4\bar{T}_4 \qquad (2)$$

Where,

Ti is the average number of Type i transition and

Ki is its corresponding weight.

According to the above equation, we use

K1 = 1, K2 = 2, and K3 = K4 = 0.

The occurrence probability of Types I and II for a random set of data is 1/2 and 1/8 respectively.

This leads to a higher value for K1T1 compared with K2T2 suggesting that minimizing the number of Type I transition may lead to a considerable power reduction

Using (2), Equation (1) can express as

$$\bar{P} = [\bar{T}_{0\rightarrow1}(C_s + C_l) + (\bar{T}_1 + \bar{2}T_2) C_c] V_{2dd} F_{ck} \qquad (3)$$

According to equation (3),

Cl can be neglected

$$P \propto T_{0\to1} C_s + (T_1 + 2T_2) C_c \qquad (4)$$

Here, we calculate the occurrence probability for different types of transitions. Consider that flit (t − 1) and flit (t) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur. Note that the first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its (i +1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively.

The three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

### 3.1 Scheme I

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

### 3.2 Power Model

If the flit is odd inverted before being transmitted, the dynamic power on the link is where,

$T_{0\to1}$, $T_1$, $T_2$, $T_3$, and $T_4$, are the self-transition activity and the coupling transition activity of Types I, II, III, and IV respectively. Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted as is and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic ith line of the link, whereas the second bit values at time t − 1 (t). As Table 3.1 shows, if the flit is odd inverted, Types II, III and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III or Type IV transitions. In particular, the transitions indicated as $T*1$ , $T**1$ and $T***1$ in the table convert to Types II, III and IV transitions, respectively.

Also, we have

$T_{0\to1} = T_{0\to0}(\text{odd}) + T_{0\to1}(\text{even})$

Where odd/even refers to odd/even lines.

Therefore, equation (5) can be expressed as

$$P \propto T_{0\to0}(\text{odd}) + T_{0\to1}(\text{even}) C_s + [K_1(T_2+T_3+T_4) + K_2 T***1 + K_3 T*1 + K_4 T**1] C_c \qquad (6)$$

Thus, if $P > P_1$, it is convenient to odd invert the flit before transmission to reduce the link power dissipation. Using (4) and (6) and noting that $C_c/C_s = 4$

We obtain the following odd invert condition

$1/4 T_{0\to1} + T_1 + 2T_2 > 1/4(T_{0\to0}(\text{odd}) + T_{0\to1}(\text{even})) + T_2 + T_3 + T_4 + 2T***1$ .

Also, since $T_{0\to1} = T_{0\to1}(odd) + T_{0\to1}(even)$

Equation (1) can written as

$1/4T_{0\to1}(odd)+T_1+2T_2>1/4T_{0\to0}(odd)+T_2+T_3+T_4+2T***1$ (7)

which is the exact condition to be used to decide whether the odd invert has to be performed. Since the terms T0→1(odd) and T0→0(odd) are weighted with a factor of 1/4, for link widths greater than 16 bits.

### 3.2.1 Encoding Architecture

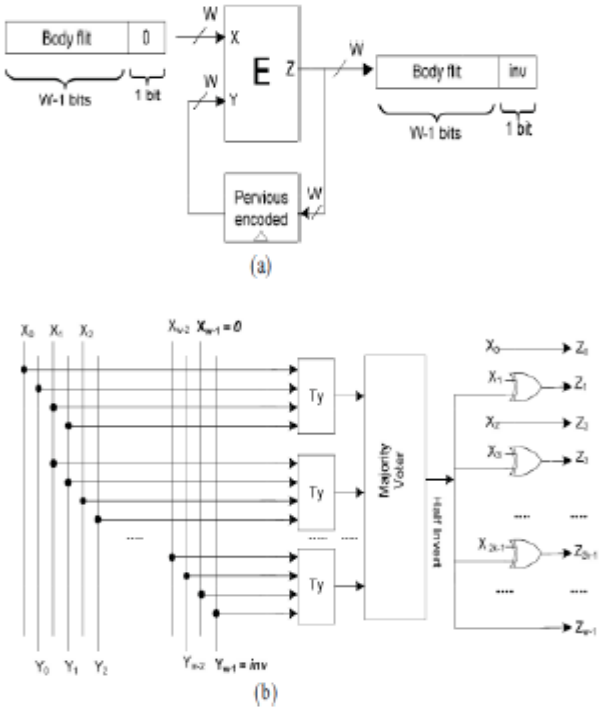


**Figure 1: Encoder architecture scheme I.**

**(a) Circuit diagram.**

**(b) Internal view of the encoder block [E].**

The use of the approximated odd invert condition reduces the effectiveness of the encoding scheme due to the error induced

By the approximation but it simplifies the hardware implementation of encoder.

Now, defining

$Tx = T3 + T4 + T ***1$ (8)

and

$Ty = T2 + T1 - T ***1$ (9)

Equation (8) can written as

$Ty > Tx$ (10)

Assuming the link width of w bits, the total transition between adjacent lines is w − 1, and

Hence,

$Ty + Tx = w - 1$ (11)

Thus, Equation (10) can written as

$Ty > (w - 1)2$ (12)

This presents the condition used to determine whether the odd inversion has to be performed or not.

The proposed encoding architecture, which is based on the odd invert condition defined by (12), is shown in Figure We consider a link width of w bits. If no encoding is used, the body flits are grouped in w bits by the NI and are transmitted via the link. In this approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not.

The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. The generic block diagram shown in Figure is the same for all three encoding schemes proposed in this paper and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of $w - 1$ payload bits and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder [Fig.3.1(b)]. The $w - 1$ bits of the incoming (previous encoded) body flit are indicated by

Xi (Yi ), i = 0, 1, . . . ,w − 2.

The wth bit of the previously encoded body flit is indicated by inv which shows

if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., X1X2Y1Y2, X2X3Y2Y3, X3X4Y3Y4 etc.) and sets its output to "1" if any of the transition types of Ty is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation.

### 3.3 SCHEME II

#### 3.3.1 Encoding Architecture

The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture which is based on the even invert condition, full invert condition and the odd invert condition. The $w^{th}$ bit of the previously encoded body flit is indicated by inv which shows if it was even, odd, or full inverted (inv = 1) or left as it was (inv = 0).The first stage of the encoder determines the transition types while the second stage is formed by a set of 1s blocks which count the number of ones in their inputs. In the first stage, we have added the Te blocks which determine if any of the transition types of T2, T **1 and T ***1 is detected for each pair bits of their inputs. For these transition types, the even invert action yields link power reduction. Again, we have four ones blocks determined the number of detected transitions for each Ty, Te, T2, T **4, blocks.

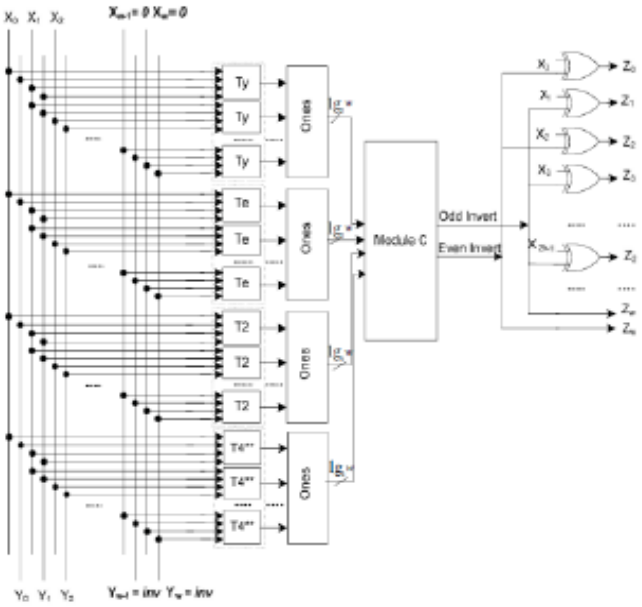


**Figure 2: Encoder architecture Scheme II**

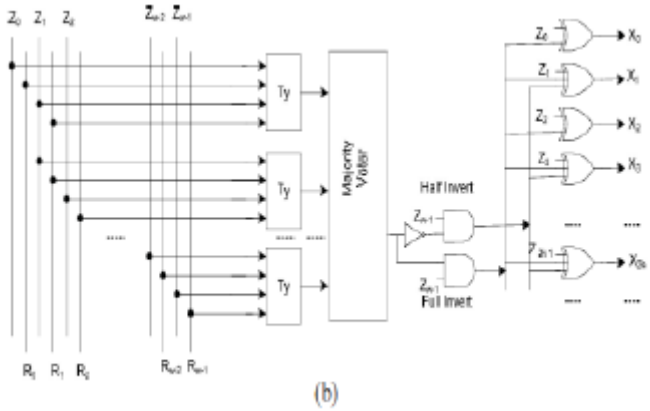


**Figure3: Decoder architecture Scheme I**

The output of the Ones blocks are inputs for Module C. This module determines if odd, even, full, or no invert action corresponding to the outputs "10," "01," "11," or "00," respectively, should be performed.

## IV. RESULTS AND DISCUSSION

In scheme I, we focus on reducing the number of type I transitions (by converting them to type III and IV transitions) and type II transitions (by converting them to type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction. If the flit is odd inverted, types II, III and IV transitions are converted to type I transitions. In case of type I transitions, the inversion leads to one of the types II, III and type IV transitions. he proposed data encoding schemes have been assessed by means of a cycle-accurate NoC simulator based on Noxim [32]. The power estimation models of Noxim include NIs, routers, and links. The link power dissipation was computed using (3) where the terms $T0\rightarrow1$, $T1$, and $T2$ were computed based on the information obtained from the cycle-accurate simulation. The following parameters were used in the simulations. The NoC was clocked at

700 MHz while the baseline NI with minimum buffering and supporting open core protocol 2 and advanced high-performance bus protocols dissipated 5.3 mW. The average power dissipated by the wormhole-based router was 5.7 mW. Based on a 65-nm UMC technology, a total capacitance of 592 fF/mm was assumed for an inter-router wire. About 80% of this capacitance was due to the crosstalk. We assumed 2-mm 32-bit links and a packet size of 16 bytes (eight flits). Using the detailed simulations, when the flits traversed the NoC links, the corresponding self-and coupling switching activities were calculated and used along with the self- and coupling capacitance of 0.237 and 0.947 nf, respectively, to calculate the power (Vdd = 0.9 V and Fck = 700 MHz).

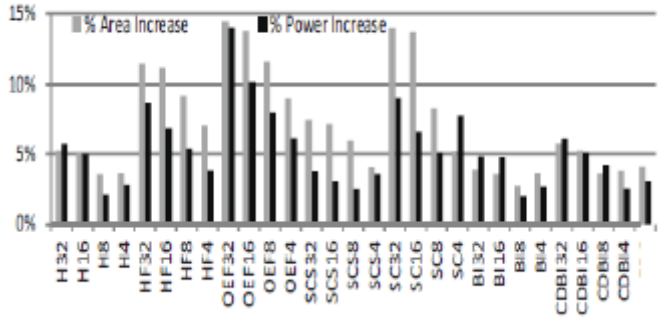


**Figure4: Percentage impact on silicon area and power dissipation of the network interface due data encoding/decoding**

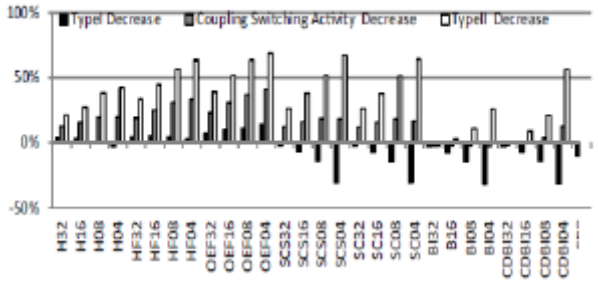


**Figure5: Total power/energy saving using different data encoding schemes.**

## V. CONCLUSION

A set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the rationale behind the proposed schemes is to minimize not only the switching activity, but also (and in particular) the coupling switching activity which is mainly responsible for link power dissipation in the deep submicron meter technology regime. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. The encoders implementing the proposed schemes have been assessed in terms of power dissipation and silicon area. The impacts on the performance, power, and energy metrics have been studied using a cycle- and bit-accurate NoC simulator under both synthetic and real traffic

scenarios. Overall, the application of the proposed encoding schemes allows savings up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

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